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A Batteryless Motion-Adaptive Heartbeat Detection System-on-Chip Powered by Human Body Heat

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Abstract

This paper presents a batteryless heartbeat detection system-on-chip (SoC) powered by human body heat. An adaptive threshold generation architecture using pulse-width locked loop (PWLL) is developed to detect heartbeats from electrocardiogram (ECG) in the presence of motion artifacts. The sensing system is autonomously powered by harvesting thermal energy from human body heat using a thermoelectric generator (TEG) coupled to a low-voltage, self-starting boost converter and integrated power management system. The SoC was implemented in a 0.18 μm CMOS process and is fully functional with a minimum input power of 20 μW , provided by a portable TEG at 20 mV with a ~ 0.5 $^{\circ}\text{C}$ temperature gradient. The complete system demonstrates motion-adaptive, power-autonomous heartbeat detection for sustainable healthcare using wearable devices.

Keywords

Wearable devices; thermoelectric energy harvesting; heartbeat; motion artifacts; batteryless; body heat

I. Introduction

WEARABLE devices can enable ambulatory measurement of human vital signs and continuous monitoring of physiological parameters, which may be valuable for chronic care and early diagnosis of disease [1], [2]. However, medically relevant recording of vitals outside of the clinic is challenging: motion artifacts degrade signal quality and detection accuracy, demanding energy-intensive signal processing. Also, long-term monitoring requires continuous, untethered power, difficult to obtain from portable batteries.

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Heart rate serves as a primary vital sign to monitor cardiovascular health [3], and continuous heartbeat monitoring can detect pulse irregularities to diagnose underlying conditions [4]; conventionally, an electrocardiogram (ECG) is used. Low-power ECG acquisition systems suitable for wearable applications are extensively reported in the literature, where techniques such as voltage scaling, compressed sampling, and duty-cycled transmission reduce overall power consumption [5]-[10]. However, the energy-efficiency of many such systems is limited to analog signal conditioning blocks; feature extraction requires digitization and back-end processing, necessitating additional hardware and energy. In addition, these systems do not mitigate real-world motion artifacts. Artifact cancellation using motion-correlated bio-impedance signals acquired in parallel or external calibration can enable ambulatory monitoring, but this incurs additional power consumption [11]-[13].

Prolonged monitoring using wearable devices typically requires frequent recharging or replacement of batteries. Ambient energy harvesting is an attractive alternative to provide complete power-autonomy. While solar and kinetic energy are possible energy sources to harvest, neither are available continuously and still require battery-based energy storage. Wireless power transmission via radio frequency (RF) [14] or inductive links [15] can be a useful battery substitute, but the resulting devices depend on the continuous availability of transmitted power.

In comparison, human body heat is available across day and night and can serve as an ambient energy source for powering body-worn devices using portable thermoelectric generators (TEG) [16]. However, the small temperature gradient ($\sim 1\text{-}2^\circ\text{C}$) between skin and ambient environment provides only tens of millivolts from a centimeter-scale TEG. Primary challenges in developing energy harvesters for such devices include efficient high-gain voltage conversion at such low input voltage, as well as low-voltage self-start. While previous work has demonstrated TEG-based body-heat energy harvesting for powering wearable SoCs, the implementations require additional energy sources such as RF [8] or solar [17] for fully-autonomous operation.

In this work, we present a batteryless, motion-adaptive heartbeat detection system powered continuously by energy harvested from human body heat [18]. To mitigate the effect of motion artifacts, the developed architecture uses a pulse-width locked loop (PWLL) to generate an adaptive threshold voltage for a heartbeat detection algorithm. This approach uses low-power analog processing of an ECG signal to provide robust rejection of both slow and fast motion artifacts, enabling accurate detection of heartbeats in an ambulatory environment. The SoC is powered by a low-voltage, self-starting DC-DC boost converter, enabling a minimum number of off-chip components; a portable TEG, an inductor, and two storage capacitors enable autonomous, efficient body-heat energy harvesting in a wearable form factor. The SoC was fabricated in a $0.18\text{ }\mu\text{m}$ CMOS process and self-starts with a supply voltage as low as 55 mV. The system is powered using a centimeter-scale TEG and remains fully functional with a minimum TEG supply of 20 mV and an input power of 20 μW .

The rest of the paper is organized as follows: Section II gives a brief description of the SoC architecture; Section III describes a low-power, motion-adaptive threshold generation and

heartbeat detection scheme; Section IV describes energy harvesting circuits; front-end analog circuits for ECG signal conditioning, along with digital back-end circuits, are described in Section V; prototype chip implementation details and measurement results are discussed in Section VI; and, brief conclusions are provided in Section VII.

II. Heartbeat detection SoC Architecture

The batteryless heartbeat detection system is shown in Fig. 1, where the SoC architecture comprises four primary blocks. The power management unit for energy harvesting has a core DC-DC boost converter with an off-chip inductor, L , on-chip start-up, control, and downstream circuits for power delivery. A low-voltage, on-chip voltage multiplier boosts the input voltage initially and powers the start-up circuits to activate the primary boost converter from cold-start [19]. Following cold-start, the output voltage of the boost converter, DV_{DD} , reaches 1.5 V and is regulated by a hysteretic on-off voltage regulator. To provide a clean supply for analog signal conditioning circuits, DV_{DD} is further regulated to $AV_{DD}=1.2$ V using a low-dropout (LDO) regulator and on-chip bandgap voltage reference. Two external storage capacitors are required: one at the output of the TEG, and another at the boosted voltage output of the converter; a 1 μ F storage capacitor on DV_{DD} is sufficient to support digital circuit switching currents.

For heartbeat detection, the ECG signal from the human body is acquired using two gel electrodes and processed with an analog front-end (AFE) block connected to the electrodes. The AFE output is compared against two independent adaptive threshold voltages for accurate heartbeat detection in the presence of motion artifacts. The outputs of the double-sided comparison block are further used by the digital back-end circuits for motion-artifact-resilient heartbeat (HB) detection. Detected heartbeats are transmitted wirelessly in 1 ms bursts using near-field communication via an on-off keying (OOK) modulation scheme. The local oscillator (LO), power amplifier (PA), and mixer in the transmitter block are all powered by DV_{DD} . Detected heartbeat pulses are also available directly at the *HB* port.

The SoC is bonded to a quad flat no-lead (QFN) package and is connected to peripheral components on a 3 cm $\times$ 3 cm printed circuit board. A commercial TEG [20] of dimension 3 cm $\times$ 3.4 cm is used for converting body heat into electrical energy. The equivalent circuit of the TEG (Fig. 1) is a DC voltage source, V_{TEG} , with a small source impedance, R_{TEG} , typically a few ohms. The TEG voltage is proportional to the temperature difference, T , between its surfaces.

III. Heartbeat detection and motion artifacts

Heartbeats occur as QRS peaks in the ECG waveform. In real-world ambulatory conditions, the ECG signal is subject to various motion artifacts, as shown in Fig. 2; as such, comparison against a fixed voltage threshold will result in undetected heartbeats. Low frequency artifacts, such as baseline drift due to respiration [22], can be removed by simple capacitive coupling at the input to the AFE, but the high pass response with a fixed cut-off frequency is not robust enough to remove motion artifacts which have undetermined frequency components. Detection using an adaptive threshold generated by signal post-

processing is widely used [23], but this is challenging for highly energy-constrained systems.

In this work, motion information is extracted directly from the ECG signal. The QRS duration, T_0 , is relatively fixed (80-100 ms) for an individual. As is shown in Fig. 3a, the width of this complex at a known voltage reference can be used to track baseline drift and to generate motion-adaptive thresholds for heartbeat detection. Approximating a single QRS complex as a triangle, from the triangle similarity we can obtain,

$$\frac{V_{\text{REF}}(n)}{V_{\text{PK}}(n)} = 1 - \frac{T_{\text{PW}}(n)}{T_0} \quad (1)$$

where $V_{\text{PK}}(n)$ is the peak voltage, $V_{\text{REF}}(n)$ is the reference voltage, and $T_{\text{PW}}(n)$ is the pulse width of the comparator output, V_{CMP} , at the n^{th} QRS complex. In (1), time domain signal, $T_{\text{PW}}(n)$ carries the information of relative voltage position between $V_{\text{PK}}(n)$ and $V_{\text{PK}}(n+1)$. If we compare $T_{\text{PW}}(n)$ with a fixed reference pulse-width, T_{REF} (chosen based on desired steady-state V_{REF}), the pulse-width error, $T(n)$ and proportional error voltage, $V(n)$ can be used to update the reference voltage for the next cycle, $V_{\text{REF}}(n+1)$. This reference tracking is modeled as

$$\begin{aligned} V_{\text{REF}}(n+1) - V_{\text{REF}}(n) &= K \cdot [T_{\text{PW}}(n) - T_{\text{REF}}] \\ &= KT_0 \cdot \left[1 - \frac{T_{\text{REF}}}{T_0} - \frac{V_{\text{REF}}(n)}{V_{\text{PK}}(n)} \right], \end{aligned} \quad (2)$$

where K is a conversion gain from time to voltage. To simplify (2), as well as to apply a linearized frequency domain analysis, we assume $V_{\text{PK}}(n)$ is a step function with a DC amplitude of $V_{\text{PK,dc}}$. A frequency domain analysis provides

$$H(z) = \frac{V_{\text{REF}}(z)}{V_{\text{PK}}(z)} = \frac{R_{\text{REF}} \cdot V_0 / V_{\text{PK,dc}}}{z - (1 - V_0 / V_{\text{PK,dc}})}, \quad (3)$$

where $R_{\text{REF}} = 1 - T_{\text{REF}}/T_0$ and $V_0 = K \cdot T_0$. Note that if $V_{\text{PK}}(n)$ has higher frequency components, (3) no longer holds and the system feedback loop may be unstable, which is discussed in a later section. From (3), the reference adapter, $H(z)$ has a DC gain R_{REF} , and hence it can be used to adapt $V_{\text{REF}}(n)$ with slow variations of $V_{\text{PK}}(n)$.

The low-pass characteristic of $H(z)$ serves the aim of reference tracking in the presence of baseline drift, and tracking bandwidth can be adjusted by controlling K . However, the update rate of this reference tracking is inherently limited to the heart rate, and it is not able to track abrupt transient artifacts, as illustrated in Fig. 4a. To address this challenge, a differentiator is used, where a QRS complex is distinguished by its bipolar slope as compared with unipolar fast artifacts. As is depicted in Fig. 4a, the detection of double-sided peaks validates a true heartbeat, distinct from one-sided peaks due to fast artifacts. Fig. 4b shows the complete block diagram of motion-resilient heartbeat detection architecture. Adaptive reference voltages, V_{REFH} and V_{REFL} are independently generated by comparing the variation of the pulse-widths of the comparator outputs (PW_{H} and PW_{L}) against that of fixed reference pulses (PW_{REFH} and PW_{REFL}) to track changes in both positive as well as

negative peaks of V_{ECGD} . An HB signal is generated when both peaks are detected, indicating a true heartbeat. This double-sided pulse-width tracking makes the heartbeat detection adaptive to both slow and fast artifacts.

This motion-resilient detection approach is uniquely suited to implementation in a power-limited SoC: no ADC or digital processing is required for feature extraction; no precision voltage reference is required, as an approximate reference is sufficient for initializing the tracking loop; utilizing the sparse nature of heartbeats, moving the tracking process from the voltage domain to the time domain saves considerable power; and, the analog front end design constraints are relaxed.

IV. Energy harvesting from body heat

Thermoelectric generators (TEG) with centimeter-scale form factor can generate tens of microwatts of power from a temperature gradient of $\sim 1\text{-}2^\circ\text{C}$, leveraging a low source impedance (R_{TEG}). However, the corresponding output voltage is tens of millivolts making it difficult to directly use the harvested energy for powering electronics; a DC-DC boost converter is needed between the TEG and downstream electronics to boost the input voltage to deliver power to the SoC.

A. Self-starting DC-DC boost converter

The primary challenges associated with the design of a boost converter for harvesting thermal energy from body-heat using a TEG are low-voltage cold-start and end-to-end power efficiency; a single-inductor, dual-path boost converter topology was adopted to meet these needs [24]. As shown in Fig. 5a, the converter uses an asynchronous start-up path comprising a low-side switch, M_{ST} , and a high-side PMOS diode, M_{D} . A charge-pump-based on-chip voltage multiplier boosts the TEG voltage during cold-start and provides power supply, V_{CP} to the start-up circuits for generating a one-shot. As the output of the multiplier ramps up to a voltage higher than $\sim 650\text{mV}$, the one-shot is asserted and it assists in charging the inductor through M_{ST} with sufficient energy required to start a secondary oscillator, CK . The falling edge of the one-shot triggers the asynchronous path to start boosting the input voltage. The intermediate boosted voltage V_{INT} , stored internally on a 200 pF capacitor, supplies power to the oscillator and to a low-power voltage supervisor circuit. The output power of the voltage multiplier and the duration of the triggering pulse are critical for the cold-start of the converter. Compared to the implementation in [24], in this work we have adopted a 20 stage charge pump with initial cross-coupled complementary stages for higher output power from the voltage multiplier [19]. In addition, the one-shot pulse-width is reduced for faster and efficient cold-start.

Once V_{INT} crosses a threshold (0.8 V), a secondary energy transfer path is enabled that operates synchronously to transfer power to a 1 μF output capacitor, C_{L} . The synchronous path is operated in discontinuous conduction mode (DCM) by synchronous control of the on-time of the high-side switch, M_{HS} , with the assistance of a digital zero current sensing (ZCS) circuit [25]. Both synchronous and asynchronous paths operate as time-multiplexed during start-up until the output DV_{DD} reaches 1 V. At this point, a power-on-reset circuit

(POR) shorts V_{INT} and DV_{DD} , and the start-up voltage multiplier and other cold-start circuits are disabled.

As the source resistance of the thermoelectric generator, R_{TEG} , is fixed, one-time tuning of the converter switching clock frequency is sufficient for maximum power point tracking (MPPT). In addition, a loss-optimized MPPT (LO-MPPT) technique was implemented to enhance end-to-end efficiency and available output power [24]. The core clock frequency of the switching converter, CK can be tuned during power-on by controlling programmable bits to take care of any static variation of the source resistance. The voltage supervisor finally regulates DV_{DD} by means of an on-off hysteretic regulation approach utilizing two on-chip reference voltages [26]. The single-inductor topology of the boost converter with integrated cold-start helps achieve both low-voltage start-up and sufficient output power at low input voltages, without requiring additional off-chip components.

B. Linear regulator for analog circuits

The boosted power supply DV_{DD} (1.5 V) generated by the DC-DC converter has significant voltage ripple (~ 100 mV) due to the hysteretic voltage regulation scheme. A clean supply, AV_{DD} (1.2 V), is generated using a downstream low drop-out (LDO) regulator to power the AFE circuits for pre-processing of the ECG signal. The LDO is designed for high power supply rejection ratio (PSRR) between the input DV_{DD} , and the output, AV_{DD} . Shown in Fig. 5b, a flipped voltage follower LDO with a dominant output pole was designed to achieve a high PSRR [27]. The internal gate poles are moved to higher frequencies by a buffer impedance attenuation technique using local negative feedback.

The regulated value of AV_{DD} is set by biasing the gate of the source follower transistor, M_S , using a single-ended op-amp and reference voltage, V_{BGR} , generated by an embedded low-power bandgap circuit [28]. The PSRR of the LDO is further improved by the op-amp. Instead of biasing the op-amp and bandgap reference directly by the input supply, DV_{DD} , self-regulated biasing is used, where the output of the LDO, AV_{DD} , itself biases the control, reducing noise injection into the LDO from DV_{DD} . The bandgap reference and regulator consume a total quiescent current of 150 nA. A 10 nA core current source, generated by a β -multiplier reference circuit provides current biasing of the LDO. It should be noted that start-up of the LDO is critical for the operation of the whole PMU and is taken care of by a dedicated start-up circuit for the current source generation.

V. Signal conditioning and heartbeat detection

The heartbeat detection circuits outlined in Fig. 1 include: front-end analog circuits for bioelectrical signal acquisition and pre-processing; PWLLs and digital circuits for motion-adaptive heartbeat detection; and, a wireless transmitter for near-field transmission.

A. Analog front-end circuits

The AFE comprises an instrumental amplifier (IA), a differentiator, and a passive switched-capacitor low pass filter. For target heartbeat detection application, pulse-width tracking based adaptive thresholding has relaxed the design requirements for the front-end IA in terms of noise and linearity. As shown in Fig. 6, a fully-differential capacitive-coupled IA is

adopted [29]. The IA provides a closed-loop gain of 40 dB, and transistor-based pseudo-resistors provide a DC path for the feedback loop. A two-stage operational transconductance amplifier (OTA) topology is adopted to provide sufficient DC gain and output swing. The first stage is realized by a self-biased current-reused topology [30] that employs both NMOS and PMOS to enhance noise efficiency. The second stage is a common-source amplifier with resistor-based common-mode feedback (CMFB) to determine the output common-mode (CM) voltage. Resistance of the CMFB resistor, also implemented using a pseudo-resistor, is large enough to limit impact on the gain. As the IA output is AC-coupled to the second stage differentiator, slight variation of output CM voltage is acceptable as long as output swing is not affected. The two-stage OTA is frequency-compensated using a Miller capacitor in series with a nulling resistor. Each OTA stage is biased at 20nA, 50nA in total including biasing circuits. The input NMOS and PMOS transistors are sized respectively as 20u/8u and 40u/8u to reduce flicker noise with $4.6 \mu V_{\text{rms}}$ input referred noise voltage integrating from 1 Hz to 1 kHz.

The output of the IA routes to a differentiator. As shown in Fig. 7, the differentiator is implemented using a capacitive-gain amplifier; a duty-cycled resistor in parallel with the feedback capacitor forms a high-pass cut-off frequency. This block serves three functional roles. First, it shapes the amplified ECG output of IA to create a differentiated ECG waveform with double-sided peaks corresponding to each QRS. In order to achieve the needed ~ 10 Hz high pass cut-off frequency, a duty-cycled resistor ($>100 \text{ G}\Omega$) is used. The clock for the resistor, CK_D , is generated utilizing the AFE core clock, CLK , and the duty-cycle of CK_D can be programmed by controlling a 4-bit capacitor bank as shown in Fig. 7 to provide a cut-off frequency range of 4-30 Hz. Second, the differentiator provides variable mid-band gain from 20-28 dB, controlled by 2-bit variable input capacitor C_I . Third, differential to single-ended conversion occurs and defines the common mode voltage $V_{\text{CM}} = 0.6 \text{ V}$. A symmetric OTA is used in the differentiator to maximize matching and output swing. The output branch is biased at 100 nA to provide sufficient output drive.

Following the differentiator, a first-order switched-capacitor low-pass filter with a gain of 2 (Fig. 8) is used. It provides a ~ 20 dB attenuation to the residual 50/60 Hz line noise in the differentiated ECG signal, V_{ECGD} . The fully-passive realization introduces no non-linearity and improves over active circuits for rail-to-rail operation, supply noise, and static power. Load capacitor C_2 is adjustable from 1-8 pF to achieve variable low-pass cut-off frequency.

A 1 kHz clock is generated on-chip using a low-power oscillator [31] and serves as the core clock, CLK for the AFE and heartbeat detection circuits. In the AFE, the clock is used for duty-cycled resistance generation and the switched-capacitor operation of the low-pass filter as described above. Low frequency nature of the ECG signal relaxes the requirement of a fast clock as well as the corresponding routing complexities.

B. Double-sided adaptive threshold generation

Shown in Fig. 9, adaptive reference tracking for positive and negative peaks of V_{ECGD} was implemented using two independent pulse-width locked loops (PWLL_H and PWLL_L), which operates similarly to a phase-locked loop. A clocked comparator operated by CLK , generates output signal (V_{CMPH} and V_{CMPL}), whose pulse-width, T_{PW} denotes the period

when V_{ECGD} is above (for positive peak) or below (for negative peak) the present reference voltages (V_{REFH} and V_{REFL}). The rising edge of comparator output triggers a one-shot (PW_{REFH} and PW_{REFL}) with a fixed predefined pulse-width, T_{REF} . The pulses are generated on-chip by individual timer blocks operated by CLK , and the pulse-widths can be independently programmed using 6-bit controls (P_H and P_L). The two pulses, PW and PW_{REF} are compared by a conventional phase frequency detector (PFD) in either side. The corresponding error pulse is stored in a pulse delay block and synchronized for both reference loops, which serves two purposes:

First, the detection logic identifies a true heartbeat signal only when dual-sided peaks are observed in the differentiated ECG signal. In this case, the reference voltage will be adjusted to track the baseline. Detection of a sole positive or negative peak is classified as an artifact, and the reference is not altered.

Second, as the QRS duration is long (~ 100 ms), adjusting V_{REF} immediately may cause secondary comparator triggering. A pulse delay block is utilized to first quantize the pulse width error using the 1 kHz core clock, CLK , and the result is stored in a register. Once the heartbeat flag signal, HB is asserted, indicating a detected heartbeat, the pulse delay block recreates the error pulse to steer the charge pump. As the QRS period is well-defined, an internal timer is used for timeout; if the interval between an error pulse and a HB signal exceeds a pre-defined expiration time, the register is reset to avoid false detection.

As described by (3), the reference tracking loop dynamics are controlled by the design parameters T_{REF} and K . T_0 is set at 50 ms, which is half of the nominal QRS duration; $V_{\text{PK,dc}}$ is chosen as 0.6 V for maximum input amplitude; K is determined by convergence requirement (3),

$$K = \frac{I_{\text{CP}}}{C_{\text{VREF}}} < \frac{V_{\text{PK,dc}}}{T_0} \quad (4)$$

where I_{CP} is the charge pump current and C_{VREF} is the storage capacitor for V_{REF} . In this work, I_{CP} is designed as 500 pA, and C_{VREF} is implemented as an adjustable capacitor bank providing 30-50 pF to control K . Transistors used in the charge pump are all selected as thick-oxide devices to minimize leakage of V_{REF} during intervals between successive heartbeats. The reference pulse width T_{REF} ($n \times T_{\text{CLK}}$) can be programmed externally by a 6-bit register up to 64 ms with the 1 kHz clock to freely position the reference voltage. The given programmability also accommodates $\pm 10\%$ variations of on-chip clock (CLK) frequency due to process corners.

C. Voltage reference at start-up and boundary conditions

As discussed in Sec. III, the reference tracking loop is conditionally stable for an arbitrary input signal. Therefore, a reference reset scheme and a stable initial reference voltage are essential if V_{REF} is likely to be out of range. Fig. 9 shows the circuit implementation of the V_{REF} boundary and startup control. Internally generated reference voltages provide the initial V_{REFH} and V_{REFL} following a reset. Due to the adaptive reference loop, the initial reference voltage need not be precise or PVT invariant. A leakage-based voltage reference

was implemented where the high and low initialization reference voltages were designed as 900 mV and 300 mV, respectively. A comparator placed in each PWLL monitors V_{REFH} and V_{REFL} to reset V_{REF} if $V_{REFH} < AV_{DD}/2$ or $V_{REFL} > AV_{DD}/2$.

D. Heartbeat Detection and Transmission

The heartbeat detection logic is designed as a finite state machine, illustrated in Fig. 10. Four states {Idle, DEHI, WALO, DELO} represent idle state, positive peak detected, waiting for negative peak, and negative peak detected, respectively. The DELO state also indicates a validated heartbeat detection, which triggers a one-shot pulse signal, HB , with a pulse width of one clock period. An internal timeout ensures the detector will not indefinitely wait for the negative peak detecting comparator output during WALO, guaranteeing that a previous false triggering of the positive peak detecting comparator will not impact the future detections. The positive and negative peak detection sequence leverages the structure of the QRS complex, where the slope is always positive and then negative, providing a robust double-sided heartbeat detection in the presences of noise and artifacts. Note that the proposed detection scheme will have a delay of multiple clock cycles ($n \times 1$ ms) between the actual QRS and the HB pulse. In addition, the delay will vary from beat to beat based on the current position of V_{REFL} relative to the negative peak of V_{ECGD} , resulting in a variation of the R-R interval. While this may limit utility for clinical R-R variation assessment, it will have negligible impact for heart rate related applications. In addition, the variation will be less due to the slow tracking bandwidth of the algorithm and the error will be averaged out in long-term heart rate measurement.

The HB signal is also used for wireless transmission of the detected heartbeat pulse. As shown in Fig. 1, the digital HB output OOK modulates a 13.56 MHz clock, which is generated on chip using a ring-oscillator and an AND gate. A high-efficiency inverter-based power amplifier transmits HB to an off-chip external matching circuit and NFC antenna. A differential path is chosen for better transfer of the PA power to the antenna. The transmitter is powered by the DV_{DD} supply, using only harvested energy.

VI. Measurements

A prototype of the SoC was implemented in a 0.18 μm silicon CMOS process, with a total area of 2.5 mm $\times$ 2.5 mm; an annotated die micrograph is shown in Fig. 11. The chip is tested in various forms for multiple purpose. Chip-on-board packaging was used for primary electrical characterization, the chip was also packaged in a quad-flat no-lead (QFN) package to demonstrate the body-heat powered SoC in a wearable form-factor, as shown in Fig. 11. An off-chip 100 μH inductor was used for the voltage boosting power converter.

To measure the minimum TEG voltage required to start up the system, a bench-top power supply with a 5 Ω series resistance was used to replicate a typical thermoelectric generator. Measurement results in Fig. 12 show battery-less cold-start of the system with a V_{TEG} of 60 mV. The boosted, regulated output supply, DV_{DD} , reaches a voltage of 1.5 V within 100 ms from cold start. The voltage ripple on DV_{DD} is due to hysteretic voltage regulation using on-chip voltage references. The further regulated voltage supply, AV_{DD} , is provided by the downstream LDO and ramps up slowly to 1.2 V using a soft-start circuit. The delay between

the DV_{DD} and AV_{DD} in the power sequence is used to reset digital circuits prior to the settling of the V_{ECGD} .

The AFE output, V_{ECGD} , and adaptive reference voltages, V_{REFH} and V_{REFL} , are buffered to output pads through independently supplied on-chip voltage followers for testing purposes. Initial values of V_{REFH} and V_{REFL} are shown as measured transient signals in Fig. 13 and settle before the common-mode stabilization of V_{ECGD} .

V_{ECGD} stabilizes after ~ 4 s following the start-up of the harvester power supply, DV_{DD} . The delay is due to the settling time of the low-power IA, which uses high resistance common-mode feedback for setting the DC operating point. This settling time does not impact the performance of the heartbeat detection; once the AFE provides a stable V_{ECGD} output, the adaptive references begin tracking the baseline and assist in motion-resilient heartbeat detection. Measured AC response of the AFE is shown in Fig. 14 at a particular set of cut-off frequencies of the differentiator and the low-pass filter. With the complete set of control bits a passband range of 4-28 Hz is achieved.

To evaluate the performance of the motion-adaptive heartbeat detection SoC, a two-electrode ECG measurement was performed using gel electrodes. The body of the subject was grounded to reduce the common mode interference due to power line coupling. The primary test outputs, V_{ECGD} , V_{REFH} , and V_{REFL} , were recorded over various movement conditions. As illustrated in Fig. 15a, as a person starts moving from seated position to walking, stretching, and running, the V_{ECGD} peaks and baseline are highly variable. The variation of these peaks in either direction corresponds to baseline shift of the QRS peaks of the ECG signal. Evident from this measurement, the presented threshold generation algorithm sufficiently tracks the peak variation with changing motion and adapts the threshold voltages for proper detection of the heartbeats.

In order to compare the performance of the presented double-sided adaptive threshold scheme against that of a fixed threshold approach for detecting heartbeats, the amplified ECG signal at the output of the IA was measured in parallel with HB output from the SoC. True heartbeats, plotted as gray bars in Fig. 16, were decoded from the recorded IA output using standard heartbeat detection algorithms in MATLAB and is verified manually. In order to show the effect of a fixed threshold based heartbeat detection in ambulatory conditions the IA output was post-processed in MATLAB for removal of mains interference and unwanted high frequency noises. A peak detection algorithm with a fixed threshold (based on the average QRS peak height) was run to detect heartbeats, depicted by the blue bars in Fig. 16. HB pulses from the SoC were counted to calculate detected heartbeats by the proposed double-sided adaptive threshold based comparison shown by the red bars in Fig. 16.

On comparing the heartbeats detected by the SoC and the fixed- V_{REF} method with true heartbeat events, it is observed that while both the approaches provide accurate detection in static, seated conditions, the error in detection of heartbeats by the fixed- V_{REF} method increases as the subject starts moving. It should be noted that a positive error is encountered when an artifact is detected as a false heartbeat and a negative error happens when a true heartbeat is not detected as the QRS peak falls below the threshold. As evident from Fig. 16,

the absolute error in heartbeat detection by a fixed- V_{REF} method increases as the person starts moving whereas, detected heartbeats from the prototype SoC has significantly less error, thanks to the double-sided adaptive threshold generation scheme.

A key feature of the implemented SoC is its low continuous power consumption that makes it suitable for powering from harvested energy from body heat, without the assistance of a battery. The AFE consumes a total average power of 504 nW, most of which is consumed by the biasing currents of the amplifier and the on-chip bias current source. The digital back-end, including adaptive double-sided threshold generation and heartbeat detection logic, consumes approximately 92 nW.

Compared to the signal processing circuits, a large proportion of the quiescent power is consumed by the RF transmitter, which sets the minimum power required for continuous, battery-less operation of the SoC. The local oscillator in the transmitter generates a clock of approximately 8.5 MHz and is always on, with an average power consumption of 4.2 μ W. The power amplifier that transmits the OOK signal modulated by the *HB* pulses to an external NFC antenna is turned on only when the heart beats occur, as shown in Fig. 17 and consumes power only in burst mode. The minimum power required for the operation of the PA during the burst mode is 5.9 μ W. The average power consumption of the PA is tens of nanowatts due to the low duty cycle (<1 ms/0.5) of the heartbeat pulses and is negligible compared to the power consumption of other blocks; however, for complete operation of the system, the power amplifier needs instantaneous power during *HB* bursts, and the SoC requires a minimum power of 10.5 μ W. It is important to note here that although a carrier frequency in the NFC band is chosen to demonstrate wireless transmission, the implemented transmitter is not standards compliant and serves primarily as a system-level proof of principle for a fully battery-less, wireless sensor system. An energy-optimized, duty-cycled transmitter for BLE or similar longer-range modalities is a possible future research direction.

Overall, the minimum power required from the TEG source for the operation of the SoC is determined by the end-to-end efficiency of the harvester and the minimum power required for the detection and transmission of heartbeats. This limits the operation of the SoC to a TEG voltage of 20 mV. At this voltage, the TEG provides an input power of 20 μ W, of which 9.5 μ W is lost in the conduction and control circuits of the power converter; the remaining power is available for the operation of the SoC. This minimum voltage operation of the SoC corresponds to a temperature difference of ~ 0.5 $^{\circ}$ C across the TEG plates, making it suitable for powering the SoC purely by body heat. The power distribution of the SoC at this minimum input voltage is shown in Fig. 17.

The performance of the implemented SoC is compared against state-of-the-art energy harvesting SoCs presented in recent literature in Table I. The low-power, low-voltage operation of the SoC enables a completely battery-less system powered by a portable thermoelectric generator using body heat, with minimal additional off-chip components.

VII. Conclusion

A low-power, motion-adaptive heartbeat detection system is presented, which demonstrates a fully battery-less, autonomous wearable sensor system-on-chip powered by human body heat. Slow and fast motion artifact rejection is provided by double-sided comparison of the differentiated ECG output against adaptive threshold voltages generated using a pulse-width locked loop; this approach enables the system to measure heartbeats accurately in ambulatory conditions.

In addition, efficient operation and low voltage cold-start of an integrated DC-DC boost converter makes the TEG-based energy harvester self-sufficient, operating continuously without batteries and without duty-cycled operation. A small number of required off-chip components and compact packaging showcases the applicability of the designed SoC for body-worn devices. Overall, the presented approach demonstrates the potential of low-power sensing and intelligent processing in the context of energy harvesting constraints to realize sustainable, continuous health monitoring.

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Fig. 1. Motion-resilient heartbeat detection SoC architecture powered by body heat using a self-starting thermoelectric energy harvester.

Fig. 2. ECG waveform (data taken from MIT-BIH database [21]) subject to motion artifacts results in missed heartbeats.

Fig. 3.

The QRS pulse width is used to track baseline drift, where a measured pulse width, $T_{\text{PW}}(n)$ is compared against a set reference pulse width, T_{REF} .

(a)

(b)

Fig. 4.

Fast motion artifacts are detected using a differentiated ECG signal to identify artifacts as distinct from heartbeats.

Fig. 5.

(a) Single-inductor self-starting boost converter architecture for autonomous thermoelectric energy harvesting [24], and (b) downstream low-power LDO with bandgap reference.

Fig. 6.
Front-end instrumentation amplifier used for ECG signal acquisition.

Fig. 7.
Differentiator circuit to create bipolar peaks corresponding to QRS complex in the ECG signal.

Fig. 8.

Fully-passive switched capacitor low-pass filter for mains (50 Hz/60 Hz) rejection.

Fig. 9. Adaptive threshold generation using a PWLL-based architecture and double-sided comparison of V_{ECGD} signal for heartbeat detection.

Fig. 10.

State machine definition for the heartbeat detection logic, which validates heartbeats and rejects artifacts by observing dual-sided pulses.

Fig. 11.

Die photo of the SoC fabricated in 0.18 μm CMOS technology. The die is packaged in a QFN and is used to demonstrate a wearable form-factor.

Fig. 12.

Measured transient showing start-up sequence of the output power supplies, as well as on/off regulation and MPPT.

Fig. 13.

Initialization and settling of V_{REFH} and V_{REFL} during start-up; once the AFE is operational, initial V_{REF} adapts to the V_{ECGD} signal baseline.

Fig. 14.

Measured AC response of the AFE channel for a set of duty-cycled resistor and capacitor values (configurable with control bits).

Fig. 15.

(a) Measured continuous transient outputs of the SoC showing dynamic behaviors of V_{REFH} and V_{REFL} adapting with the variation of the V_{ECGD} at different moving conditions of the subject, and (b) short duration transient plots showing heartbeat detection by a fixed-threshold-based ECG signal comparison (top), and by the proposed adaptive-threshold-based double-sided comparison of differentiated ECG signal (bottom).

Fig. 16.

Measured accuracy of heartbeat detection with the proposed adaptive- V_{REF} technique and comparison with a fixed- V_{REF} technique.

Fig. 17.

(a) Illustration of instantaneous burst power and average power of the SoC, and (b) measured distribution of the harvested power and utilization of the extracted power (marked with the dotted arrow) by the SoC.

TABLE I

Performance comparison with similar SoCs

References		This work	JSSC'13 [8]	JSSC'15 [14]	TBCAS'15 [17]	JSSC'10 [15]	JSSC'15 [9]
SoC Features	Technology	0.18 μm	0.13 μm	0.18 μm	0.13 μm	0.18 μm	65 nm
	Supply Voltage	1.2 V(Analog) 1.5 V(Digital)	0.3-1.2 V	1-1.8 V	<1.4 V	1.8 V	0.6/0.4 V
	ADC-less	Yes	No	No	No	No	No
	Total Power Consumption	4.6 μW	19 μW	24 μW	6.45 $\mu\text{W}^{(2)}$	12 μW	64 nW
AFE	Input Signal	ECG	ECG/EMG/EEG	EMG	ECG/EMG/EEG	ECG	ECG
	Noise	4.6 μV_{rms} (1-1000 Hz)	<2 μV_{rms}	<4 μV_{rms} (4-1000 Hz)	-	0.51 μV_{rms} (0.5-100 Hz)	6.52 μV_{rms}
	Gain	66-74 dB	40-78 dB	43-58 dB	-	46-60 dB	51-96 dB
	Power	504 nW	4 μA	7.5 μW	2 μW	-	19 nW
Digital	Function	HB Detection	R-R/ AFib/ENV Detection	TDMA Control	R-R/AFib Detection/FFT/ Filter	-	Arrhythmia Detection
	Processor-less	Yes	No	Yes	No	-	No
	Clock Frequency	1 kHz	2 kHz-1.7 MHz	500 kHz	187.5-500 kHz	-	10 kHz
	Power	92 nW	2.1 μW	4.2 μA	2.27 μW	-	45 nW
PMU	Harvesting Source	Body heat	Thermal/Rf	RF	TEG/Solar	RF	-
	Bulky Off-chip Components	1 inductor	-	1 supercapacitor	2 inductors 1 supercapacitor	12x4 inductors	-
	Start-up Voltage	55 mV	600 mV	-	220 mV	-	-
	Start-up Time	80 ms	7 s	-	-	-	-
	Input boost Voltage	9.4 mV	30 mV	0.8 V	10 mV	0 dbm	-
	Power Efficiency	80%	35%	64% ⁽¹⁾	74.9%	54.9% ⁽³⁾	-

⁽¹⁾ Boost efficiency⁽²⁾ Digital + radio power⁽³⁾ Rectifier efficiency.