Published in final edited form as:

Conf Proc IEEE Eng Med Biol Soc. 2019 July ; 2019: 5125–5128. doi:10.1109/EMBC.2019.8857171.

Recessed Traces for Planarized Passivation of Chronic Neural Microelectrodes

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Abstract

Implantable microfabricated neural electrodes have numerous neuroscientific research and clinical applications. However, these devices are prone to failure after several months *in vivo*. One mechanism is failure of passivation layers followed by corrosion of metal traces in the saline environment. It has been suggested that mechanical stress accelerates passivation layer failure and that stress is concentrated whenever passivation layers have a non-planar topography. Therefore, we developed a simple process for recessing metal traces within the substrate so that overlying passivation layers are planar. The process requires no extra masks and no post-passivation planarization steps.

I. Introduction

Neural electrode arrays record or send signals directly into the nervous system for neuroscientific research and therapeutic purposes. Tens of thousands of patients have benefitted from deep brain stimulation for Parkinson's disease [1] and cochlear implants for hearing loss [2, 3]. More recently, microfabrication technology has enabled batch processing of smaller, more sophisticated devices such as Blackrock microelectrode arrays used in neuroprosthetic clinical trials [4, 5] and planar silicon electrodes used in animal research [6–9]. Unfortunately, these devices often fail within months of implantation [10–12].

Several co-contributing failure modes appear to be responsible [10, 13–15]. Among these, ingress of moisture through pinholes and fractures in passivation layers has been reported [12, 14–17]. Degradation of passivation can expose too much of the electrode sites [14, 15], cause the electrode metal to detach [18], or create short-circuits with the traces [16, 19]. Various polymers [14–17, 19] and ceramics [12, 18] have been tried but all are vulnerable to degradation.

One largely overlooked aspect in these studies is the effect of mechanical stress. Typically, passivation layers must conform to the uneven topography of metal traces and electrode sites. To address this, one group fabricated devices where the traces were recessed (or buried) within the substrate, allowing the overlying passivation layers to be planar, and found that such devices had significantly improved longevity [20]. They theorized that the

planarized passivation layers had fewer stress concentration areas and were therefore less susceptible to stress corrosion cracking.

Another group examined planar silicon electrodes after 4–6 months *in vivo* and found that the traces corroded most quickly near the electrode sites [12]. Finite-element modeling revealed that these were areas of greatest mechanical stress, lending further credence to the idea that reducing stress concentrations could improve device longevity.

In this work, we developed a simple fabrication technique for achieving recessed traces. The technique involves reactive ion etching (RIE) immediately before deposition of metal traces. Since the processes are done back-to-back, the metal is self-aligned in the trenches, and no additional masks are necessary. By controlling the etch and deposition times, the recessed traces can be made flush with the wafer surface within about 10 nm, allowing overlying passivation layers to have planar topography. This technique may be applied to any process where planarization is desired without chemical-mechanical polishing.

II. Methods

A. Overview

Fig. 1 shows an overview of the processes. First, photoresist is patterned. Then, for recessed traces only, RIE is performed. Metal is deposited by electron beam evaporation then lifted off in acetone. Residues are cleaned, then passivation layers are deposited by plasma-enhanced chemical vapor deposition (PECVD). While non-recessed traces result in raised features in the overlying passivation layers, recessed traces are flush with the surface of the wafer so that overlying passivation layers are planar. Fabrication was performed at the University of Connecticut, Storrs, CT, USA and the Center for Nanoscale Systems at Harvard University, Cambridge, MA, USA.

B. Wafers and Photolithography

AZ 5214E-IR (Merck, Darmstadt, Germany) photoresist was spun onto 4" polished silicon wafers with 1 μm wet-grown thermal oxide (Ultrasil, Hayward, CA, USA). Image reversal lithography was used to pattern the trace metal layer of a layout for silicon-based cochlear nucleus probes [8]. Traces were 10 μm wide with 10 μm pitch, narrowing to 5 μm on curves and widening to 40 μm near the bond pads. After hardbaking, the photoresist was typically 1.5 μm thick with 1 μm undercut.

C. Reactive Ion Etch

Three different inductively-coupled plasma (ICP) RIE processes were compared. The first was a CHF₃-based oxide etch with added CF₄, H₂, and Ar. The second was a modified version of the first with increased pressure, decreased bias, and increased H₂ for reduced anisotropy. The third was designed for high anisotropy using Ar, C₃F₈, low pressure, and high bias power. The etch rate was characterized beforehand so samples could be etched to the desired depth (400 nm) in one step.

D. Metal Deposition

30 nm titanium, 20 nm platinum, 300 nm gold, then 50 nm titanium were deposited at a rate of 1.0, 1.5, 2.0 and 1.0 Å/s, respectively, using a Denton electron beam evaporator pumped below 2×10^{-6} Torr. Samples were positioned in the center of the chamber, perpendicular to the source, at a throw distance of about 50 cm, with substrate rotation turned on.

E. Lift-off and Cleaning

To lift off metal, samples were immersed in acetone for at least 1.5 h, gently swabbed, moved to fresh acetone, sonicated for 5 min, then rinsed with isopropanol and water. Then, samples were etched for 5 min in an oxygen plasma barrel asher at 150 W. After that, an optional argon ICP RIE was used to reduce the size of metal “fences.” Less than 30 min before passivation, a modified RCA clean was performed by dipping samples into a solution of 100 ml water, 20 ml ammonium hydroxide, and 20 ml hydrogen peroxide for 5 s then rinsing with water.

F. Passivation

Passivation layers were deposited in a parallel electrode PECVD reactor. Eight layers were deposited in the order NONONONO, where N is silicon nitride and O is silicon oxide, with total thickness 1.85 μm .

G. Characterization

Scanning electron microscopy (SEM) images were taken in secondary electron mode with 2–5 kV accelerating voltage. Focused ion beam milling was performed using a ZEISS Crossbeam with gallium ion source. Heights of features were measured using a profilometer. Finished devices (with 55×37 or 110×37 μm sputtered iridium electrode sites) were epoxied and wire-bonded to custom printed circuit boards. AC impedance measurements were obtained with a ZIVE MP2 electrochemical workstation (WonATech, Seoul, South Korea) using room-temperature phosphate buffered saline (PBS) (pH 7.4), an Ag/AgCl reference electrode, a large stainless steel counter electrode, and 10 mV peak-to-peak sinusoids at 1 kHz.

III. Results

A. Reactive Ion Etch

Fig. 2 shows SEM images of the samples following reactive ion etching. All three etch recipes were able to etch a 400 nm trench in the silicon oxide while still preserving some of the photoresist’s undercut. Recipe 1 had an etch rate of 195 nm/min, 2:1 selectivity vs. photoresist, and a sidewall profile of about 85°. Recipe 2, designed for decreased anisotropy, had an etch rate of 64 nm/min, 3:1 selectivity vs. photoresist, and a sigmoidal sidewall profile that undercut the resist more than the other recipes. Recipe 3, designed for maximal anisotropy, had an etch rate of 410 nm/min, 2:1 selectivity vs. photoresist, and a sidewall profile near 90°.

B. Cleaning (Oxygen)

After lift-off, we discovered that acetone and sonication were insufficient to remove polymer residues that appeared in thin bands alongside the traces (Fig. 3). Longer soaks, longer sonication, and Remover PG (MicroChem, Westborough, MA, USA) were unable to remove these residues, however oxygen plasma succeeded. Removing these residues was critical because otherwise the passivation layers formed raised bumps over the residues.

C. Cleaning (Argon)

We observed small, sharp metal “fences” along the edges of some traces. The fences were direction-dependent. In the center of the wafer there were no fences. Towards the left edge, however, there would be fences along the left edge; towards the top, the top, and so on. The fences were more prominent when RIE Recipe 1 had been used. Recipe 2 had less prominent fences, but left a wide gap between metal trace and silicon oxide. Recipe 3 had less prominent fences and the smallest gap so was chosen as the preferred recipe. To improve yield near the edges of the wafer, an argon etch was used. 80 s of etching was sufficient to reduce the size of the fences without excessively widening the gap between trace and sidewall. When incorporating this step, an extra 10–15 nm was budgeted into the depth of the initial RIE trench to anticipate the difference in etch rates of silicon oxide and metal during argon etching.

D. Passivation

After passivation, non-recessed traces were easily visible on SEM due to the steeply-sloped areas on either side of the trace where the passivation layers curved up over them (Fig. 4). The sloped areas appear bright on SEM due to topography, not composition. Recessed traces, meanwhile, were difficult to locate because their topography was nearly planar. Nevertheless, it was possible to find a small valley along the edges of the traces. Next, focused ion beam milling was used to examine the internal structure of a recessed, passivated trace (Fig. 5). We observed a small keyhole directly above the gap between trace metal and silicon oxide sidewall, but no cracks in the passivation layers.

E. Characterization

Profilometry revealed that after etch and deposition rates were properly characterized, recessed traces typically had a surface topography that was planar within about 10 nm.

To show that devices fabricated using this technique were functional, finished devices were attached to custom PCBs and DC continuity from the electrode sites to the PCB bond pads was verified in a saturated NaCl solution. Then, in PBS, AC impedances at 1 kHz were measured to be 127 ± 40 k Ω .

IV. Discussion

Overall, our simple technique was successful at creating recessed traces with planar topography, and did not create any issues in the functionality of finished devices. The AC impedances were in line with typical sputtered iridium microelectrodes of this size.

The success of Recipe 3 suggested that minimal undercut and a sidewall angle close to 90° was superior. Too much undercut, as in Recipe 2, resulted in too wide of a gap between metal and silicon oxide. Meanwhile, we speculate that the non-90° sidewall angle of Recipe 1 was responsible for its exacerbated fences by allowing some metal to deposit on the sidewalls.

Oxygen plasma cleaning was essential for removing polymer residues after lift-off. The chemical resilience of these residues suggests they may have been fluorocarbons or heavily-crosslinked polymers that formed during RIE.

Metal fences are the main area requiring improvement in this method. While the center had no fences, and argon etching reduced the size of the fences elsewhere, a 100% yield with no fences whatsoever would have been preferred. The direction-dependent nature of the fences strongly suggests that the fences were caused by the non-vertical deposition angle that occurs towards the edges of the wafer in the electron beam evaporator. Therefore, fences could be reduced if a deposition system with a longer throw distance was used, and conversely, fences would be increased if a sputter deposition system was used. Another option would be to use a brief isotropic wet etch to dissolve the fences, if the choice of metals allows.

The small gap between metal and sidewall is another area that could be improved. Even with minimal undercut and vertical sidewalls, the non-vertical edge of the metal created a V-shaped gap (Fig. 5). In theory, this gap could be eliminated by allowing metal to deposit onto appropriately-sloped sidewalls, but in practice, this would likely also exacerbate fences. A more facile approach might be to use conformal passivation techniques such as atomic layer deposition, chemical vapor deposition (e.g. Parylene), or spinning (e.g. polyimide or spin-on glass) in place of or in combination with PECVD. Annealing might further improve gap filling.

The next step will be to determine whether recessed traces with planar passivation resist degradation better than non-recessed traces with non-planar passivation. If the difference is substantial, our technique represents a simple technique to improve the longevity of neural electrodes that could be added into virtually any planar silicon microelectrode fabrication process [6–9]. For very thin electrodes, one could even use this technique to position traces in the center (vertically) of the electrode, which would reduce mechanical stresses due to dissimilar materials, as suggested in [12]. Outside the field of neural electrodes, our method could also be used in situations where planarization is desired but the cost and complexity of chemical mechanical polishing is prohibitive [21].

Acknowledgment

We would like to thank Joseph Favata and Sina Shahbazmohamadi at the University of Connecticut for performing FIB analysis, Helena Silva at the University of Connecticut for sharing her cleanroom facilities, and Ling Xie and Kenlin Huang at the Center for Nanoscale Systems at Harvard University for helping design the RIE recipes.

Research supported by NIH grants R01DC014044 and R24NS086603 (MH).

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Figure 1.

Overview of the process: (1) photolithography, (2) reactive ion etching, (3) deposition of metal by electron beam evaporation, (4) lift-off and cleaning, (5) deposition of passivation layers. The recessed process seeks to avoid creating any curved, stress-concentrating areas.

Figure 2.

SEM images of the three different etching recipes. The material on top is photoresist and the smoother material below it is the silicon oxide which has had a trench etched into it.

Figure 3.

(A) SEM image of polymer residues remaining along the edges of the traces. (B) Edge of a trace after oxygen plasma cleaning has removed the residues.

Figure 4. SEM images of non-recessed (A, C, E) and recessed (B, D, F) traces after passivation. (A, B) The steeply-sloped edges of non-recessed traces are easily visible, while recessed traces have almost no topography and are nearly invisible without greatly boosting contrast. (C, D) Close-up. (E, F) High magnification at the edge of a trace. The only topography in the recessed trace is a small valley caused by the gap between trace metal and trench sidewall.

Figure 5.

Focused ion beam cross-section of a recessed trace. In the center of the image, between the metal and the silicon oxide sidewall, a small keyhole can be seen. There do not appear to be any cracks in the passivation layers.