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Tunable and Lightweight On-Chip Event Detection for Implantable Bladder Pressure Monitoring Devices

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Abstract

Lower urinary tract dysfunctions, such as urinary incontinence and overactive bladder, are conditions that greatly affect the quality of life for millions of individuals worldwide. For those with more complex pathophysiologies, diagnosis of these conditions often requires a urodynamics study, providing physicians with a snapshot view of bladder mechanics. Recent advancements in implantable bladder pressure monitors and advanced data analysis techniques have made diagnosis through chronic monitoring a promising prospect. However, implants targeted at treatment must remain in the bladder for long periods of time, making minimizing power consumption a primary design objective. Currently, much of the typical implant's power draw is due to data transmission. Previous work has demonstrated an adaptive rate transmission technique to reduce power consumption. However, the ultimate reduction in power consumption can only be attained when the device does not transmit bladder pressure samples, but rather *bladder events*. In this paper, we present an algorithm and circuit level implementation for on-chip bladder pressure data compression and event detection. It is designed to be a complete, tunable, and lightweight diagnosis and treatment framework for bladder pressure monitoring implants, capable of selectively transmitting compressed bladder pressure data with tunable quality, "snapshots" of significant bladder events, or simply indicate events occurred for the highest energy efficiency. The design aims to minimize area through resource reuse, leading to a total area of 1.75 mm², and

employs advanced VLSI techniques for power reduction. With compression and event detection enabled, the design consumes roughly 2.6 nW in TSMC 0.18 - μm technology. With only event detection, this reduces to 2.1 nW, making this approach ideal for long-life implantable bladder pressure monitoring devices.

Keywords

Biomedical implants; energy-efficiency; data compression; algorithms

I. INTRODUCTION

OVERACTIVE bladder and urinary incontinence are two examples of lower urinary tract dysfunctions, debilitating conditions which affect millions of individuals worldwide, imposing large financial burdens, and reducing the quality of life [1]. For individuals with more complex pathophysiologies, diagnosis of these conditions can be facilitated through the use of urodynamic testing, an acute procedure which involves filling the bladder with saline at super physiological rates, and monitoring bladder pressure, volume, and other metrics with respect to time. In some cases, the infusion of saline into the bladder at faster-than-physiological rates can produce results that may not be representative of bladder function during natural filling, which occurs at significantly lower rates. Meanwhile, the catheters used for infusion and pressure measurements can affect bladder activity, which can potentially confound results.

Ambulatory Urodynamics, a diagnostic test designed for observing bladder activity over longer periods of time with natural filling, has been demonstrated [2]. However, long-term usage of such ambulatory setups is impractical due to the wired nature of the sensors. Wireless, implantable pressure monitors can feasibly replace much of the equipment used in these studies, while enabling data collection over longer periods of time. A number of such devices have emerged to meet this need [3]–[9]. An example use case of such a device is shown in Fig. 1(a): an implanted pressure monitor, wirelessly charged and configured, transmits data to a custom device capable of receiving data from the implant and stimulating lower urinary tract nerves when required.

Minimizing power consumption is a common theme among bioimplantable devices, especially those aimed at chronic treatment applications, since higher power draw requires either larger batteries or more frequent recharges. Larger batteries are often not an option for such constrained environments, and requiring more frequent recharges can be cumbersome to end users when considering the typical inefficiency of wireless power transfer systems. To maintain a small implant size, reduce the frequency of recharges (as well as recharge cycles), and ensure long device lifetimes, device power consumption must be minimized.

For the device presented in [3], power consumption from transmission at 100 Hz sampling is roughly 90% of the total power draw (Fig. 1(b)). An efficient compression algorithm could enable devices to reduce transmission power. Ultimately, a vocabulary-based compression scheme in which the events themselves, or rather unique codes representing these events, are transmitted, rather than the raw or compressed signal data, can provide the most significant

reduction in transmission power requirements [11]. For human bladder pressure signals, deciding what events to transmit can be achieved using Context Aware Thresholding (CAT), an algorithm designed to autonomously discriminate between different bladder events in the presence of noise [12]. Closed-loop neural control of the bladder using CAT has been successfully demonstrated in a human subject [13], though the algorithm has not yet been implemented in hardware. In this paper, we present a novel algorithm and circuit architecture which enables an implanted device to seamlessly transition between one of three states, in which the device transmits:

- 1) compressed bladder pressure with tunable quality
- 2) a short window of compressed bladder pressure, but only when an event is determined to have occurred
- 3) only bladder events, represented by unique codes

These options provide physicians with a complete framework for both diagnosis and treatment of urinary incontinence and other lower urinary tract dysfunctions. Specifically, the first option outputs the most data, although this can be adjusted by setting the compression quality. It can therefore be used for the original diagnosis. The second option, which outputs a snapshot of the data when an event occurs, outputs significantly less data, and can be used to either confirm a diagnosis, or for troubleshooting; for example, if the device is overstimulating, it may be worthwhile to see what is considered an event, in case further algorithm tuning is required. The third option outputs the least amount of data, simply indicating to the stimulator what event has been detected. This is most useful for treatment, as only a few bits are needed to differentiate between different events.

In particular, this paper makes the following novel contributions:

- 1) We present a tunable, lossy compression algorithm which leverages the properties of human bladder pressure signals to perform effective data compression.
- 2) We incorporate decision making hardware which uses multiresolution analysis and adaptive thresholding to detect bladder events *in situ* and in real time.
- 3) We validate the approach using recorded bladder pressure data from 14 human subjects, and show that the algorithm can achieve high compression ratios with low reconstruction error when configured to transmit only pressure data, and can accurately classify bladder events in real time.
- 4) We provide hardware implementation details with optimizations for ultralow power consumption, as well as area and power results from synthesis and layout in TSMC 0.18 μm technology.

Having both compression and decision making hardware enables an implanted device to transmit either compressed data, compressed data and detected bladder events, or just the events, for the highest level of flexibility and reduced power consumption. Furthermore, significant portions of the circuitry are shared between the compression-only hardware and the decision making hardware, improving the area and energy efficiency of the implant. To

the best of our knowledge, this is the first example of a combined diagnosis/treatment implant for lower urinary tract dysfunction.

The rest of this paper is organized as follows: Section II gives a brief background on the properties of human bladder pressure which are used in the compression algorithm; Section III describes the compression algorithm design and flow; Section IV describes the event detection, designed to operate on compressed data; Section V provides an overview of the hardware implementation, synthesis and layout results, and a discussion on reducing power consumption for the implant device; finally, Section VI concludes with future directions for the research.

II. BACKGROUND AND MOTIVATION

Generally, changes in human bladder pressure during natural filling occur very slowly relative to modern electronic device speeds, as shown in Fig. 1(c). Even when filled super-physiologically at a rate of 100 mL/min in urodynamics studies, static bladder pressure typically rises slower than 4 cm H₂O/min. Bladder contractions are fast relative to storage pressure changes, occurring with a maximum pressure rate-of-change of 10 cm H₂O/s and typically lasting 1 to 30 seconds [14]. Motion artifacts superimposed on bladder pressures have higher frequency content, leading to recommended sample rates of 100 Hz to avoid aliasing effects.

Recent published works have demonstrated significant progress towards developing an effective bladder pressure sensor for chronic implantation [3]–[5], [15]–[17]. The primary goal for a chronic, implanted bladder pressure monitor is to provide feedback data on the bladder state with sufficient accuracy and low latency such that contractions may be distinguished and acted upon separately from motion artifacts. These sensors measure pressure directly, and so require post-processing to determine when a significant bladder event has occurred. Alternatively, monitoring neural activity in the lower urinary tract has shown promise in estimating bladder volume or predicting contractions [18]–[20], though such systems may not be ideal for chronic, ambulatory measurements, since mechanical stability of the neural interface is imperative for recording accuracy.

For the direct measure approach, thresholding is a common technique for predicting bladder events that is relatively low-cost. However, its efficacy outside of a clinical setting is limited, since superimposed motion artifacts necessitate measuring abdominal pressure as well. The development of Context Aware Thresholding (CAT) has shown that, with sufficient post-processing, it is feasible to discriminate between significant bladder events and the superimposed artifacts with bladder pressure only [12]. This has made direct measurements for single channel systems viable for providing feedback to a closed-loop stimulation system. Therefore, once a viable sensor is available, such a control algorithm can be used for treatment of lower urinary tract dysfunction.

In general, bladder pressure post processing has been performed off-chip using an external signal processor. This is logical for catheter-based measurement, which is the standard practice for clinical urodynamics; but in a future diagnosis and treatment system which relies

on wireless transmission of bladder pressure data, performing this post-processing *on-chip* has numerous added benefits, namely reducing wireless transmission power and bandwidth requirements.

This is attractive because data transmission from implantable medical devices consumes significant energy and is often the dominant power draw even in single-channel systems. For example, the device in [3] consumes 10x more energy when transmitting samples at 100 Hz than at 1.5 Hz (as shown in Fig. 1(b)). Prior strategies for minimizing data transmission in pressure monitors have implemented very low, sub-Hz sample rates or burst transmissions of pressure history; these strategies have long latency which prevents real-time closed-loop bladder control. We demonstrated that a sparse approach can be effective, wherein pressure data is adaptively transmitted to match the activity level in the pressure signal. By only transmitting “important” samples real-time, low-latency telemetry was maintained, and average transmission power was reduced by 96% with 1.5% average error [3]. The major drawback of the sparse transmission approach is that signal information is inherently lost when samples are not transmitted. This fundamentally prevents a faithful reconstruction, which may contain important diagnostic symbols for some patients. Pre-transmission compression can mitigate reconstruction errors, but requires silicon area and computation power draw on the implanted device. Modern VLSI technology combined with new circuit topologies, however, can manage this tradeoff by performing data compression in an efficient and lightweight manner suitable for implementation in an ultralow-power implant device.

III. COMPRESSION OF BLADDER PRESSURE DATA

Based on the properties of human bladder pressure data detailed in Section II, we note that the approximation of expected values within a limited sample window can serve as sufficient representations of bladder state for the majority of the recording period. Meanwhile, events like non-voiding or voiding contractions, or spikes in vesical pressure due to the contribution of the abdominal muscles, present as *unexpected* changes in bladder pressure, and therefore must be handled with greater attention to detail.

A. Algorithm Flow

In this context, we present an algorithm which leverages these properties to perform efficient compression of bladder pressure data (Fig. 2). Samples are first processed with a lightweight exponentially-weighted moving average (EWMA) [21], expressed by the recursive relation in (1).

$$S_t = \begin{cases} Y_t & t = 0 \\ \alpha Y_t + (1 - \alpha)S_{t-1} & t > 0 \end{cases} \quad (1)$$

Following this stage, we utilize a lifting scheme version of the Haar wavelet transform, which intrinsically meets the requirements for discriminating between periods of bladder filling and periods of bladder activity. Specifically, we employ a series of lifting stages, separating low frequency signal approximations from high frequency details [22]. Sample

data are split into even and odd elements, on which certain operations, namely the *predict* and *update* steps, are performed. These result in computation of successive even and odd elements in the transform space, as defined by (2) and (3).

$$odd_{j+1,i} = odd_{j,i} - even_{j,i} \quad (2)$$

$$even_{j+1,i} = even_{j,i} + \frac{odd_{j+1,i}}{2} \quad (3)$$

A total of n -bytes, where n is a power of two, are processed in a single lifting stage, which generates $n/2$ approximations, and $n/2$ details. Subsequent stages similarly reduce the time resolution by half. Furthermore, at each stage, a tunable threshold T_d applied coarsely to the odd (detail) coefficients of (2), determines which components are unexpected, and therefore should be retained in the final reconstruction. Coefficients which are below the threshold are stored as 0. This process tends to produce long runs of 0s (0-runs) in the resulting wavelet domain. Therefore, Run Length Encoding (RLE) is applied in the final processing stage. The encoder output is passed to the packet assembly, which first outputs the header data, containing the run lengths, followed by the corresponding values at each position.

With human bladder pressure data, we observed that one level of RLE tends to produce headers containing sequences of 1s (1-runs) interrupted by single instances greater than 1, corresponding to the 0-runs in the original data. Therefore, excepting rare cases in which the length of a 0-run is 1, it is possible to apply a second level of RLE on the header data itself, as shown in Fig. 3. In the rare case of a single element 0-run, we can judiciously insert a non-zero placeholder that is below the cutoff threshold, such that the second level of RLE can be consistently applied to further compress the data. An example of this 2-pass RLE is shown in Fig. 3.

B. Determination of T_d Range

Further analysis of the compression approach uncovers interesting properties for the average output size. Typically, thresholds below 3 do not produce 0-runs of sufficient length, which results in compressed representations that require more space than the original. We define the data compression ratio (DCR) as the ratio between compressed and uncompressed data sizes. For example, a 64 byte packet represented in 22 bytes yields a ratio of 22/64, or 34%. In the worst case, if no runs are found, the total size can be expressed as $2n + 1$: 1 byte for header length, the n -byte header array, and the n -byte values array, leading to a DCR of about 200%. Because the signal complexity for a given window is nondeterministic, success of the compression strategy is dependent on finding an appropriate range of values for T_d which provide a goodbalance between data size reduction and reconstruction error in the average case.

We determine this range empirically using a human cystometry dataset, which includes 64 recordings of vesical pressure from 14 human subjects sampled at 100 Hz and 8 bits per sample, with each recording lasting just over 8 minutes. An example recording is shown in

Fig. 1(c). Subjects had confirmed Neurogenic Detrusor Overactivity due to Spinal Cord Injury. Data were acquired at the L. Stokes Cleveland VA Medical Center using clinical urodynamics procedures as approved by their Institutional Review Board.

Taking the window size $n = 64$, this yields roughly 773 non-overlapping sample windows per recording, or approximately 50000 total samples windows in the dataset. Each of these sample windows was compressed with thresholds starting at $T_d = 0$, and compression ended once the percent decrease between subsequent output sizes fell below 0.1%. We observed that a minimum threshold of ± 4 ADC codes, up to a maximum of ± 14 ADC codes (with an 8 bit ADC), provided an appropriate thresholding range for the cystometry dataset. Below 4, resulting data were generally larger than the original, while above 14, the average output size stayed relatively constant. These values correspond to approximately $\pm 1.6\%$ to $\pm 5.5\%$ of the 8-bit ADC range.

Note that the value of threshold T_d is inversely proportional to the resulting compression ratio and directly proportional to reconstruction error. A high value of T_d will result in longer 0-runs at the cost of quality, whereas a low value has the inverse effect. Therefore, we define a single compression quality metric Q as

$$Q = \left\lfloor T_{max} \times 2^R \right\rfloor - T_d \quad (4)$$

where $T_{max} \approx 0.055$, R is the ADC resolution in bits, and T_d is the threshold value used to obtain a compressed signal with quality Q . This enables a user to specify a desired quality from 0 to 10, where 0 corresponds to low quality, high compression, and 10 corresponds to high quality, low compression. In practice, a Q value of 0 will produce more highly compressed results and reconstructions that tend to omit abdominal-pressure (motion) induced artifacts in the vesical pressure measurement, whereas a Q of 10 will produce high-fidelity reconstructions including motion artifacts. This is demonstrated in Fig. 4(b). The particular choice therefore depends on the clinical application.

C. Quality of Reconstruction

Fig. 4(a) shows a sample output for a 60 second compression window with $Q = 4$. On average, the compressed data required 8.8 Bytes for each 64 Byte window (14%), with an average root-mean-square (RMS) error of 1.14 pressure units. This is slightly better than the expected compressed size of 17%, and comparable to the expected RMS error of 1.15, as shown in Fig. 4(c). Table I shows results for compression and RMS error for all subjects, at selected quality factors of 0, 5, and 10. In the worst case quality ($Q = 0$), a DCR of 0.16 ± 0.02 was achieved, with an RMS error of 1.34 ± 0.40 , while in the best case ($Q = 10$), a DCR of 0.27 ± 0.10 was achieved, with an RMS error of 0.81 ± 0.18 . Fig. 4(b) visually demonstrates how the output can vary for different levels of Q ; note that, for the lower levels of quality (0 and 3), both rises in pressure are ignored, whereas at higher levels of quality (6 and 9), one or both events are represented. DCRs for these windows range from 5% ($Q = 0$, 3) to 17% ($Q = 6$) and 23% ($Q = 9$).

IV. ON-CHIP EVENT DETECTION

The Context Aware Thresholding (CAT) algorithm has been previously tested on both recorded bladder pressure in a simulated real-time environment [13], as well as in real-time in a prospective study with a single human subject, demonstrating effective event detection for closed-loop control of the human bladder [12]. While CAT was designed to be efficient in hardware, it has not yet been implemented as such.

The basis of the CAT algorithm is the separation of vesical pressure into high and low frequency components followed by adaptive thresholding on each resulting signal. At a given time t , the current window's threshold value is computed as the n th percentile from an ordered list of pressure samples. The four tap Daubechies wavelet *db2* is used for generating high and low pass filter coefficients. This wavelet was chosen because on short time scales, the slow-changing vesical pressure signal can be approximated well with constant and linear polynomial terms. However, the hardware cost of the more complex *db2* wavelet, as compared to the Haar wavelet, is relatively high, requiring addition/subtraction and multiplication with floating point numbers (e.g. $\sqrt{3}/4$). The Haar lifting scheme, on the other hand, can utilize simple binary addition/subtraction and bit shifts for division by 2. The loss of a single bit of precision due to bit shifting is acceptable in both diagnosis and treatment applications, making Haar the superior choice from an area/power perspective.

However, using Haar, we lose the ability to encode approximation polynomials with degree

1. On short time scales (e.g. 0.5s), and not during a significant event such as a contraction, human bladder pressure is relatively constant. On the other hand, during a contraction, the maximum pressure rate of change occurring within the bladder is around 10 cm H_2O /s, and therefore will not typically remain constant during a 0.64 s window. Moreover, the Haar detail coefficients actually encode deviations from the pairwise signal average, which provides additional information about the activity in the signal. We can leverage this additional information to enable efficient event detection in hardware by activating the decision making circuitry only when the signal activity exceeds a threshold value.

A. Detecting Activity in the Wavelet Space

Similar to the Detail Threshold (T_d) described in Section III-B, the Activity Threshold is determined using the same human cystometry dataset. For each recording, all bladder events—defined as a precipitous rise in pressure at least 10 cm H_2O above the mean—were noted, and the signal activity, as measured by the 3rd and 4th level Haar detail coefficients, was logged. Recall that the compression scheme operates on 64 (2^6) samples at a time; thus, there are 8 (2^3) coefficients in the 3rd detail level, and 4 (2^2) coefficients in the 4th detail level. At these scales, there is a time resolution of 0.08 and 0.16 seconds per sample, so more weight is given to deviations at the 4th level of detail than to those at level 3. Specifically, the number of coefficients above T_d in level 3 are divided by 2, which can be accomplished by a right bit shift in hardware, and added to the number of coefficients above T_d in level 4. If the activity score $AS > 1$, the event detector is enabled. In effect, this activity threshold acts as a gating mechanism to the event detection hardware. The activity detection is lightweight, re-using the output from the compression's Haar transform stage, and can therefore reduce overall power consumption.

The caveat to using the number of non-zero detail coefficients is that the sensitivity of the activity detection will vary with T_d : higher values of T_d will tend to make the gating mechanism less sensitive, but could potentially cause the implant to miss important events. Conversely, a low value of T_d , which is ideal for diagnosis, will tend to be more sensitive to changes in pressure, regardless of the cause, potentially enabling the event detector more often than necessary. As shown in Table I, the average duty cycle of the event detection hardware ranges from $36\% \pm 22\%$, $25\% \pm 19\%$, and $20\% \pm 16\%$, for $Q = \{0, 5, 10\}$, respectively. The Detection Accuracy is given for $Q = 5$, averaging $91\% \pm 5\%$ events detected, with 0.4 ± 0.2 false positives per event detected [12]. As noted in previous work, successful event detection means that the algorithm automatically detected the event within 1 second of event onset. In practice, as long as the event is detected “in time”, which may be *several* seconds after onset [13], there will still be sufficient time to inhibit the bladder contraction by triggering neurostimulation. Performance of the modified event detection algorithm is shown in Table II.

B. Computation of the Adaptive Event Thresholds

The original design of the CAT algorithm calls for adaptive thresholds which are computed independently on signal approximations and details using separate percentile values. Computation of the percentile is achieved using a sorted list. An 8-bit, 8-input bitonic sorting network [23] is used for sorting incoming values, such that 1.28 seconds worth of sample history are used in the computation. We also adopt the nearest rank definition of percentile computation; in the case of 8 items, the value at index 7 corresponds to the 90th percentile. This greatly simplifies the hardware implementation at the cost of some precision. A diagram of the bitonic sorter is provided in Fig. 5.

V. IMPLEMENTATION RESULTS

The algorithm was implemented in hardware using Verilog HDL, synthesized to gates using Synopsys Design Compiler, and Cadence Encounter was used for layout. We perform synthesis and layout at the $0.18 \mu\text{m}$ and $0.5 \mu\text{m}$ technology nodes to observe the effects of scaling on the design. The design was simulated using Synopsys VCS using as input samples from the human cystometry dataset, described in Section III. The overall hardware architecture is shown in Fig. 6.

A. Compression Hardware Architecture

Initial filtering (EWMAF) is performed with $\alpha = 0.5$, enabling the use of efficient bit-shifting instead of more costly division. The Haar lifting scheme (HAAR_XFM) is implemented sequentially in a single module, which enables efficient resource utilization. In addition, following the operations defined in Eqns. (2) and (3), the implementation operates on data in-place, such that only a single $n \times m$ – bit set of registers is required for all stages, as shown in Fig. 6(b). A total of 4 stages are used to process the 64 byte packets, leading to $64 \gg 4 = 4$ bytes of approximation coefficients, which are generally non-zero, and 60 bytes of detail coefficients. In practice, the majority of the details in Level 1 (32 bytes) and Level 2 (16 bytes) are below T_d and are therefore omitted from the packet. Any detail coefficients above the threshold are considered to be important or significant events in the signal, and are

therefore retained in the packet. Once coefficients are computed, the packet is transferred to the run length encoder, which encodes data and assembles it into the final packet format (RLE_PKT) for transmission.

B. Event Detection Hardware

As described in Section IV, event detection occurs in two stages: activity detection and event detection. Activity detection requires very few components. If one non-zero value is identified in the transform packet between bytes 4 and 7 (detail level 4), or two non-zero packets are found between bytes 8 and 15 (detail level 3), the remaining comparisons are not executed, and the Event Detection circuitry is enabled (SN_EN in Fig. 6(c)). Then, the most recent approximation coefficient (i.e. byte 3 of the transform packet) is compared to the 90th percentile value (at rank 7 of 8) at the previous output of the sorting network; if it exceeds this value, an event is considered to have occurred. The new values are then shifted into the sorting network inputs. However, because an 8-input network is used, and there are already 8 values stored for each set of coefficients, it is necessary to have one additional comparator to handle the new input. This is used to check whether the new input is greater than the smallest stored coefficient. If it is, it will replace the smallest coefficient in the memory prior to sorting. Otherwise, no sorting is required, and the new value is discarded. Once sorting is complete, the newly ordered values are buffered at the output for comparison in the next cycle.

Two sets of buffers are available, one for the approximation coefficients, and one for the details, and a control unit selects which are written to or read from each time a packet is processed. For the bitonic sorting network, the number of comparators required is $\mathcal{O}(n \log^2(n))$. Therefore, it is preferable to have two sets of 8×8 -bit registers than to have two separate sorting networks for the two types of coefficients. Other, more area efficient sorting networks, such as Knuth's provably-optimal 8 input sorting network, can be used to reduce area and power overhead.

C. Hardware Emulation

The above designs for the compression and event detection circuitry were first tested in simulation with VCS, and then mapped to a Field Programmable Gate Array (FPGA), which enables hardware emulation of the design for functional and timing verification in hardware. The design was mapped to a Cyclone IV (EP4CE22) device, which operates at a core voltage of 1.0V and contains 22,320 programmable logic elements. A Terasic DE0-Nano development board, which contains the EP4CE22, was used for testing.

The design occupied roughly 54% of the device resources (12,139 of 22,320), while operating at a maximum frequency of 29.06 MHz. A breakdown of the area utilization by submodule is given in Table III. Note that the majority of the area – just under 75% – is dedicated to the Haar transform module, while the only major Event Detection submodule is the bitonic sorter, which consumes nearly 95% of the logic elements in the event detection module. The estimated power consumption for the design, obtained using Quartus II PowerPlay Power Analyzer and vector-based estimation, was 106 mW, making it suitable for an external application, such as part of a pressure monitoring and data logging system.

While the DE0-Nano development board does have an on-board ADC, for the purpose of emulation, we opted to load samples from on-chip memory in the FPGA. Sample data were converted to the appropriate memory initialization file (MIF) format, and read in at the system frequency of 25 MHz. Signal activity was observed using the built-in SignalTap II Logic Analyzer, which enables us to monitor internal nodes in near real-time. The outputs, including signal activity levels, state of the event detection circuitry, and compressed packets, were logged and compared with simulation results, and were found to match for the sample data. An example output is shown in Fig. 7. Here, the detrusor pressure signal is shown for reference. The signal activity level indicates when the event detection circuitry is enabled. The three overlaid signals show the three different types of outputs possible from the system, including constant compressed packets (solid line), "snapshot" packets, which are only transmitted when there is sufficient signal activity (dashed line), and event codes (circle markers). At this time, the event detector only detects contraction events, and therefore only needs a binary value to indicate whether or not an event has occurred.

D. Area, Power, and Performance

Layouts with TSMC 0.18 μm and AMI 0.5 μm technology [24] result in total areas of 1.75 mm^2 and 15.00 mm^2 . Roughly 40% of the overall area is due to the memory elements, implemented as flip-flops. Using different memory technologies such as SRAM, or even emerging nanoscale memory technologies, can result in significant area reduction.

One key observation in the design is the relatively low clock frequency required for functional operation. Specifically, the ADC performs 100 Hz sampling, yielding one 64 Byte packet every 0.64 seconds. By comparison, the algorithm requires between 318 and 444 cycles – with a considerably shorter critical path – to produce a compressed packet; the variation in cycles arises from the packet output stage, since its duration depends on the resulting packet size. On average, the number of cycles will vary from 325 to 332 for different values of Q ranging from 0 to 10, respectively. This presents many opportunities for low power design, including

- 1) Using high V_T gates for static power reduction.
- 2) Coarse-grained supply gating of individual pipeline stages for static power reduction.
- 3) Reducing V_{DD} for static and dynamic power reduction.

Table IV shows synthesis results at 0.18 μm and 0.5 μm technology nodes. Note that the static power for 0.5 μm is about 1.5x higher than that at 0.18 μm , as shown in the standard cell library reference [24]. Synthesis results at 0.18 μm also demonstrate that static power is about 10x greater than the dynamic power when operating at the minimum required frequency, roughly 7x the speed of the sample clock – in this case, 694 Hz – as dictated by the worst case number of processing cycles. Scaling below 0.18 μm would exacerbate this disparity; it is crucial, therefore, to reduce the effect of leakage on the circuit. Supply gating has been effectively used in similar situations [25], and has been shown to effectively reduce leakage power by above 90% in some cases [26]. Therefore, we can expect to achieve significant power savings by operating at a higher frequency, leading to longer idle times. By

varying the DC_CLK frequency between 1 kHz and 100 MHz, and assuming the worst case average runtime (332 cycles), we observed that the total (static + dynamic) average power consumption can be reduced from 1.2 μ W to as low as 2.6 nW (0.18 μ m), and from 3.6 μ W to 17.8 nW (0.5 μ m). This is achieved in both cases when operating DC_CLK at 1 MHz, leading to an effective duty cycle of $5.4 \times 10^{-4}\%$ compared to the 0.64 s required to fill the 64 Byte sample buffer. This also reduces the post-packet acquisition latency, enabling more responsive conditional neurostimulation in treatment applications [12]. In addition, we assumed $Q = 5$ for the purposes of the activity detection, which results in an average event detection duty cycle of about 25% (Table I), which further reduces the power consumption. Furthermore, if *only* event detection is required, the RLE_PKT stage, which consumes approximately 18% of the total power, can be permanently disabled, leading to an average power consumption of 2.1 nW and 14.6 nW for 0.18 μ m and 0.50 μ m, respectively.

Supply gating transistors also require additional power control signals. Due to the deterministic nature of the first three pipeline stages, each module can generate the supply enable signal for its neighbor (“PWC” in Fig. 6(a)). We adopt this approach to simplify the IC power network design and reduce the area overhead.

VI. CONCLUSION

We have presented a novel, tunable algorithm for wavelet transform based efficient compression of bladder pressure data. We have tested the algorithm using a large human cystometry dataset, and results show excellent compression with low average RMS error. We have integrated the compression algorithm with Context Aware Thresholding, which has been modified to operate in ultralow power hardware, sharing considerable resources for improved area and energy efficiency, while not sacrificing detection accuracy. The proposed framework will enable future bladder pressure monitoring devices to transmit either compressed data at various levels of compression, compressed snapshots of events, or only event codes for the highest energy efficiency, providing physicians with the flexibility to choose between the diagnosis and treatment options using the same implant. We have presented efficient hardware implementation of our design. Results from synthesis and layout of the hardware in 0.18 μ m technology demonstrate ultra-low average power of 2.6 nW with an area of 1.75 mm². To the best of our knowledge, this is the first example of a combined compression and event detection algorithm which is tailor-made to human bladder pressure data, that is also amenable to ultralow-power hardware implementation. In this way, it can simultaneously support diagnosis, long-term monitoring, and treatment of lower urinary tract dysfunction using a closed-loop system. Furthermore, it can provide an important tool for biomedical research in this area.

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Biography

Robert Karam (S'12–M'17) received the B.S. and M.S. degrees in computer engineering from Case Western Reserve University (CWRU), Cleveland, OH, USA, in 2012 and 2016, respectively, and the Ph.D. degree in computer engineering from the University of Florida, Gainesville, FL, USA, in 2017.

From 2012 to 2017, he was with the L. Stokes Cleveland VA Hospital, Advanced Platform Technology Center (APTC) as a Biomedical Engineer, where he developed novel algorithms and hardware for processing bladder pressure signals. In 2017, he joined the Department of Computer Science and Engineering, University of South Florida as an Assistant Professor, where he conducts research in the areas of hardware security, reconfigurable computing, and algorithm and hardware code-sign for implantable devices and wearables.

Dr. Karam is a member of ACM, and has served as a reviewer for several IEEE journals, including IEEE TRANSACTIONS ON MULTI-SCALE COMPUTING SYSTEMS (TMSCS) and IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS (JETCAS). He received an NSF Award for Young Professionals Contributing to Smart and Connected Health at the 2016 IEEE Engineering in Medicine and Biology Conference (EMBC), as well as a Best Paper Award at the 2016 IEEE Biomedical Circuits and Systems Conference (BioCAS).

Steve J. A. Majerus (M'06–SM'16) received the B.S. and M.S. degrees in electrical engineering from Case Western Reserve University (CWRU), Cleveland, OH, USA, in 2007 and 2008, respectively, and the Ph.D. degree for the design and implementation of an ultra-low-power CMOS ASIC for wireless bladder pressure monitoring in 2014.

From 2009 to 2012, he was with Scientific Monitoring as an IC design engineer, where he designed a high-temperature (200 °C) bulk-CMOS chip set for distributed aircraft engine controls, consisting of a delta-sigma sensor interface, linear IDAC spool valve controller, and programmable dual PWM H-bridge. He continued this work from 2012 to 2015 with BluBerry, where he designed a 225 °C brushless DC motor controller ASIC. From 2014 to 2016, he was a Sr. Research Associate at CWRU, studying integrated 4H-SiC JFET instrumentation amplifiers for (>450 °C) operation. Meanwhile, since 2007, he has been with the Advanced Platform Technology Center (APTC) in Cleveland, OH continuing his work in low-power ASICs for biomedical applications. In 2014, he was appointed a Core

Investigator for APTC and is continuing his research in implantable pressure sensors, intravascular ultrasonic imaging, and vascular health monitoring.

Dr. Majerus is a reviewer for several IEEE journals, including IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS, IEEE SENSORS JOURNAL, IEEE TRANSACTIONS ON MULTI-SCALE COMPUTING SYSTEMS, and IEEE TRANSACTIONS ON NEURAL SYSTEMS AND REHABILITATION.

Dennis J. Bourbeau received the B.S. degree in biomedical engineering and international studies from Worcester Polytechnic Institute (WPI) in Worcester, MA, USA, in 2002, and the Ph.D. degree in bioengineering from the University of Pittsburgh in Pittsburgh, PA, USA, in 2011, for using microstimulation of spinal roots to evoke functional hindlimb motor responses.

In 2011, he was appointed as a Biomedical Engineer at the Louis Stokes VA Medical Center, Cleveland, OH, USA, to conduct research focusing on developing approaches that use electrical stimulation to restore pelvic autonomic functions lost to spinal cord injuries or other neurological disorders. In 2016, he was dually appointed Staff Scientist at the MetroHealth Medical Center, Cleveland, to continue his research on neurogenic pelvic autonomic dysfunctions.

Dr. Bourbeau is a member of the Society for Neuroscience, the Academy of Spinal Cord Injury Professionals, and the American Spinal Injury Association, and serves on the Research and Development committee at the Cleveland VA Medical Center.

Margot S. Damaser (SM'03) received the A.B. (Hons.) degree in engineering science from Harvard and Radcliffe Colleges, Cambridge, MA, USA, in 1987, and the Ph.D. degree from the Joint Bioengineering program of the University of California at Berkeley and San Francisco, CA, USA, in 1994. She completed two postdoctoral fellowships, one in the Departments of Urology and Physiology & Biophysics at Lund University, Lund, Sweden, and the 2nd in the Urology Department of the Hospital of the University of Pennsylvania, Philadelphia, PA, USA.

She is currently a Professor of molecular medicine in the Cleveland Clinic Lerner College of Medicine at Case Western Reserve University, Cleveland, OH, USA and has joint appointments as Full Staff in the Biomedical Engineering Department of the Lerner

Research Institute and the Glickman Urological and Kidney Institute at Cleveland Clinic, Cleveland, OH, USA. She also is a Senior Research Career Scientist in the Advanced Platform Technology Center of the Louis Stokes Cleveland Department of Veterans Affairs Medical Center, Cleveland. She has conducted research on urodynamics and the causes of and treatments for urinary incontinence for over 20 years. She has more than 130 scientific peer-reviewed publications, has a number of patents pending, and has had research grants from NIH, VA, private foundations, and several companies. She is widely regarded as an International Expert on urodynamics, models for studying female pelvic floor disorders, and new technologies in female urology and pelvic floor disorders. She is currently developing several novel devices & systems for improved diagnosis and treatment of incontinence.

Dr. Damaser serves on NIH, VA, DOD, and private foundation study sections and as an editorial board member of the journal *Neurourology & Urodynamics* and *PLoS ONE*. In 2000, she was awarded the Presidential Early Career Award for Scientists and Engineers, for outstanding research on the human urinary bladder using mathematical modeling along with physiological and neurological studies. This is the highest honor bestowed by the U.S. Government on young professionals at the outset of their independent research careers. In 2014 she was elected to the American Institute for Medical and Biological Engineering (AIMBE) College of Fellows, representing the top 2% of medical and biological engineers. Dr. Damaser is a reviewer for several IEEE journals including IEEE TRANSACTIONS ON BIOMEDICAL ENGINEERING.

Swarup Bhunia (M'05–SM'09) received the B.E. (Hons.) degree from Jadavpur University, Kolkata, India, the M.Tech. degree from the Indian Institute of Technology (IIT), Kharagpur, India, and the Ph.D. degree from Purdue University, West Lafayette, IN, USA. Currently, he is a preeminence Professor and Steve Yaturu Faculty Fellow of Electrical and Computer Engineering in the University of Florida, Gainesville, FL, USA. Earlier he served as the T. and A. Schroeder Associate Professor of Electrical Engineering and Computer Science at Case Western Reserve University, Cleveland, OH, USA.

He has over ten years of research and development experience with over 200 publications in peer-reviewed journals and premier conferences and six authored/edited books. His research interests include hardware security and trust, adaptive nanocomputing, and novel test methodologies. He received the IBM Faculty Award (2013), National Science Foundation career development award (2011), Semiconductor Research Corporation Inventor Recognition Award (2009), and SRC technical excellence award (2005) as a team member, and has received several best paper awards and nominations. He is cofounding editor-in-chief of a Springer journal on hardware and systems security. He is also a cofounder of a startup, Hakham Systems, which aims at developing hardware security education platforms.

Dr. Bhunia has been serving as an Associate Editor of IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, IEEE TRANSACTIONS ON MULTI-SCALE COMPUTING SYSTEMS, *ACM Journal of Emerging Technologies*, and *Journal of Low Power Electronics*, and has served as guest editor of IEEE DESIGN & TEST OF COMPUTERS (2010, 2013) and IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS (2014). He has also served as co-program chair of IEEE IMS3TW 2011, IEEE NANOARCH 2013, IEEE VDAT 2014, and IEEE HOST 2015, and in the program committee of several IEEE/ACM conferences.

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Fig. 1.

(a) Schematic diagram illustrating the use of an implanted wireless bladder pressure monitor for diagnosis and treatment of lower urinary tract dysfunction. (b) Breakdown of current draw for wireless transmission by the implant at 100 Hz ($95\ \mu\text{A}$) vs 1.5 Hz ($10.5\ \mu\text{A}$); other circuitry independently draws $10\ \mu\text{A}$ [3]. (c) Measured vesical pressure, showing a contraction starting at time $t \approx 125$. The insert shows that, on small scales, the signal changes very slowly, and is therefore highly compressible (from [10]).

Fig. 2.

Algorithm flow for efficient compression of bladder pressure data. Outputs of each stage are shown to the right [10].

Fig. 3.

Example of two-pass Run Length Encoding on the transformed data. In Pass 1, the data is encoded; in Pass 2, the Pass 1 header content itself is encoded in the same manner.

Fig. 4.

(a) (Top) Sample algorithm output ($Q = 4$) showing original and reconstructed pressure signals for 60 seconds of data. The compressed signal required an average 8.8 Bytes for each 64 Byte window, with an average RMS error of 1.14; (Bottom) Post-threshold detail coefficients from the lifting scheme. The extended 0-runs enable more efficient compression by Run Length Encoding. (b) Sample algorithm outputs for a single 64 byte (0.64 second) window showing variation in output for various values of Q ; note that, in this case, a $Q = 3$ disregards transient pressure spikes, and the entire window is represented as the signal average. (c) Quality of algorithm output, comparing average compression ratios with corresponding reconstruction error for all values of Q (from [10]).

Fig. 5.

An 8-bit, 8-input bitonic sorting network. Connections represent comparisons, such that inputs are sorted in descending order.

Fig. 6.

(a) Hardware implementation of the data compression algorithm, optimized for ultra-low power consumption. Neighboring modules enable power and clock signals to subsequent processing stages. (b) Expanded view of lifting scheme implementation, featuring memory resource reutilization for area and power efficient processing ([10]) (c) the Activity Detector operates on the transform output and selectively enables the Event Detector for improved power efficiency.

Fig. 7.

Example outputs of compression and event detection hardware on data from two subjects. (top) Original detrusor pressure signal. (center) Three output modes ($Q = 5$), showing compressed data (diagnosis), snapshot output (diagnosis/treatment), or events only (treatment). (bottom) Activity detection signal, which controls power to the event detection hardware. Events (circle markers) are successfully detected shortly after onset, which is important for inhibiting unwanted events [12].

TABLE I

AVERAGE COMPRESSION AND RECONSTRUCTION ERROR FOR SUBJECTS 1–14, FOR $Q = \{0, 5, 10\}$ (STANDARD DEV. SHOWN)

#	Compression (Frac. of Orig.)			Error (RMS)		
	0	5	10	0	5	10
1	0.23	0.29	0.58	2.53	2.10	1.33
2	0.17	0.20	0.29	1.54	1.20	0.81
3	0.16	0.16	0.20	0.95	0.85	0.69
4	0.15	0.18	0.27	1.31	1.05	0.73
5	0.15	0.18	0.26	1.48	1.20	0.83
6	0.16	0.18	0.29	1.43	1.23	0.86
7	0.14	0.17	0.24	1.21	0.98	0.68
8	0.13	0.14	0.19	1.08	0.82	0.59
9	0.15	0.17	0.23	1.32	1.14	0.84
10	0.16	0.17	0.20	1.09	0.98	0.82
11	0.17	0.18	0.27	1.36	1.22	0.94
12	0.17	0.20	0.28	1.40	1.17	0.84
13	0.14	0.15	0.16	0.68	0.61	0.53
14	0.16	0.18	0.26	1.41	1.22	0.89
	0.16 ± 0.02	0.18 ± 0.03	0.27 ± 0.10	1.34 ± 0.40	1.13 ± 0.32	0.81 ± 0.18

TABLE II

AVERAGE DUTY CYCLE (TIME WHEN EVENT DETECTION IS ENABLED) AND CORRESPONDING DETECTION ACCURACY (STANDARD DEV. SHOWN)

#	Event Detector Duty Cycle			Detection Accuracy	
	$Q = 0$	$Q = 5$	$Q = 10$	Events (%)	FPR [12]
1	0.71	0.60	0.54	82	0.4
2	0.18	0.08	0.06	97	1.1
3	0.40	0.28	0.21	93	0.5
4	0.75	0.61	0.49	87	0.2
5	0.02	0.01	0.01	95	0.3
6	0.45	0.36	0.28	92	0.3
7	0.09	0.07	0.06	82	0.7
8	0.32	0.19	0.13	90	0.5
9	0.33	0.21	0.16	88	0.4
10	0.05	0.03	0.02	90	0.4
11	0.60	0.48	0.31	99	0.6
12	0.31	0.15	0.11	85	0.1
13	0.44	0.16	0.10	94	0.2
14	0.44	0.31	0.27	96	0.3
	0.36 ± 0.22	0.25 ± 0.19	0.20 ± 0.16	91 ± 5	0.4 ± 0.2

TABLE III

HARDWARE MAPPING RESULTS FOR EP4CE22 FPGA: AREA UTILIZATION BY SUBMODULE

Submodule	Area (LEs)	% Total Area
Input Filtering	18	< 1
Haar Transform	8989	74
Packet Assembly	1003	8
Sample Buffer	20	< 1
Event Detection	2109	17
Total	12,139	100

TABLE IVSYNTHESIS RESULTS WITH AND WITHOUT LEAKAGE CONTROL FOR 0.18 μM AND 0.5 μM TECHNOLOGIES

	w/ Control		w/o Control	
	0.18 μm	0.5 μm	0.18 μm	0.5 μm
DC_CLK (kHz)	1000	1000	1	1
P_{avg} (dyn) (nW)	0.89	14.8	108.0	1819
P_{avg} (sta) (nW)	1.68	2.82	1072	1797
P_{avg} (tot) (nW)	2.56	17.5	1181	3637
Eng./Packet (nJ)	104.8	718.0	756.1	1232