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An Inductive Voltage/Current-Mode Integrated Power Management with Seamless Mode Transition and Energy Recycling

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Abstract

An integrated power management (IPM) with the unique capabilities of seamless-voltage/current-mode (SVCM) operation and energy recycling is presented for robust inductive power delivery. Utilizing parasitic bulk diodes with lower voltage drop, this IPM seamlessly transitions between voltage mode (VM) and current mode (CM) in a safe and robust fashion, extending the input-voltage range (removing dead zone) and significantly improving power-conversion efficiency (PCE) in CM operation. The IPM first provides the required load power (P_L) by one-step rectification/regulation, and then stores the surplus energy into a storage capacitor to extend the receiver (Rx) operation time via energy recycling when the input power is insufficient. The theory behind the energy recycling is presented. A proof-of-concept chip was fabricated in a 0.35 μm CMOS process. In measurements, the chip safely achieved a regulated voltage of 3 V for a wide input-voltage range (without dead zone) by switching the Rx LC-tank at 142 kHz. With zero input power, the chip extended the Rx operation time by 250% thanks to the energy recycling.

Keywords

Inductive link; power management; energy recycling; DC-DC converter; voltage/current mode; rectifier

I. INTRODUCTION

INDUCTIVE coupling is widely used for wireless power transmission (WPT) in applications such as implantable medical devices (IMDs) [1]–[3]. Fig. 1a shows a conventional inductive WPT link with a transmitter (Tx) coil (L_1), driven by a power amplifier (PA), and a receiver (Rx) coil (L_2) followed by a power management (rectifier + regulator) to convert the received AC voltage (V_R) to a constant DC voltage (V_L) across the load (R_L). A key requirement in inductive WPT is to efficiently and reliably deliver

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required power to the load ($P_L = V_L^2/R_L$) considering worst-case variations of powering distance (d), coils' alignment and orientation, and R_L .

Conventional integrated power management (IPM) structures utilize a two-step AC-DC conversion (Fig. 1a), which can remarkably reduce the power conversion efficiency (PCE) within the Rx, particularly when the received power (P_{Rx}) is much higher than the required P_L [4]–[6]. In this paper, PCE is defined as P_L/P_{Rx} . To improve PCE and remove one off-chip capacitor, rectification and regulation can be performed in one step [7]–[9]. But when P_{Rx} is much higher than the required P_L in conditions such as reduced d , perfect alignment, or increased R_L , additional P_{Rx} will be wasted within the Rx (P_{Waste} in Fig. 1a) due to voltage regulation or over-voltage protection (OVP). Thus, there is a need for IPM structures that can restore such dissipated power (Fig. 1b).

Inductive IPMs can operate in voltage mode (VM) [10], current mode (CM) [11]–[13], or reconfigurable voltage/current mode (VM-CM) [14], [15]. While VM structures, utilizing active switches, achieve high PCE, their voltage conversion efficiency, defined as $VCE = V_L / V_{R,peak}$ (V_R amplitude), is low. They can improve VCE by utilizing off-chip components, such as an inductor in a boost converter, adding to the Rx size, complexity, and cost [16]. Although CM structures can increase VCE particularly when $V_{R,peak} < V_L$, they suffer from low PCE when $V_{R,peak} > V_L$.

For optimal operation with both small and large V_R , we have recently proposed the VM-CM structure that discretely switches between VM and CM based on $V_{R,peak}$. But VM-CM suffers from multiple shortcomings: 1) during the CM operation, large $V_{R,peak}$ can occur (particularly when V_R is large) that can damage the IPM (unsafe operation), thus limiting the V_R range, 2) discrete switching between VM and CM requires additional circuitry for V_R sensing and control, and 3) due to the power transistors' voltage drop, $V_{R,peak}$ threshold for discrete switching depends on P_{Rx} and P_L which change during operation, further complicating the design.

Fig. 2 summarizes the safe operation region of VM, CM, and VM-CM structures. It shows that current IPM structures cannot tolerate a wide range of V_R , thus creating a dead zone. To extend the safe V_R range and remove the dead zone, we have recently proposed a seamless-voltage/current-mode (SVCM) structure [17]. This structure seamlessly transitions between VM and CM during each switching cycle, and employs the parasitic bulk diode of the power transistor to limit $V_{R,peak}$ within the safety region (remove the dead zone).

Compared with [17], in which we only presented the SVCM concept with some measurement results, in this paper we have the following contributions: 1) detailed description of the SVCM operation and its control circuits validated by more measurement results, and more importantly 2) a unique energy-recycling technique (Fig. 1b), combined with SVCM in a novel fashion, in which surplus received energy is stored and recycled when needed, thus improving the Rx operation time and minimizing P_{Waste} in Fig. 1a. Although energy recycling has been utilized in energy harvesting in past [18], to the best of our knowledge this is the first work that demonstrates energy recycling for inductive power delivery.

In this work, we have combined both energy-recycling and SVCM techniques in a proof-of-concept chip prototype called energy recycling seamless-voltage/current-mode (ERSVCM) IPM chip. The SVCM and energy-recycling concept and circuit modeling will be discussed with details in Section II. The ERSVCM chip architecture, including detailed circuit schematics and operations, is presented in Section III, followed by the comprehensive measurement results and conclusion remarks in Sections IV and V, respectively.

II. PROPOSED ENERGY RECYCLING AND SEAMLESS-VOLTAGE/CURRENT-MODE (SVCM) TECHNIQUES

A. SVCM Concept

Fig. 3a shows the simplified circuit schematic of the proposed SVCM technique for charging C_L to regulated V_L of 3 V by operating in both VM and CM via controlling P_2 and N_1/P_1 switches with SW_2 and SW_1 , respectively. Similar to our VM-CM structure in [15], in SVCM only two off-chip capacitors, i.e., C_2 for resonance and C_L , are needed for rectification, regulation and OVP, eliminating one off-chip capacitor.

Fig. 3b shows the conceptual waveforms of L_2 current (i_{L2}), V_R , V_L , and $SW_{1,2}$ for the SVCM operation with self-regulation and OVP at the power carrier frequency of $f_p = 1/T_p$. During each repeated time period of T_{sw1} , the operation mode seamlessly transitions from VM for $[T_{sw1}/T_p - 1]$ power cycles to CM for one T_p . In VM, N_1/P_1 are turned on (SW_1 : high), and P_2 acts as an active switch (half-wave active rectifier) to charge C_L if $V_R > V_L$. For $V_R < V_L$, the L_2C_2 -tank just stores the received energy as P_2 is off. In CM, P_2 is turned off (SW_2 : high), V_{B2} is connected to V_L to employ P_2 parasitic source-bulk diode (D_2), and at the time zero-crossing of V_R with the maximum energy stored in L_2 (i_{L2} peak), N_1/P_1 are tuned off to generate a sharp $V_{R,peak}$ as large as $\sim [V_L + 0.7]$ V to charge C_L via D_2 , which is the only path for i_{L2} . Therefore, a high VCE greater than one can be achieved for $V_R < V_L$ [12]. Such T_{sw1} cycle with VM and CM operations is repeated over and over.

Unlike active rectification in VM, passive rectification (D_2) is utilized in CM because the on-time duration of P_2 in CM should be relatively much smaller (particularly for low P_{Rx}), which will require a wideband comparator with minimal offset, increasing power consumption.

Since D_2 is only used for short time periods during CM charging phase and P_2 bulk is connected to highest voltages for the rest of the operation, utilizing the bulk diode has minimal adverse effect on the P_2 performance. However, one should be careful about any current injections from the body of P_2 to the main substrate. In the layout, we separated power transistors from sensitive circuits.

Similar to [15], the reverse current from C_L to the L_2C_2 -tank is used for the self-regulation of V_L and OVP. When V_L is larger than the desired supply level (3 V in this work), the on-time duration of P_2 is increased by the proper adjustment of SW_2 waveform. Therefore, P_2 remains on for longer time to allow the reverse current to flow from C_L to the L_2C_2 -tank, regulating V_L at 3 V. In addition, connecting C_L to the L_2C_2 -tank via P_2 detunes Rx which is used for OVP when V_R is drastically higher than V_L .

Fig. 4a compares simulated $V_{R,peak}$ of the conventional CM [15] and the proposed SVCM ($V_L = 3$ V) at different steadystate V_R (no switching). As V_R was increased to ~ 2 V, in the conventional CM with a diode-connected pass transistor more energy was stored into the L_2C_2 -tank in each cycle, and consequently, larger and unsafe $V_{R,peak} > 5$ V was occurred, creating a dead zone for $V_R > 2$ V. In contrast, SVCM delivered the same amount of energy with much smaller and safer $V_{R,peak} < 4$ V (removing the dead zone), because $V_{R,peak}$ was limited to $[V_L + 0.7]$ V thanks to the parasitic diode D_2 with smaller voltage drop and shorter turn-on time.

Fig. 4b compares simulated PCEs of our VM-CM in [15] and SVCM at different R_L ($V_L = 3$ V). For $R_L = 5$ k Ω , at which both structures only operated in CM due to low $V_{R,peak}$, SVCM achieved much higher PCE thanks to D_2 lower voltage drop. At $R_L = 50$ k Ω , SVCM achieved a PCE of 55% compared with 35% of VM-CM ($\sim 1.6\times$ improvement). For $R_L < 5$ k Ω , VM-CM achieved slightly higher PCE because it only operated in VM while SVCM operated mostly in VM and one cycle in CM in each T_{sw1} . Nonetheless, Fig. 4b clearly shows the advantage of SVCM in improving PCE when V_R is low (CM).

B. Energy Recycling Concept and Modeling

Fig. 1b shows the high-level concept of the energy recycling in inductive power delivery with the goal of creating an energy reservoir to store the surplus received energy and recycle it when needed ($P_{Rx} < P_L$). In Fig. 1b, C_L is first charged to the desired V_L using the SVCM operation. Then the surplus P_{Rx} , if any, is stored in a storage capacitor (C_s) as P_{store} over time by SVCM operation. When $P_{Rx} < P_L$ due to any WPT uncertainties, P_{store} is recycled back to C_L ($P_{recycle}$ in Fig. 1b) to maintain functionality. Since C_s voltage (V_{Cs}) could be lower than V_L in some conditions, the Rx LC-tank is reused to transfer energy from C_s to C_L regardless of their voltage levels, thus eliminating the need for an off-chip inductor as in a boost converter and minimizing P_{Waste} in Fig. 1a.

Fig. 5a shows the simplified circuit schematic of the energyrecycling technique in which surplus received energy is first stored on C_s via P_4 and N_1/P_1 switches using the SVCM operation discussed in Section II.A, and then transferred to C_L (if $P_{Rx} < P_L$) via controlling P_4 and N_1/P_1 switches with SW_4 and SW_1 , respectively. P_2 is always off (SW_2 : high) and V_{B2} is connected to V_L .

Fig. 5b shows the energy-recycling key waveforms that can be divided into three regions. In region-I, defined as T_1 duration in Fig. 5b, N_1/P_1 are tuned off and P_4 is turned on ($SW_{1,4}$: low) to transfer energy from C_s to the series L_2C_2 -tank. If $V_{Cs} > [V_L + 0.7]$ V, D_2 is turned on and some energy is transferred to C_L as well. In region-II, defined as T_2 duration, P_4 is tuned off and N_1/P_1 are tuned on ($SW_{1,4}$: high) to have L_2 resonate with C_2 and change the polarity of L_2 current (i_{L2}) to positive for charging C_L in the next step. In addition, the stored energy in C_2 (during T_1) is also transferred to L_2 . In region-III, defined as T_3 duration, at the peak of i_{L2} , where all the energy is stored in L_2 (C_2 is discharged), N_1/P_1 are turned off (SW_1 : low) to deliver all L_2 energy to the load ($R_L \parallel C_L$) via D_2 with a sudden V_R jump to $[V_L + 0.7]$ V. The total switching period (T_{sw2}) in the energy recycling is $T_1 + T_2 + T_3$, which is repeated. By adjusting T_3 and consequently T_{sw2} , V_L can be regulated at its

desired level of 3 V. For instance, if V_L is slightly higher than 3 V, T_3 is elongated until $V_L < 3$ V.

C. Energy-Recycling Modeling

Fig. 6 shows the simplified circuit model of the energy-recycling technique in all three regions with the assumptions of $V_{Cs} < V_L$ (D_2 : OFF in region-I), neglected Tx effect on Rx (often the case for loosely coupled coils, large d), and $C_L \parallel R_L \approx C_L$ (large RL and CL) for the sake of simplicity. Switching transistors ($P_{1,2,4}$, N_1), L_2 , and D_2 in Fig. 5a are modeled with their equivalent loss resistances of $R_{P1,2,4}$, R_{N1} , R_{L2} , and R_{D2} , respectively. Since the equivalent circuit model in all regions includes an inductor and a capacitor (second order), the transient i_{L2} in all regions can be found from,

$$L_2 \frac{di_{L2}(t)}{dt} + \frac{1}{C_T} \int i_{L2}(t) dt + R_T i_{L2}(t) = 0, \quad (1)$$

where R_T and C_T are the equivalent series resistance and capacitance with L_2 , respectively. The solution for i_{L2} can be written as,

$$i_{L2}(t) = \exp(-\alpha(t - t_d)) [A_1 \cos(\omega_d(t - t_d)) + A_2 \sin(\omega_d(t - t_d))], \quad (2)$$

where $t_d = t_0$, t_1 , and t_2 in regions I-III (Fig. 5b), respectively. One can find α and ω_d in (2) from,

$$\alpha = \frac{R_T}{2L_2}, \omega_d = \sqrt{\omega_0^2 - \alpha^2}, \omega_0^2 = \frac{1}{L_2 C_T}, \quad (3)$$

A_1 and A_2 in (2) can also be found from initial conditions,

$$A_1 = i_{L2}(t_d), \quad A_2 = (di_{L2}(t_d)/dt - \alpha A_1)/\omega_d. \quad (4)$$

It should be noted that initial conditions at the onset of each region need to be found from i_{L2} at the end of the precedent region. In region-I, $i_{L2}(t_0) = 0$, $di_{L2}(t_0) = -V_{Cs}(t_0)/L_2$, $R_T = R_{L2} + R_{P4}$ and $C_T = C_2 C_s / (C_2 + C_s)$, where $V_{Cs}(t_0)$ is V_{Cs} initial voltage in region-I. As $V_{Cs}(t_0)$ is increased, $|A_2|$ and consequently i_{L2} also increase which results in more charge transfer from C_s to C_L . By substituting (3) and (4) in (2), one can find $i_{L2}(t)$ in region-I and $i_{L2}(t_1)$ as the initial condition for region-II, in which $R_T = R_{L2} + R_{P1} \parallel R_{N1}$, $C_T = C_2$, and $di_{L2}(t_1) = -[V_{C2}(t_1) + i_{L2}(t_1)(R_{L2} + R_{P1} \parallel R_{N1})]/L_2$ with

$$V_{C2}(t_1) = \frac{1}{C_2} \int_{t_0}^{t_1} i_{L2}(t) dt, \quad (5)$$

using $i_{L2}(t)$ in region-I. In region-III for $t_2 < t < t_3$, $R_T = R_{L2} + R_{D2}$, $C_T = C_L$, and $di_{L2}(t_2) = -[V_L(t_2) + V_{D2} + i_{L2}(t_2)(R_{L2} + R_{D2})]/L_2$ in which $V_L(t_2)$ and V_{D2} are the initial load

voltage and D_2 voltage drop, respectively. Therefore, the amount of V_L increase, i.e., $V_{L,inc}$, after each energy transfer cycle (T_{sw2}) can be calculated as,

$$\Delta V_{L,inc} = \int_{t_2}^{t_3} i_{L2}(t) dt / C_L, \quad (6)$$

using $i_{L2}(t)$ in region-III. For $t_3 < t < t_4$ in Fig. 5b, D_2 forces i_{L2} to remain zero until the next switching cycle (T_{sw2}) begins.

Since the charge transfer to the load only happens at $t_2 < t < t_3$, C_L should provide the required power for R_L for the rest of T_{sw2} , and V_L decreases by $V_{L,dec}$ which can be found from

$$\Delta V_{L,dec} = V_L(t_0) \left(1 - \exp\left(\frac{-T_{off}}{R_L C_L}\right) \right), \quad (7)$$

where $T_{off} = T_{sw2} - (t_3 - t_2)$. It should be noted that for $V_{Cs} > V_L$, D_2 is turned on in region-I, C_L is in parallel with $C_2 C_s / (C_2 + C_s)$, and the same procedure can be carried out to find the circuit parameters with new initial conditions at each region.

It is worth noting that for energy recycling ($P_{Rx} \approx 0$; no WPT), larger C_s is always beneficial for twofold: 1) it avoids $L_2 C_2$ -tank detuning in region-I (Fig. 6a) where C_s is added in series with the $L_2 C_2$ -tank for a short time period (<250 ns), minimizing its effect on PCE, and 2) it provides a larger energy storage reservoir, further improving the Rx operation time when P_{Rx} provided by the inductive link is insufficient.

To validate the accuracy of the energy-recycling model, the energy-recycling circuit in Fig. 5a was simulated in the Cadence Spectre circuit simulator (Cadence Technology, San Jose, CA), and results were compared with those of the model. Table I lists the circuit parameters in our simulations. The operation frequency was considered to be $f_p = 1/(L_2 C_2)^{1/2} = 1$ MHz, initial $V_{Cs} = 2$ V, $V_L = 3$ V, and $V_{D2} = 0$ for simplicity.

Fig. 7 shows simulated vs. calculated results for i_{L2} , V_R , V_{Cs} , V_L , and $SW_{1,4}$ signals for three charge transfer cycles ($3 T_{sw2} = 3 \mu s$). V_{Cs} was discharged gradually from 2 V to 1.93 V to charge C_L from 3 V to 3.04 V. In each T_{sw2} , the energy was first transferred to L_2 increasing i_{L2} to ~ 40 mA, and then SW_1 became low and V_R jumped to 3 V to provide a path for i_{L2} to charge C_L . Although $V_{Cs} < V_L$, the energy was transferred from C_s to C_L thanks to the proposed energy-recycling technique that utilizes the $L_2 C_2$ -tank as a current source. Fig. 7 also shows that simulation and calculation results match very well.

T_1 and T_{sw2} are the two key parameters to regulate V_L at the desired level by controlling the transferred-energy rate. Fig. 8 shows normalized charge transfer vs. T_1 and T_{sw2} . To maximize the amount of the transferred charge, T_1 and T_{sw2} should be maximized and minimized, respectively, because maximizing T_1 allows more energy to be transferred from C_s to L_2 while minimizing T_{sw2} increases the rate of charge transfer. For $f_p = 1/T_p = 1$ MHz,

maximum T_{sw2} and minimum T_1 are approximately $T_p = 1 \mu s$ and $T_p/4 = 250$ ns, respectively.

III. ERSVCM CHIP ARCHITECTURE

Fig. 9 shows the block diagram of the proposed ERSVCM chip operating at $f_p = 1$ MHz to generate a constant V_L of 3 V. The configuration-selection block determines whether the chip should operate in SVCM or energy-recycling configurations based on V_L , V_{Cs} and V_R amplitudes according to the operation algorithm shown in Fig. 10. The operation of the ERSVCM chip can be divided into three regions: energy recycling (Re₃), charging C_L to 3 V via SVCM (Re₁), charging C_s up to 4 V via SVCM (Re₂). Between Re₁ and Re₂, Re₁ has the priority, meaning that the chip first operates in Re₁ to charge C_L to 3 V, and then it switches to Re₂ to charge C_s up to 4 V. If C_s is still charging and V_L goes below 3 V, the chip automatically switches back to Re₁ to charge C_L back to 3 V, and then again switches back to Re₂ to charge C_s . When C_s is charged to 4 V, the chip remains in Re₁ and employs reverse current to regulate V_L at 3 V as long as P_{Rx} is enough. If P_{Rx} is not enough, the chip switches to Re₃ to use energy recycling.

In Re₁, $SW_{3,4}$ are high ($P_{3,4}$: OFF), and V_{B1} , V_{B3} , and V_{B4} are connected to the highest voltage between zero or V_n (the source voltage of PI in Fig. 9), V_R or V_{Cs} , and V_n or V_{Cs} , respectively. The switch-controller block generates proper $SW_{1,2}$ signals based on the SVCM technique (Section II.A). In Re₂, P_2 and D_2 are turned off (SW_2 : high, V_{B2} : the highest voltage between V_R and V_{Cs}), and the switch-controller block generates proper $SW_{1,3}$ signals for SVCM operation, in which P_3 acts as an active switch controlled by SW_3 (half-wave active rectifier) to charge C_s via the VM operation as long as $V_R > V_{Cs}$. For the CM operation, P_3 parasitic diode (D_3) provides the current path (similar to Re₁ operation).

When P_{Rx} is ultralow for $> 200 \mu s$ (intermittent WPT conditions), detected by sensing the V_R amplitude in the configuration-selection block, Re₃ is enabled to transfer the stored energy in C_s to C_L (Section II.B). In this chip, minimum T_1 and T_{sw2} are set to 90 ns and 950 ns, respectively, and in Re₃ the switch-controller block adjusts T_{sw2} to regulate V_L at 3 V. T_1 can also be adjusted externally. The bulk voltages (V_{B1-B4}) in each operation region and $V_{BGR} = 1.5$ V are generated by the body-biasing and BGR blocks, respectively.

For SVCM operation in both Re₁ and Re₂, T_{sw1} was fixed at $7 \mu s$ to achieve the switching frequency, $f_{sw1} = 1/T_{sw1}$, of 142 kHz. Based on our CM modeling in [15], for tens of microwatts to mW power levels ($R_L = 0.5\text{--}100$ k Ω) optimal f_{sw1} in CM operation for given inductive link parameters in Table I is within 200–500 kHz range (f_{sw1} increases with decreasing R_L). For small R_L (high P_L), P_{Rx} and consequently V_R should be high enough for proper operation, and therefore, SVCM mostly operates in VM ($6 \mu s$ in each T_{sw1}) rather than CM ($1 \mu s$ in each T_{sw1}). However, for large R_L (low P_L), P_{Rx} and consequently V_R can be small, and therefore, SVCM potentially operates only in CM in each T_{sw1} . Therefore, it is key for CM to be efficient at large R_L which is the basis for choosing low f_{sw1} of 142 kHz that led to higher PCE in circuit implementation compared with 200 kHz in modeling.

Fig. 11 shows the block diagrams and key operational waveforms of the switch-controller block. The Re_1 - Re_3 controllers in Figs. 11a and 11b receive the configuration-selection signal (Re_3) to accordingly generate intermediate control signals that are fed into SW_1 - SW_4 controllers in Fig. 11c to properly generate SW_{1-4} signals based on the SVCM and energy-recycling concepts. If Re_3 is low (no energy recycling), $Re_{1,2}$ controller in Fig. 11a is enabled. A time-base generator (TBG1), whenever is reset, outputs high after $4\ \mu s$ to enable the ZD_Comp1 comparator. Meanwhile, CP_1 and CP_2 comparators compare $0.5 \times V_L$ and $0.375 \times V_{CS}$ with $V_{BGR} = 1.5\ V$ to determine if V_L and V_{CS} have reached their targeted values of 3 V and 4 V, respectively. If CP_1 output is high in Re_1 ($V_L < 3\ V$) or CP_2 output is high in Re_2 ($V_{CS} < 4\ V$) or during startup (St : high), ZD_Comp1 is enabled by TBG1 to detect the time zero-crossing of V_R to consequently generate a sharp SW_1 - $Re_{1,2}$ pulse (SW_1 pulse in $Re_{1,2}$ regions) using a synchronization block. The synchronization block, including two cascaded D-flip-flops and an AND gate, counts three pulses (three rising edges of ZD_Comp1 output) to generate a rising edge, which is then converted to a short pulse (active low) with the width of 500 ns by the Pulse Gen-1 block. In addition, after three consecutive falling edges of ZD_Comp1 output, DFF1 outputs high to change the operation mode from VM to CM by controlling Mux1 output ($Mode$ signal), resulting in VM ($Mode$: low) for $6\ \mu s$ and CM ($Mode$: high) for $1\ \mu s$. After each $T_{sw1} = 7\ \mu s$, Pulse Gen-1 output resets all flip-flops and TBG1 for the same process to be repeated.

If Re_3 is high (energy recycling), Re_3 controller in Fig. 11b is enabled. Again, a time-base generator (TBG2) creates a rising edge after $T_{d2} = T_2 + T_{3,min} = 860\ ns$ upon reset. If CP_1 is high ($V_L < 3V$), Pulse Gen-2 generates a sharp SW_4 - Re_3 pulse (active low) with T_1 width. At the rising edge of SW_4 - Re_3 , SW_1 - Re_3 becomes high and ZD_Comp2 is enabled by DFF2 to detect the time zero-crossing of V_R . The falling edge of the SW_1 - Re_3 is created at the next positive edge of V_R to transfer the stored energy as i_{L2} to C_L and reset DFF2 for the next repeated T_{sw2} cycle. In Re_3 , for $V_L > 3\ V$ (CP_1 : low), Pulse Gen-2 outputs zero and no charge transfer will be occurred, automatically adjusting T_3 width to regulate V_L at 3 V.

In Fig. 11c, SW_1 and SW_4 are generated by either SW_1 - $Re_{1,2}$ or SW_1 - Re_3 and SW_4 - Re_3 or V_L , respectively, depending on the operation mode (Re_3). For SW_2 , during Re_3 or startup (St : high) or Re_1 with CM operation ($Mode$: high), in all of which P_2 should be off to use D_2 , Dc_1 becomes high to connect SW_2 to V_L . In Re_1 during VM ($Mode$: low), Asc_1 becomes high to connect SW_2 to the output of the Active_Switch_Comp1, comparing V_L with V_R to generate proper SW_2 pulses with controlled reverse current (using CP_1 output) for simultaneous rectification, self-regulation, an OVP. In Re_2 , SW_2 is connected to V_{h1} , which is the maximum voltage between V_L and V_R as shown in Fig. 12, to turn P_2 off. Similar to SW_2 , SW_3 is generated for charging C_s as shown in Fig. 11c.

Fig. 12 shows the body-biasing block that generates V_{B1-B4} according to the operation mode, as discussed before. A Max_Dect circuit, comprising of two series-connected PMOS transistors, detects maximum voltage between two inputs. In Fig. 12, transmission gates ($TG_{1,2}$), which pass large currents, use large transistors with the size of $8\ mm / 0.6\ \mu m$.

IV. MEASUREMENT RESULTS

Fig. 13 shows the ERSVCM chip micrograph fabricated in a 0.35- μm 2P4M standard CMOS process with an active area of 2.4 mm². A pair of planar Tx and Rx coils (L_1 and L_2) with specifications listed in Fig. 13 were fabricated on printed circuit boards (PCBs). A signal generator was used as the input source to drive the $L_1 C_1$ -tank at 1 MHz. The $L_2 C_2$ -tank and $C_L = 4.7 \mu\text{F}$ were connected to the chip.

Fig. 14 shows the measured transient waveforms of V_R and V_L for the SVCMM operation in Re₁ vs. the input power variation ($\sim V_{TX}$ in Fig. 1) at $R_L = 100 \text{ k}\Omega$. When V_{TX} was increased from 2.4 V_{p-p} to 4.7 V_{p-p}, the chip successfully provided $V_L = 3 \text{ V}$ with the safe $V_{R,peak}$ of 4.1 V. As shown in Fig. 14 inset for $V_{TX} = 2.4 \text{ V}_{p-p}$, since the steady-state $V_{R,peak}$ was as small as 2.2 V ($< 3 \text{ V}$ for VM operation), the chip operated only in CM with $f_{sw1} = 142 \text{ kHz}$ to charge C_L with a VCE of 1.4 V/V. For higher $V_{TX} = 4.7 \text{ V}_{p-p}$, resulting in higher received power, the chip mostly operated in VM with high PCE due to the large $V_{R,peak} > 3 \text{ V}$ and only operated for one cycle in CM in each T_{sw1} based on the SVCMM operation. The chip also employed the reverse current frequently to discharge C_L when $V_L > 3 \text{ V}$ and limited the maximum $V_{R,peak}$ to 4.1 V (OVP) by detuning the $L_2 C_2$ -tank with C_L . It should be noted that OVP occurred because C_s was already charged to 4 V.

Fig. 15 shows the measured transient waveforms of V_R , V_L , and V_{Cs} for the SVCMM operation in Re₂ with $C_L = C_s = 4.7 \mu\text{F}$ and initial $V_{Cs} = 0$. In this 500 μs time window, the chip charged C_s up to 3.8 V. At the beginning with small V_{Cs} , the chip continuously employed both VM (for 5 cycles) and CM (for one cycle) in each T_{sw1} to charge C_s . Fig 15 inset shows the results for charging V_{Cs} to 1.65 V with the limited $V_{R,peak}$ of 2.4 V and D_2 voltage drop of $\sim 0.75 \text{ V}$. For $V_{Cs} = 3.8 \text{ V}$ as shown in Fig 15 inset, the chip only employed CM to charge C_s because the steady-state V_R was smaller than 3.8 V. In this case, during CM operation $V_{R,peak}$ was 4.6 V, which was still within the safe region of $< 5 \text{ V}$ in this process.

Fig. 16 shows measured V_L , V_{Cs} , and V_R in the energy-recycling configuration (Re₃) without any input power ($V_{TX} = 0$) at $C_L = C_s = 4.7 \mu\text{F}$ and $R_L = 100 \text{ k}\Omega$. These waveforms match very well with the conceptual waveforms in Fig. 5b. During $T_1 = 100 \text{ ns}$, P_4 was turned on to transfer energy from C_s to the $L_2 C_2$ -tank (V_R jumped to 3.8 V at the beginning with $V_{Cs} = 4 \text{ V}$). During T_2 , P_4 and N_1/P_1 were turned off and on, respectively, and i_{L2} polarity changed. Then at the beginning of T_3 , N_1/P_1 were turned off that resulted in a sudden jump in V_R to $\sim 3.7 \text{ V}$ (i.e., $V_L + 0.7 \text{ V}$) to turn D_2 on and complete the charge transfer to C_L . Therefore, V_L remained constant at 3 V. In Fig. 16, minimum $T_{sw2} = 950 \text{ ns}$ was employed by the chip to transfer energy to C_L very frequently.

Fig. 17 shows measured V_R , V_{Cs} , and V_L in Re₃ for $C_L = C_s = 4.7 \mu\text{F}$ and $V_{TX} = 0$ (no input power), when $R_L = 5 \text{ k}\Omega$ was suddenly connected across C_L at the beginning of the trace. The chip could successfully transfer energy from C_s to C_L (V_{Cs} reduced from 4 V to 2.2 V) to maintain $P_L = 1.8 \text{ mW}$ for $\sim 2.75 \text{ ms}$ with only 0.1 V drop across V_L . Without energy recycling, V_L dropped by 0.1 V after 0.78 ms. Therefore, the proposed energy-recycling

technique extended the Rx operation time by 250%. The maximum power efficiency in energy recycling was measured 41% for $V_{C_s} = 4$ V.

Fig. 18 shows the complete chip performance in an intermittent WPT condition with drastic V_{T_x} changes between 0 and 5.3 V_{p-p} and the sudden addition of $R_L = 3$ k Ω ($C_L = C_s = 4.7$ μ F). At the beginning with large continuous $V_{T_x} = 5.3$ V_{p-p} and $R_L = 100$ k Ω , by operating in SVCMM with self-regulation and OVP the chip successfully regulated V_L at 3 V and then transferred the extra energy to C_s by charging it to $V_{C_s} = 4$ V. After ~ 2 ms of the trace beginning, V_{T_x} was switched between 0 and 5.3 V_{p-p} for ~ 0.5 ms, which had negligible effect on V_L and the chip continued operating in Re₁. Then V_{T_x} was intentionally reduced to 0 and $R_L = 3$ k Ω was added for ~ 0.65 ms to mimic a worst-case scenario. Since P_{R_x} was zero and extra load power was needed, the chip operated in Re₃ to keep V_L constant at 3 V by recycling energy from C_s to C_L (V_{C_s} reduced to 3 V). Then as V_{T_x} was increased to 5.3 V_{p-p} again, the chip started functioning in SVCMM (Re₁ and Re₂) to recharge C_s to 4 V, and regulate V_L at 3 V with OVP.

Fig. 19a shows the measured PCE and $V_{R,peak}$ of the ERSVCM chip during the SVCMM operation vs. R_L at $V_L = 3$ V and $C_L = 4.7$ μ F. A maximum PCE of 75% was achieved for $R_L = 0.5$ k Ω . The PCE was higher at smaller R_L , because the required $V_{R,peak}$ was higher, and therefore, the chip operated in VM as an efficient active rectifier for more cycles. At higher R_L with required smaller $V_{R,peak}$, the chip employed less-efficient CM more frequently leading to reduced PCE. Nonetheless, a high PCE of $> 64\%$ was achieved for a wide range of R_L 10 k Ω . In Fig. 19a, $V_{R,peak}$ was maintained within the safe region of < 5 V for all R_L values.

Fig. 19b shows measured PCE and V_L for different P_{R_x} (1.7–12.5 mW) at $R_L = 1, 2$ and 10 k Ω when the chip operated in SVCMM (no energy recycling). Since the chip needs at least $V_L = 2.6$ V to function properly, when P_{R_x} was not sufficient both V_L and PCE dropped to zero, which was expected. On the other hand, when P_{R_x} was too high, V_L remained constant at 3 V thanks to voltage regulation via the reverse current, but PCE reduced due to voltage regulation. Fig. 19b clearly shows that there is an optimal P_{R_x} at each R_L for achieving the highest PCE. For $P_{R_x} = 10.5$ mW and $R_L = 1$ k Ω , maximum PCE of 78.8% was achieved at $V_L = 2.8$ V.

Table II compares the performance of the proposed ERSVCM chip with the state-of-the-art IPMs. To the best of our knowledge, in inductive power delivery the ERSVCM chip is the first that employs the SVCMM operation along with energy recycling to extend the input-voltage range and Rx operation time for efficient, reliable, and safe WPT. In our proof-of-concept chip prototype, Rx operation time was extended by 250% at $R_L = 5$ k Ω by storing and recycling the surplus received energy. The chip achieved a maximum measured PCE of 75% for the SVCMM operation at $R_L = 0.5$ k Ω . The chip also performed simultaneous self-regulation and OVP using the reverse current in charging both C_L and C_s . The measured line and load regulation (defined as V_L / V_L) were 1.8% (steady-state V_R : 1.5 V, 3 V) at $R_L = 100$ k Ω and 0.8% (R_L : 0.5 k Ω , 100 k Ω) for $V_L = 3$ V, respectively. This chip only requires three off-chip capacitors for multiple functions including Rx resonance, rectification, regulation, OVP, and energy recycling. Compared with our VM-CM in [15], the ERSVCM

chip occupies more active area (2.4 mm^2) and requires one more off-chip capacitor, mainly due to the addition of the energy-recycling functionality. Considering only SVCMM, similar number of off-chip capacitors (only two) is required and the active area is only 1 mm^2 .

In this work, we used a 5-V process to demonstrate the feasibility of the proposed energy recycling technique. But to achieve the best of the proposed technique, one can 1) utilize a larger capacitor (or even a rechargeable battery) for C_s as a large energy reservoir, and 2) implement energy recycling in a higher voltage process to charge large C_s up to very high voltages, practically enabled by the SVCMM operation. This can result in gradually storing all the surplus P_{Rx} in a big reservoir and utilize it when needed even with a small C_L . In conventional IPMs, C_L can also be the large capacitor. However, no matter how large C_L is, it should only be charged to the designated regulated supply, which is typically low, and to maintain good load/line regulation, its voltage can only drop for tens of mV. Therefore, it still limits the continuous operation of the Rx. Moreover, using a large C_L can result in slow startup. These said, the tradeoff between improved performance and chip complexity should also be considered.

V. CONCLUSION

We have presented the theory, ASIC implementation, and measurement results of a new strategy for inductive power delivery in that the surplus received energy is stored on a storage capacitor (or a battery) as an energy reservoir to be recycled back into the load when the received power is inadequate. Utilizing both VM and CM operations with seamless transitions extended the safe input-voltage range, eliminating the dead zone in current IPMs. The proposed ERSVCM chip could extend the system operation time by 250% for $R_L = 5 \text{ k}\Omega$ thanks to the energy-recycling technique. In measurements, despite severe transmitted-power variations in a mimicked intermittent WPT scenario, the chip successfully achieved a regulated supply of 3 V by operating in CM with high VCE and employing energy recycling. With only one off-chip capacitor, rectification, regulation, and OVP have been achieved with the reverse current. The chip achieved a high PCE of 75% at the output power of 18 mW with measured line and load regulations of 1.8% and 0.8% in one-step self-regulation, respectively.

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Biography

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Fig. 1. Schematic diagrams of (a) the conventional inductive link with a rectifier and a regulator, and (b) the proposed inductive power-management scheme with energy recycling.

Fig. 2.

Safe operation region vs. steady-state V_R for different IPM structures. The proposed SVCM structure eliminates the dead zone (extended V_R range).

Fig. 3.

(a) Simplified circuit schematic of the proposed SVC structure, and (b) key conceptual waveforms of i_{L2} , V_R , V_L , and $SW_{1,2}$ for the SVC operation with simultaneous self-regulation and OVP.

Fig. 4.

(a) Simulated $V_{R,peak}$ vs. steady-state V_R for the conventional CM in [15] and the proposed SVCM. (b) Simulated PCEs vs. R_L for the VM-CM in [15] and the proposed SVCM ($V_L = 3$ V).

Fig. 5. (a) Simplified circuit schematic of the proposed energy-recycling technique, and (b) key waveforms, including i_{L2} , V_R , V_L , and $SW_{1,2,4}$, in the energy recycling operation.

Fig. 6. Simplified circuit model of the proposed energy-recycling technique in (a) region-I, b) region-II, and c) region-III.

Fig. 7. Simulated vs. calculated key waveforms of the proposed energy-recycling technique with perfectly matched results.

Fig. 8.
Simulated normalized charge transfer vs. T_1 and T_{sw2} for the proposed energy-recycling technique.

Fig. 9.

Simplified block diagram of the proposed energy-recycling seamless-voltage/current-mode (ERSVCM) chip with seamless transition between VM and CM, energy-recycling, self-regulation, and OVP capabilities over an extended input voltage range.

Fig. 10.

The chip operation algorithm for optimal switching between different operation regions to maintain V_L at 3 V regardless of P_{RX} variations.

Fig. 11.

Schematic diagrams and key operational waveforms of the switch-controller block: (a) Re₁ and Re₂ cont., (b) Re₃ cont., and (c) SW₁₋₄ cont..

Fig. 13.
Proposed ERSVCM IPM chip micrograph operating at 1 MHz and occupying an active area of 2.4 mm².

Fig. 14.

Measured transient waveforms of V_R and V_L vs. the input power ($\sim V_{Tx}$) variations at $R_L = 100 \text{ k}\Omega$ and $C_L = 4.7 \text{ }\mu\text{F}$ for the SVC operation in Re_1 .

Fig. 15.

Measured transient waveforms of V_R , V_L , and V_{Cs} for the SVCM operation in Re_2 with $C_L = C_s = 4.7 \mu F$.

Fig. 16.

Measured transient waveforms of V_R , V_L , and V_{Cs} in the energy-recycling configuration (R₃) with $V_{Tx} = 0$ at $C_L = C_s = 4.7\text{ }\mu\text{F}$ and $R_L = 100\text{ k}\Omega$.

Fig. 17.

Measured V_R , V_{Cs} , and V_L in the energy-recycling configuration (Re₃) when $R_L = 5 \text{ k}\Omega$ was added across C_L , demonstrating that the chip could maintain load power for 2.75 ms with small V_L drop of 0.1 V at $V_{Tx} = 0$.

Fig. 18.

Measured V_R , V_L , and V_{Cs} waveforms for the chip transitions between the SVCM (Re₁ and Re₂) and energy-recycling (Re₃) operations for an intermittent WPT condition with drastic V_{Tx} changes and R_L addition.

Fig. 19.

(a) Measured PCE and $V_{R, peak}$ vs. R_L during the SVCM operation at $V_L = 3$ V, and (b) measured PCE and V_L vs. P_{RX} for different R_L ($C_L = 4.7$ μ F).

TABLE I

CIRCUIT PARAMETERS USED IN THE ENERGY-RECYCLING MODELING AND SIMULATION

Parameter	Value	Parameter	Value
L_2 (μH)	4.2	C_L (nF)	100
$R_{L2}(\Omega)$	0.5	C_s (nF)	100
C_2 (nF)	6	f_p (MHz)	1
$R_{NI}/R_{PA}(\Omega)$	0.5	R_{D2}	0.5

BENCHMARKING OF THE ERSVCM CHIP AMONG STATE-OF-THE-ART INDUCTIVE POWER MANAGERMENTS

TABLE II

Publication	TPE-2014 [10]	ISSCC-2018 [16]	ISSCC-2015 [5]	ISSCC-2016 [13]	JSSC-2017 [15]	This Work
CMOS Technology (μm)	0.18	0.18	0.35	0.18	0.35	0.35
Operation Frequency (MHz)	13.56	13.56	2	0.05	1	1
Rx Architecture	VM	VM	CM	CM	VM-CM	SVCM
Energy Recycling	No	No	No	No	No	Yes
PCE (%) @ P_L (mW)	67.9 @ 19	67.8 @ 10	87 @ 220	61.2 @ 0.0028	VM: 77 @ 10	75 @ 18
Self-Regulation	No	No	No	- [*]	Yes	Yes
Line Regulation (%)	-	-	-	-	VM: 0.8 CM: 2.5	1.8
Load Regulation (%)	-	-	-	-	VM: 0.75 CM: 2.2	0.8
Dead Zone in Input-Voltage Range	Yes	No ^{**}	Yes	Yes	Yes	No
Over-Voltage Protection (OVP)	No	No	Yes	No	VM: Yes CM: No	Yes
Rx Operation-Time Extension (%)	-	-	-	-	-	250
# of Off-Chip Capacitors [†]	4	4	4	*	2	3
Output Power Range (mW)	6.4–32	2–50	50–1450	0.0006–0.0028 ⁺⁺	0.1–20	0.09–18
Active Area (mm^2)	~0.055	~1.25	~4.8	0.54	0.52	2.4

[†]For Rx resonance, rectification, regulation, OVP, and energy recycling.⁺⁺At Rx coil.^{*}Battery charger.^{**}Utilizing off-chip inductor.