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Stimulation and Artifact-suppression Techniques for in-vitro High-density Microelectrode Array Systems

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Abstract

We present novel voltage stimulation buffers with controlled output current, along with recording circuits featuring adjustable high-pass cut-off filtering to perform efficient stimulation while actively suppressing stimulation artifacts in high-density microelectrode arrays. Owing to the dense packing and close proximity of the electrodes in such systems, a stimulation through one electrode can cause large electrical artifacts on neighboring electrodes that easily saturate the corresponding recording amplifiers. To suppress such artifacts, the high-pass corner frequencies of all available 2048 recording channels can be raised from several Hz to several kHz by applying a “soft-reset” or pole-shifting technique. With the implemented artifact suppression technique, the saturation time of the recording circuits, connected to electrodes in immediate vicinity to the stimulation site, could be reduced to less than 150 μ s. For the stimulation buffer, we developed a circuit, which can operate in two modes: either control of only the stimulation voltage, or control of current and voltage during stimulation. The voltage-only controlled mode employs a local common-mode feedback operational transconductance amplifier with a near rail-to-rail input/output range, suitable for driving high capacitive loads. The current/voltage controlled mode is based on a positive current conveyor generating adjustable output currents, while its upper and lower output voltages are limited by two feedback loops. The current/voltage controlled circuit can generate stimulation pulses up to 30 μ A with less than $\pm 0.1\%$ linearity error in the low-current mode, and up to 300 μ A with less than $\pm 0.2\%$ linearity error in the high-current mode.

Index Terms

CMOS; high-density microelectrode array (HD-MEA); extracellular recording and stimulation; current/voltage controlled stimulation; pseudo-resistor; artifact suppression; soft reset pole-shifting

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I Introduction

Microelectrode arrays (MEAs) have been widely used in recent years for in-vitro examination of neuronal cells and neural networks. These MEAs enable long-term bi-directional interfacing with networks of living cells by providing extracellular electrical stimulation and electrophysiological recording features [1, 2]. Recent CMOS-based active MEA devices, especially high-density (HD) MEAs, provide the capability to simultaneously perform electrophysiological recordings from thousands of electrodes at cellular/subcellular spatial resolution [3–6]. The high spatio-temporal resolution of these devices enables better separation and assignment of neural activities for closely spaced neurons as well as very localized stimulation of single individual neurons [7].

Extracellular electrical stimulation of neurons using MEAs is achieved by, for example, applying potentials through electrodes in the vicinity of targeted neurons, thus altering their membrane potentials. Stimulus with proper amplitude and duration will cause depolarization of the neuron membrane and will evoke an action potential (AP) response [8]. Faradaic and non-Faradaic processes may occur during stimulation. In the case of a non-Faradaic process, charge redistribution in the double-layer capacitor, formed at the electrode/electrolyte interface, occurs. In the case of a Faradaic process, charge transfer and redox reactions may occur due to electron transfer at the electrode surface [9]. Faradaic processes may entail unwanted electrochemical reactions and formation of reactive species, which may lead to electrode degradation and production of compounds that are toxic to the cells [10]. Upon exceeding a safe potential window, determined by the electrode material, electrolysis may occur [9].

For electrical stimulation, either voltage-controlled or current-controlled circuits are used [11]. The voltage-controlled technique offers the advantage of being able to obviate Faradaic processes by precisely controlling the electrode voltage and maintaining it within a safe range. It, therefore, has been widely used with MEAs [12]. The generated current, however, depends on the electrode impedance, which may vary considerably due to fabrication variation or aging. This may cause variations in the volume of the tissue that is stimulated [13, 14]. Therefore it is desired to have a circuit which can accurately control the output current during the stimulation pulse.

Current-controlled stimulation features direct control over the electrode current [15] but do not provide any control over the electrode voltage, so that high electrode voltages can occur entailing unwanted electrochemistry, tissue damage, or electrode degradation. Mostly biphasic current pulses with opposite polarity in each phase are used, along with charge-balancing techniques to assure zero net charge transfer [16]. Charge balancing can be achieved using large blocking capacitors (several hundred nF) at the output of the stimulation circuit to block DC currents [17, 18]. As such large blocking capacitors cannot be integrated on chip, active charge balancing techniques have been developed, where either the offset current is regulated or a compensating charge is transferred to the electrode, upon detecting residual voltages after stimulation [19–21]. For very small MEA electrodes, featuring high impedance, the electrode voltage may rapidly reach the supply voltage, which

prevents the generation of balanced positive and negative current pulses, so that high-voltage compliance circuits have been developed [22–25].

An undesirable issue accompanying any type of electrical stimulation is the effect of the stimulation signals on the recording channels. Typically, recording channels are designed to detect electrophysiological signals with amplitudes from tens of μV to a few mV and frequencies from 1 Hz to 10 kHz, whereas the stimulation circuits generate signals with amplitudes of a few hundred mV. Such large amplitude signals can easily drive the recording circuits or channels that are connected to electrodes near the stimulation site into saturation and are known as “stimulation artifact”. The recording channels are normally designed with a very low high-pass cutoff frequency for filtering out low-frequency electrode potential drifts, so that the saturation state of the channels may last up to tens of milliseconds [26, 27]. If the recording channels are not saturated, digital signal processing methods, such as subtraction of the averaged artifact signal, can be utilized to detect action potentials [28–31]. However, when saturated, the recording channels cannot record any electrophysiological signals, so that hardware engineering techniques are needed to decrease this dead time and suppress the stimulation artifacts. Analog techniques and ASICs have been previously developed for artifact suppression in MEAs, such as disconnecting the recording channels or resetting them in a unity-gain feedback during the stimulation phase, or applying adaptive filtering [32–35]. Their application entails additional artifacts, as such techniques impose a rapid topological change in the recording channels during disconnection or reset.

In this paper, we present a new stimulation circuit, which forms part of a large integrated multifunctional system [6, 36], details of which, however, have not been presented previously. The stimulation circuit can work either in voltage-only controlled or current/voltage controlled mode. The current/voltage controlled mode provides continuous control over the current and voltage of the generated stimulation pulse by exploiting a similar technique as used in high-voltage compliance stimulation circuits [22–25]. Moreover, we present a technique to suppress stimulation artifacts either on all active readout channels or on the electrodes in immediate vicinity of less than $15\ \mu\text{m}$ to the stimulation site, a so-called “soft reset” or pole shifting technique, which temporarily increases the high-pass cut-off frequency of the signal amplification stages. This technique, which was, to the best of our knowledge, for the first time implemented in a CMOS HD-MEA system, can be applied to any arbitrarily selected subset of up to 2048 recording channels so that multiple stimulation sites (with different stimulation waveforms) can be used simultaneously, while the associated artifact can be suppressed on all active readout channels if necessary. Although pole shifting has been applied previously (e.g., in refs. [26, 27]), the developed soft reset technique is different from techniques that rely on switching or disconnecting of electrodes and recording amplifiers for discharging and reset [26–28, 32, 33] as will be detailed in Section III. These techniques produce additional artifacts in the recording channels due to the switching. The developed artifact suppression technique has not been previously described [6, 36] and will be explained and characterized in detail.

This paper is organized as follows. Section II briefly describes the overall multifunctional MEA system. Section III includes a detailed description of the stimulation buffers in the voltage-only controlled and the current/voltage controlled mode, as well as of the circuit

implementation of the artifact-suppression or soft-reset technique. In Section IV, the electrical characterization results of those units are summarized. Section V shows biological measurement results, acquired by exploiting the implemented stimulation circuit and artifact suppression technique, and Section VI concludes the paper.

II System Overview

The developed stimulation buffers and recording channels form part of a recently developed multifunctional HD-MEA microsystem [6, 36]. The system chip includes a large sensing area of $4.48 \times 2.43 \text{ mm}^2$ comprising 59'760 ($= 332 \times 180$) electrodes of $3 \times 7.5 \text{ }\mu\text{m}^2$ size at a pitch of $13.5 \text{ }\mu\text{m}$. The system incorporates several types of sensing units with the aim of extracting a wide spectrum of information from the same neuronal culture or brain slice. The overall HD-MEA system includes 16 dual-mode stimulation buffers (can be configured in the voltage-only or current/voltage controlled mode), 2048 action-potential recording channels, 32 local-field-potential recording channels, 32 current recording units, 32 impedance measurement units and 28 neurotransmitter detection units. The integrated input-referred noise of an AP recoding channel, including the ADC, was $2.4 \text{ }\mu\text{VRMS}$ in the AP band (300 Hz–10 kHz), and $5.4 \text{ }\mu\text{VRMS}$ over the full band (1 Hz–10 kHz) [6]. A switch-matrix approach has been used to route different measurement/stimulation buffers to arbitrarily selectable electrodes or subsets of electrodes. Fig. 1 shows the block diagram of the whole system. Both, AP and LFP recording channels are equipped with stimulation artifact suppression capability. In this paper, we will focus on the stimulation buffers and the artifact suppression technique that have not been detailed previously.

The 16 dual-mode stimulation buffers are grouped in two blocks of 8 buffers. Three digital/analog converters, DAC_0 to DAC_2 , are shared among all buffers in each block to generate arbitrary stimulation pulses. As shown in Fig. 1, all stimulation buffers can work in two modes: (1) by closing the switches labeled with “V”, voltage-only controlled stimulation is achieved; (2) by closing the switches labeled with “IV”, current/voltage controlled stimulation is achieved. OTA_{VBuf} is a near rail-to-rail operational transconductance amplifier (OTA), which is used in both operating modes. In the voltage-only controlled mode, OTA_{VBuf} is configured in unity-gain feedback, whereas in the current/voltage controlled mode, it works as the buffer part of a positive current conveyor of type II (CCII+). During stimulation, this current conveyor generates tunable output current pulses, which are delivered to the stimulation electrode. The upper and lower bounds of the electrode voltage are controlled by two voltage limiters, whose threshold voltage are set by two digital/analog converters, DAC_3 and DAC_4 , respectively. All the mentioned DACs (DAC_0 - DAC_4) are resistor-ladder DACs featuring 10-bit resolution.

2048 AP recording channels have been integrated on the chip. Each channel consists of 4 fully-differential amplification stages. The first two stages employ MOS transistors, biased in the weak inversion region, called pseudo-resistors, to realize very high resistances in the range of $T\Omega$. Using these pseudo-resistors together with the AC-coupling input capacitors, a very low high-pass cut-off frequency (tens of mHz to a few Hz) has been achieved to filter out low-frequency electrode potential drifts. In addition, during stimulation, the gate voltages of these MOS transistors can be adjusted in a way that their resistances are two to

three orders of magnitude smaller than their normal value. Thus, the recording channels can recover very quickly after stimulation, a feature that will be elaborated in more detail in the next section.

III Circuit Implementation

A Near Rail-to-Rail OTA for the Voltage-Only Controlled Stimulation Mode

The implementation of the stimulation buffer included the design of a near rail-to-rail OTA for the voltage-only controlled mode. For this stimulation mode, the buffer has to drive a large capacitive load of one or several electrodes (up to nF range) while consuming low quiescent power.

Given the large electrode capacitance, a two-stage Miller-compensated opamp would not be a suitable choice for this application due to the necessity of using a large Miller capacitor to keep the opamp stable. Therefore, an OTA topology with a dominant pole at the output was chosen, as such topology is more stable for large electrode capacitances. For OTAs, a large gain is achieved by having a high output resistance, so that resistive loads can substantially degrade the gain. For the voltage-only controlled stimulation mode, the OTA is configured as unity-gain feedback, eliminating the necessity to use feedback resistors. To have the ability to generate high-amplitude stimulation pulses (the supply voltage is limited to 3.3 V), the OTA needs to have a near rail-to-rail output swing, which, in turn, requires the same common-mode input range due to the unity-gain feedback.

Fig. 2 shows the schematic of the proposed OTA. Its near rail-to-rail input/output range is achieved as follows; the common-mode input voltage is sensed by M_7 and M_8 . M_7 and M_8 then set the gate voltages of M_{12} and M_{13} , which, in turn, control the drain voltages of the input transistors M_1 - M_4 . When the input common-mode voltage is close to V_{DD} , M_3 and M_4 are turned off, but the drain voltages of M_1 and M_2 remain high to keep them in saturation. In contrast, upon applying an input common-mode voltage close to ground, the drain voltages of M_3 and M_4 are sufficiently low to keep them in saturation while M_1 and M_2 are turned off. The local common-mode feedback technique [37] has been adopted by adding the resistors R_1 and R_2 in the OTA to provide a large output current with a low quiescent current. The use of this technique also increases the gain-bandwidth product (GBW) significantly.

B Current Conveyor with Output Voltage Limiters for the Current/Voltage Controlled Stimulation Mode

For the voltage-only controlled mode, the voltage level of the stimulation pulse is precisely controlled, but the output current delivered to the electrode is not controlled. The maximum output current of the OTA for the voltage-only mode can be controlled by adjusting its bias current [27], however, the relationship between maximum output current and bias current is nonlinear, so that the control would be poor. To achieve better control over both output voltage and current, we improved the current conveyor reported in [38] and developed a new design, illustrated in Fig. 3.

The proposed stimulation buffer incorporates a CCII+ that converts the input DAC voltage into a corresponding output current. The same OTA, OTA_{VBUF} , was reused for this mode as well, and the resistors R_3 and R_4 have been added in parallel to R_1 and R_2 to decrease current boosting and the OTA's gain. According to simulations, R_3 and R_4 decrease the gain by 13 dB and increase the phase margin from 15° to 70° . Meanwhile, R_{IN} has a value of 50 k Ω , so that a $\pm 30 \mu A$ current is generated upon applying ± 1.5 V through the DACs. This current flows into the current conveyor where it is then mirrored to the output branch and delivered to the electrode. The circuit features a low- and high-current mode. In the low-current mode, the generated current is directly mirrored to the output, whereas, in the high-current mode, M_{29} and M_{33} are connected to the output branch by closing the switches S_3 and S_4 . M_{29} and M_{33} are ten times larger than M_{28} and M_{32} , and therefore, the output current can become as large as $\pm 330 \mu A$ without increasing the quiescent current in the first two branches of the current conveyor.

OTA_{UP} , M_{31} and OTA_{DN} , M_{30} form two independent feedback loops to control the electrode voltage (V_{EL}). The OTA_{UP} , M_{31} feedback loop is triggered when $V_{EL} > V_{UP}$, and the OTA_{DN} , M_{30} feedback loop is triggered when $V_{EL} < V_{DN}$. Whenever one of the two feedback loops is triggered, the output current is nearly turned off, and only a small bias current is still flowing. This bias current keeps the feedback loop active and continuously regulates V_{EL} to be fixed either at V_{UP} or V_{DN} . The current/voltage controlled mode yields similar voltage stimulation pulses as the voltage-only controlled mode, however with adjustable and controllable output current.

C Pseudo Resistors and Stimulation Artifact Suppression

A simplified schematic of the AP recording channel is shown in Fig. 4. A description of its overall design can be found in [6], so that we will here focus on the design of the pseudo resistors and the stimulation artifact suppression features. As already mentioned, each AP recording channel includes four fully-differential gain stages. The first stage employs an open-loop topology with resistive loads to achieve low noise. The second stage includes a closed-loop structure to have an accurate gain and to provide anti-aliasing filtering at 7 kHz. Both, the third and fourth stages have been realized with switched-capacitor amplifiers to handle a large signal swing and implement 8-to-1 multiplexing. Finally, every 64 neural signals are sampled at 20 kS/s and digitized by a 10-bit successive-approximation register (SAR) analog/digital converter (ADC), capable of converting at 1.28 MS/s. The digital data is sent off chip and processed by a field-programmable gate array (FPGA).

Pseudo resistors, normally realized with MOS transistors, biased in the weak inversion region, play an important role in realizing the two first-order high-pass filters (HPFs) in front of the first and the second stage, as shown in Fig. 4. In the first stage, the HPF (C_1 and R_{PR1}) eliminates the low frequency drifts of the electrode potentials. In the second stage, the HPF (C_3 and R_{PR2}) removes the offset of the first stage, avoiding saturation of the whole amplification chain. Both HPFs should have very low cutoff frequencies (< 10 Hz) in order not to distort the AP signals. As the capacitors are limited to around a few pF due to area constraints, the pseudo resistors (R_{PR1} and R_{PR2}) need to feature large enough resistances (in the T Ω range).

Although conventional pseudo-resistor structures can achieve such large resistances, the resistance spreads are large due to process and temperature variations. To overcome this drawback, we devised two novel structures [6, 39], shown in Fig. 4. R_{PR1} consists of a PMOS and an NMOS transistor, connected like a transmission gate and biased by a PMOS and an NMOS current mirror. R_{PR2} includes two NMOS transistors connected in series, whose gate voltages are biased with an NMOS-only level shifter, improved from a structure using a PMOS level shifter [40] for better process tracking. In both structures, the first-order dependence of the overdrive voltages of the transistors in R_{PR1} and R_{PR2} on their threshold voltages is cancelled out, which results in a much smaller resistance spread compared to conventional structures.

In addition, the resistances of R_{PR1} and R_{PR2} can be easily adjusted through their bias currents. Therefore, the high-pass cutoff frequencies can be tuned to compensate for process and temperature variations and to accommodate different experimental scenarios. This feature is further exploited in this work to suppress stimulation artifacts. Shortly before stimulation, the bias currents of the pseudo resistors are set to much higher values than during normal operation, so that the high-pass cutoff frequencies are increased to the kHz range. As a result, the gains of the first two stages are reduced to an extent that these two stages are not saturated during stimulation and their operating points are preserved. In addition, the time constants associated with the two HPFs became small (in the 100 μ s range), so that, right after stimulation, the recording channels quickly recover and record neuronal signals. We call this technique, which is based on pole-shifting, “soft reset”, as the amplifier is gently reset. This “soft-reset” technique can be applied to any arbitrarily selected subset of recording channels, as the respective suppression features are implemented in all 2048 recording channels that can be simultaneously used. The soft reset technique presented here is clearly different from techniques, which include switching or disconnecting of electrodes and recording amplifiers for charge injection, discharging or reset [26–28, 32, 33]. These techniques reported in [26–28, 32, 33] include to remove stimulation artifacts from or discharge the stimulating electrode itself. As we have a much larger density of electrodes in the array (5490 electrodes/mm²) in comparison the reported systems [26–28, 32, 33], and as each neuron produces signals on approx. 20-40 electrodes, we did not attempt to recover signals on the stimulation electrode itself. Although pole shifting also was applied in [26, 27], it was only the last of a total of three steps including (i) disconnection of the recording amplifier during stimulation, (ii) reconnection of the amplifier and connection of a low-impedance discharge path to approximately restore the original situation and (iii) connect high-impedance discharge path and simultaneously apply pole-shifting to the feedback resistor. Any procedure or technique that is based on switching produces additional artifacts in the recording channels as a consequence of the switching operation, which is not the case for our developed soft-reset technique that only relies on precisely timed transient pole-shifting.

IV Electrical Characterization

The multifunctional MEA chip, including the stimulation buffers and AP recording channels, has been fabricated in an industrial 0.18- μ m 1P6M CMOS technology, followed by in-house post-processing to deposit the platinum electrodes. A shifted-electrode design

and the application of a silicon nitride/silicon oxide passivation stack was used to protect the circuitry in the chip against liquids and metabolic products of the cell cultures and to prevent toxic materials from being released by the chip into the cell medium [2].

Fig. 5 shows a chip micrograph with the floorplan of the different measurement blocks. The electrode array is in the center of the chip. The 2048 AP recording channels are placed on the top and bottom side of the chip, while the rest of the measurement units are placed at the left and right side in a symmetrical arrangement. The chip was wire-bonded to a four-layer packaging printed circuit board (PCB), which was partitioned into analog and digital sections to prevent noisy digital signals from contaminating sensitive analog signals. A glass ring was glued on the packaging PCB to contain the cell culture medium. Finally, epoxy was used to cover the bonding wires while leaving the electrode array area open to interact with the cells and liquid phase.

To evaluate the performance of the chip, a measurement setup has been developed, including: (1) A custom-designed supporting PCB to generate bias voltages and clock signals and to provide the test input/output connections. On the supporting PCB, a USB controller (FT245RL) and an FPGA (Spartan-3E, Xilinx Inc., San Jose, USA) were mounted to fetch and buffer the configuration commands and to transmit them to the chip with precise timing (less than 1 μ s delay between commands); (2) A data acquisition (DAQ) Card (NI PXIe-6544, National Instruments, Austin, USA) was used to acquire the digital data from the chip and send them to a PC for online visualization and data storage.

For characterization of the stimulation buffer in the voltage-only controlled mode, a 500 pF external capacitor in parallel with a 1 M Ω resistor were used as load, which emulated a Pt-black electrode. The measured impedance of the Pt-black electrodes of the array (electrode size: 3 x 7.5 μ m²) was 450 k Ω with a phase angle of 55 degrees in the kHz range [6]. The electrode-electrolyte interface of bright and Pt-black (30–40 fold reduction of impedance magnitude) electrodes had been characterized in physiological saline between 1 Hz and 1 MHz (see Fig. 1 in Supplement) [6]. In the frequency range from 10 Hz to 10 kHz the impedance showed 1/f roll-off characteristics and predominantly capacitive behavior as evidenced by phase angles of 60°–80°. At frequencies over 10 kHz, the spreading resistance started to dominate the impedance.

A biphasic ± 1 V voltage pulse, centered around 1.65 V (the voltage of the reference electrode), was generated using the on-chip DACs and applied to the buffer. The output voltage and output current of the buffer are shown in Fig. 6.a and 6.b, respectively. The maximum output currents, obtained with 4 μ A, 6 μ A, and 8 μ A bias currents, were approximately 85 μ A, 190 μ A, and 315 μ A. Fig. 6.c shows the linearity analysis results. The buffer featured a 10-bit linearity for a voltage range of ± 1.45 V relative to the common-mode voltage of 1.65 V, which was 200 mV away from the power supply and ground rails. The open-loop characteristics of the buffer included a DC gain of 74 dB, a unity gain bandwidth of 75 kHz and a phase margin of 89° for a bias current of 4 μ A; and a DC gain of 77 dB, a unity gain bandwidth of 200 kHz and a phase margin of 82° for a bias current of 8 μ A, simulated with a capacitive load of 500 pF. The measured quiescent power consumption

of the OTA and the biasing circuitry was 105 μW for a bias current of 4 μA and 225 μW for a bias current of 8 μA . The buffer occupied an area of 0.011 mm^2 .

Fig. 7 shows the characterization results of the stimulation buffer, configured in the current/voltage controlled mode. The input voltage to the current conveyor was generated using the on-chip DACs, and its output current was adjusted to $\pm 20 \mu\text{A}$ and $\pm 100 \mu\text{A}$ using the low- and high-current modes, respectively. The current pulses were programmed to include 80 μs of positive currents and 80 μs of negative currents. The lower voltage limit (V_{DN}) was programmed to be 1.65 V, while the upper voltage limit (V_{UP}) was set to 2.65 V so that the output voltage swing was constrained to 1.0 V in order to generate a 1.0 V monophasic stimulation pulse. The load was again an external 500 pF capacitor. The DAC's output voltage, the output current, and the output voltage of the generated pulses for all these configurations are shown in Figs. 7.a and 7.b. It can be seen that the output currents were automatically switched off by the two feedback loops, when the output voltage reached the two programmed voltage limits. It is evident by comparing Fig. 7 with Fig. 6 that the current/voltage controlled stimulation mode provides more accurate control over the output current than the voltage-only controlled mode. Figs. 7.c and 7.d show the linearity measurement results of the current conveyor in the low- and high-current mode. The low-current mode features less than $\pm 0.1\%$ linearity error for a $\pm 30 \mu\text{A}$ output current, and the high-current mode has less than $\pm 0.2\%$ linearity error for a current range of $\pm 300 \mu\text{A}$. The measured quiescent power consumption of the stimulation buffer was 251 μW and 306 μW in the low- and high-current mode, respectively, including the corresponding biasing circuitry. A single buffer occupied an area of 0.046 mm^2 .

To evaluate the influence of the soft reset or pole shifting technique on the high-pass cutoff frequencies (f_{HPF}) of the first- and second-stage amplifiers, a 10 mV sinusoidal chirp signal from 0.1 Hz to 100 kHz was applied to the action potential (AP) recording channels, and the frequency responses of the first two amplification stages were recorded. Fig. 8 shows the measured transfer functions of the first two amplification stages, with and without activating the soft reset technique. The overall high-pass cutoff frequency was increased from 15 Hz to 4.23 kHz (Fig. 8) by the application of soft reset.

V Results of Biological Experiments

For all bio-measurements, dissociated cortical neurons (E18 Wistar rats) were cultured for 3-4 weeks on top of the MEA chips prior to the recordings. All experimental animal protocols were approved by the Basel-Stadt veterinary office according to Swiss federal laws on animal welfare and were carried out in accordance with the approved guidelines. The experiments were conducted under controlled environmental conditions inside an incubator at 37 °C and 5% CO_2 .

To effectively elicit electrical activity of single cells, the stimulation site should be close to an axon of a targeted cell [7]. For our experiments in the current/voltage-controlled stimulation mode, a stimulation electrode at a distance of 192 μm (approx. 14 electrodes) from the cell soma of interest was selected. The application of stimulation pulses, with sufficiently large voltage and current amplitudes (biphasic pulse of $\pm 450 \text{ mV}$ voltage

amplitude and 6 μA current amplitude) to this electrode evoked APs in the targeted neuron. The recorded data are shown in Fig. 9.a, and a consistently low jitter between the stimulation pulses and the recorded APs indicates that these APs were indeed evoked by the stimulation pulses. For comparison, we also included a trace of spontaneous activity in the Supplemental material. Like the signal displayed here, spontaneous APs feature characteristic first negative, then positive signals with amplitudes in the 300 μV range and durations between 2-3 ms (onset to end of signal). More spontaneous activity can be seen in [6]. The recording electrode near the cell soma was more than 5 inter-electrode distances away from the stimulation electrode (see Fig. 10), therefore, the recording channel was not driven into saturation, and artifact suppression was not required for this experiment. By decreasing the current or voltage amplitude of the stimulation pulse, the probability of evoking an AP decreased. Fig. 9.b shows the result of decreasing the voltage amplitude to ± 400 mV and the current amplitude to 1 μA . A total gain of 1024 was configured for the recording channels for these measurements (1st and 2nd stage=16x, 3rd stage=4x and 4th stage=1x).

To study the stimulation probability for different current and voltage levels, a set of biphasic stimulation pulses was generated and applied to the stimulation electrode, and the response of the targeted neuron to these pulses was recorded. The current/voltage controlled stimulation buffer, configured in the low-current mode, was used to generate biphasic stimulation pulses at 4 different current settings of 0.7 μA , 1 μA , 3 μA , and 6 μA . The voltage amplitude of the biphasic pulses was configured to fall within a range of ± 250 mV to ± 500 mV and was increased in steps of 5 mV. For each current/voltage value, 10 stimuli were applied, and a stimulation probability was calculated as the percentage of successfully evoked action potentials. This stimulation protocol was repeated 5 times to obtain an average stimulation probability for each current/voltage value, and a sigmoid curve was fitted to the data (Fig. 9.c).

The data indicate that a larger voltage amplitude of the stimulation pulse was required to evoke action potentials at low output current settings. This was likely due to the increase of the rise/fall time of the pulse caused by lower current levels. When the current was large enough to cause a steep slope in the pulse, a further increase of the current did not significantly improve the stimulation efficiency any more. The stimulation efficiency, under these conditions, was solely dependent on the voltage amplitude of the biphasic pulse.

To test the effectiveness of the soft-reset technique in suppressing stimulation artifacts, an AC signal of a frequency of 1 kHz was applied to the medium and a ± 400 mV biphasic stimulation pulse with 200 μs for each phase was applied to an electrode. The 1 kHz AC signal was applied to the bath to find out, how fast this reference signal could be recorded upon and after applying the stimulation pulse. The respective stimulation pulse was generated by using the on-chip DACs, and the stimulation buffers were configured in the voltage-only controlled mode. The responses were recorded with and without application of the soft reset feature. Fig. 10.a shows that the soft reset technique could substantially reduce the dead time of the recording channels, which were connected to electrodes immediately neighboring the stimulation site (inset in Fig. 10a). The close-ups (Fig. 10.b) show the response of the recording channels in 10.a immediately before and after stimulation, with and without application of the soft reset. The soft reset was activated 100 μs before issuing

the stimulation pulse and released 150 μ s after the pulse. The recording channels were available for recording right after the release of soft reset, and no switching artifact was visible in the signals. The exact activation and release period of the soft reset depends on several parameters, such as electrode impedance, stimulation pulse amplitude and gain/cut-off frequency of the recording channels. Fig. 10.c shows two time-series of recorded electrical images using the electrodes immediately surrounding the stimulation site and affected by stimulation artifacts. Responses are shown for a 13×11 electrode configuration with the stimulation electrode in the center. The locations of the electrodes are marked with dots in the last image of each row.

The top-row images were obtained from measurements without applying the soft reset, whereas the bottom row shows measurements with application of the soft reset. The top-row images show that the stimulation pulse affected electrodes within a radius of 67.5 μ m (5 electrodes) and lasted for more than 10 ms. The bottom row shows the effectiveness of the soft reset technique in suppressing the stimulation artifacts. Although some offset was superimposed on the recorded response, the channels recovered very quickly from saturation upon application of the soft reset so that it is possible to record signals even on electrodes immediately adjacent to the stimulating electrode at less than 15 μ m distance. The remaining offset could be further reduced by digital filtering of the recorded data.

To evaluate the performance of the artifact suppression on neuronal recordings, two electrodes near an active and spontaneously firing neuron were selected for stimulation and recording (Fig. 10.d). Large numbers of spontaneous action potentials and stimulated activity waves propagating through neural networks have been shown in [6]. Biphasic stimulation pulses (± 450 mV) were generated using the stimulation buffers in the voltage-only mode. The responses of the selected recording electrode with and without application of the soft reset are illustrated in Fig. 10.e. The resulting large neuronal spikes are likely to be the post-synaptic action potentials, according to their delay with respect to the stimulation event. The consistency in the occurrence of small signals (shown in the inset of Fig. 10.e) that could be recorded immediately after the stimulation evidenced the efficiency of the artifact suppression technique. Such small signals immediately after the stimulation would otherwise remain undetectable due to the saturation of the recording channels. The configured gain of the recording channels was 1024 for Figs. 10.a and 10.b and 2048 for Figs. 10.c to 10.e.

VI Conclusion

Details of CMOS circuits for electrical stimulation of electrogenic cells and a stimulation artifact suppression technique have been presented. The circuits have been integrated into a multifunctional HD-MEA system. While most of the stimulation circuits are based on either voltage-controlled [34, 41, 42] or controlled current excitation [4, 16, 43], this work aimed at developing a circuit where the output level of current and voltage can be independently adjusted. The reported stimulation buffers here generate stimulation pulses with more than 9 bit linearity. The stimulation-artifact-suppression technique was, to the best of our knowledge, for the first time implemented in HD-MEA systems. It was implemented in the amplifiers of all 2048 recording channels and decreased the recovery time of the AP

recording channels, connected to the electrodes adjacent to the stimulation site (i.e., at less than 15 μm distance), to 150 μs without any switching-induced artifacts. No effort was undertaken to recover the signal on the stimulation electrode itself due to the large available electrode density, which ensures the simultaneous recording of any individual neuronal action potential by more than 40 electrodes. The performed biological measurements with cultured neurons showed the dependence of neuronal excitability on current and voltage levels of the biphasic stimulation pulses. The possibility of applying controlled current and voltage stimulation pulses, along with the possibility to record neuronal responses 150 μs after stimulation and in immediate vicinity to the stimulation site, provide excellent means to gain a better understanding of extracellular electrical stimulation mechanisms.

Supplementary Material

Refer to Web version on PubMed Central for supplementary material.

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Fig. 2.
Schematic of the proposed near rail-to-rail Operational Transconductance Amplifier (OTA)
for the voltage-only controlled stimulation mode. All the transistor sizes are in μm .

Fig. 3.

Schematic of the proposed stimulation buffer. The switches marked with “V” are used for configuring the buffer into the voltage-only controlled mode and those marked with “I/V” are used for configuring the buffer into the current/voltage controlled mode.

Fig. 4. Schematic of the pseudo-resistors for implementing the soft reset feature in the first and second stage amplifiers of the Action-Potential (AP) recording channels.

Fig. 5. Micrograph of the multifunctional High-Density Microelectrode Array (HD-MEA); the die size is $12 \times 8.9 \text{ mm}^2$.

Fig. 6.
Characterization of the stimulation buffer working in the voltage-only controlled mode.

Fig. 7.

Characterization of the stimulation buffer in the current/voltage controlled mode. Output response for the low-current mode (a) and the high-current mode (b) with the voltage limiters set to 2.65 V for V_{UP} and 1.65 V for V_{DN} (indicated with arrows at V_{OUT} signals). Linearity analysis for the low-current mode (c) and the high-current mode (d).

Fig. 8.

Characterization of the transfer functions for the first two stages of the recording channels with/without applying the soft reset. Applying the soft reset increased the overall high-pass cutoff frequency from 15 Hz to 4.23 kHz.

Fig. 9.

Probability of evoking spikes for different current and voltage values of the stimulation pulses. Successfully evoked activity by applying stimulation pulses with sufficiently large voltage and current amplitudes (a). By decreasing the current or voltage amplitudes of the stimulation pulses, the probability of evoking activity drops (b). Comparison of the stimulation efficiency of the applied biphasic pulses at 4 different current levels and voltage amplitudes from ± 250 mV to ± 500 mV in 5mV steps (c).

Fig. 10.

Stimulation artifact suppression using the proposed soft-reset technique: Recorded traces around a stimulation site with and without applying the soft reset (a). Zoom-in around the stimulation time (b). The soft reset starts 100 μs before the stimulation pulse and ends 150 μs after the pulse. Two time series of electrical images in response to a ± 400 mV stimulation pulse (c). Top row: No artifact suppression was applied. The saturation of recording channels due to stimulation artifact is observed within a radius of up to 5 electrodes ($67.5 \mu\text{m}$) away from the stimulation site. Bottom row: The soft reset technique was applied for

artifact suppression. The last frame in each row depicts the locations of the recording electrodes (black dots). Location of neurons on top of the electrode array and positions of the selected electrodes for stimulation and recording around an active cell (d). Recorded spikes upon stimulation with and without application of the soft reset (e).