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Fabrication of Flexible Superconducting Wiring with High Current-Carrying Capacity Indium Interconnects

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Abstract

The X-ray integral field unit (X-IFU) is a cryogenic spectrometer for the Advanced Telescope for High ENergy Astrophysics (ATHENA). ATHENA is a planned next-generation space-based X-ray observatory with capabilities that surpass the spectral resolution of prior missions. Proposed device designs contain up to 3840 transition edge sensors, each acting as an individual pixel on the detector, presenting a unique challenge for wiring superconducting leads in the focal plane assembly. In prototypes that require direct wiring, the edges of X-IFU focal plane have hosted aluminum wirebonding pads; however, indium (In) ‘bumps’ deposited on an interface layer such as molybdenum nitride (MoN) can instead be used as an array of superconducting interconnects. We investigated bumped MoN:In structures with different process cleans and layer thicknesses. Measurements of the resistive transitions showed variation of transition temperature T_c as a function of bias and generally differed from the expected bulk T_c of In (3.41 K). Observed resistance of the In bump structures at temperatures below the MoN transition (at 8.0 K) also depended on the varied parameters. For our proposed X-IFU geometry (10 μm of In mated to a 1- μm In bump), we measured a minimum T_c of 3.14 K at a bias current of 3 mA and a normal resistance of 0.59 m Ω per interconnect. We also investigated the design and fabrication of superconducting niobium (Nb) microstrip atop flexible polyimide. We present a process for integrating In bumps with the flexible Nb leads to enable high-density wiring for the ATHENA X-IFU focal plane.

Keywords

Indium interconnects; Superconducting flexible wiring; X-IFU

1 Introduction

The Advanced Telescope for High ENergy Astrophysics (ATHENA) is an upcoming ESA space-based X-ray observatory with a planned NASA contribution for the mission. Its focal plane will contain the X-ray integral field unit (X-IFU), a cryogenic spectrometer [1]. The detector's pixels are transition edge sensors (TES), which require up to 10 mA of supercurrent-carrying capacity, I_c , at the operating temperature of 100 mK, for onboard characterization and calibration. In our planned prototype, each pixel requires two readout wires, for up to 7680 total connections. All connections within the focal plane must have sufficient I_c to enable calibration.

This study aimed to identify processes and techniques that meet the supercurrent-carrying capacity requirement with high yield and fabricability. As seen in Fig. 1, a direct-wired X-IFU prototype has the focal plane's edges lined with aluminum (Al) wirebonding pads; flexible superconducting wiring (FLEX) is used to carry signal around the corner to the bias circuits and amplifiers on each side of the fixture. We pursued the replacement of the wirebonds on the hexagonal detector chip (HEX) with arrays of indium (In) 'bumps' deposited on molybdenum nitride (MoN) film, which can instead be used as superconducting interconnects. Full replacement requires the integration of the In bumps with the FLEX.

Starting with proven structures from the Submillimeter Common-User Bolometer Array II (SCUBA II)/Raytheon process and the James Webb Space Telescope (JWST) Microshutter assembly, we varied In film thicknesses and interface cleans to examine how superconducting properties change with the process used [2, 3]. Additionally, with superconducting joints, a post-annealing step with temperatures approaching the melting point of In has been used for single-sided bump processes [4]. Typical X-ray detector absorber materials may also oxidize or interdiffuse at high temperatures; thus, we required that the assembly of the In bumps not use a post-annealing step. We also restricted our process by the geometry of the absorbers, which are cantilevered and stand 5-10 μm above the focal plane. Since In is integrated into the detector plane prior to the absorbers, we required that the In thickness on that side of the bump assembly be less than 5 μm (the minimum absorber height). We tested In bump thicknesses of 10 and 1 μm mated in 10:10 and 10:1 arrangements.

For our resulting In bump geometries, we measured critical temperature T_c , onset of resistance temperature T_o , and normal resistance R_n while varying bias current. Here, we present the results of our electrical characterization of the FLEX and of the two types of In bump circuits. We also report on our progress toward the fabrication of flexible superconducting niobium (Nb) microstrip with integrated In bumps.

2 Fabrication

2.1 Indium Bump Fabrication

We describe the fabrication of In bump array coupons to evaluate the yield and supercurrent-carrying capacity in a double-sided bump process. Test arrays of In bumps were fabricated

on 4" oxidized silicon wafers with a patterned MoN layer, yielding five chips from each wafer. Among several wafers, we varied the fabrication method through changes to the thickness of thermally evaporated indium, the surface clean power and method on MoN prior to In deposition, and the surface clean on the In bump surfaces prior to bump bonding. While each bump array (10 and 1 μm thicknesses) was patterned using the same mask, some variation in the bump dimensions arose from the varied cleans. This has been measured and calibrated.

To create the In features, positive photoresist was oven-baked, exposed, and image-reversed in an ammonia (NH_3) oven prior to developing. Image reversal provided the best undercut profile for the thick In film liftoff. We then evaporated In to two different thicknesses (10 and 1 μm), utilizing two different argon (Ar) plasma cleans for the MoN pads. For the 10 μm bumps, 250 or 800 V was applied to the anode during the clean, while the 1 μm wafer received an 800 V clean. The process was completed via an overnight liftoff in acetone. The results of the differing cleans and thicknesses following In liftoff can be seen in Fig. 2. Despite the apparent differences in appearance, yield, and I_c , results of these two bump arrays were similar.

2.2 FLEX Fabrication

The goal of this fabrication process was to be able to run two layers of superconducting Nb wiring across a polyimide bridge. With its low thermal conductivity and high flexibility, the polyimide can serve as thermal isolation for the focal plane as well as a flexible connection to readout circuitry located below the focal plane [5]. Fabricating the flexible Nb microstrip, or FLEX, required that we etch a layer of polyimide with a sloped sidewall and deposit two layers of Nb microstrip wiring on the slope.

On a silicon wafer with a 2000 Å thick silicon oxide (SiO_2) film, following an adhesion promoter, polyimide was spun to a thickness of 6.5 μm on the wafer. Next, the polyimide layer was cured in a vacuum oven at 200 °C and then 350 °C, utilizing a N_2 gas backfill of 4 mTorr during the heating process. An O_2/CF_4 etch was then used to create a sloped sidewall with minimal pitting of the sloped polyimide surface. After etching the layers of SiO_2 deposited on the wafer, sputtered Ti/Nb/Ti was deposited; the latter was next patterned into the first layer of leads. A second layer of SiO_2 was added to create insulation between lead layers. Vias were etched into the oxide prior to deposition of the second Ti/Nb/Ti layer. Next, the first layer polyimide process was repeated for a second layer; however, the second layer of polyimide was etched only with O_2 plasma as there was no need to maintain as smooth a polyimide layer for subsequent steps. Following the second polyimide layer etch, Al contact pads were deposited. Finally, four individual chips were yielded using deep reactive ion etching.

2.3 Integration of Indium Bumps on FLEX Chips

The integration of In bumps and FLEX follows the same processes stated above in Sect. 2.2, inserting the 10 μm In bump deposition process and an MoN pad layer. After liftoff of the In layer, the wafer is coated in photoresist, wax bonded to a glass wafer, and deep etched to produce chips with integrated FLEX and In bumps as shown in Fig. 3. Heating of the wafer

post-indium deposition is limited to 110 °C, which is needed to wax-mount the wafer for deep etching.

A chip 1.5 cm in size proved sufficient to enable 640 microstripped wiring pairs with a 20 μm pitch: the wire count needed for the ATHENA full-scale prototype. The trapezoidal shape of the polyimide region is used to limit the surface area of the die attach side (the side of the chip with the 10 μm indium bumps) over the focal plane. This will allow us to fit six of them around the edges of the HEX chip. Additional In bumps beyond the 1280 needed for the wiring array were used to increase the required bumping force for a stronger bond of the die to the HEX. In future iterations, we will consider using post-bump epoxy underfill to increase bond strength.

3 Assembly and Characterization

3.1 FLEX Chips

Chips were characterized and tested using an adiabatic demagnetization refrigerator (ADR) system to cool the chips to 2 K. By wirebonding to Al pads on the FLEX chips, four terminal measurements of the Nb transitions using different bias currents were taken with a resistance bridge. These transitions were measured for the Nb leads on the polyimide layer, and on the polyimide/silicon interface, in order to characterize the quality of the leads (Fig. 4).

The deposited metal transitioned from superconducting to normal above 9 K as expected on all regions of the chip; however, there was an exception for some narrow regions where the polyimide was sloped. T_c in these regions tended to vary between 5 and 7 K and dominated the current-carrying capacity. The addition of the SiO_2 layer between the two leads pushed T_c higher in this region for the first Nb layer deposition. Our measurements indicated that even in a relatively low T_c region, I_c will approach 10 mA. We are currently investigating the optimization of the Nb leads' photoresist patterning as well as the deposition techniques.

3.2 Indium Bumps

We assembled test modules using the chips described in Sect. 2.1. Our goal was to characterize the two different thicknesses of In bumps (1 and 10 μm) as well as observe the effects of the different cleans. In order to test the devices, we first flip-chip, bump-bonded two 10 μm bump chips together, forming three different in-series circuits (4 bumps, 312 bumps, and 528 bumps) to test in our ADR system using a resistance bridge. Prior to bump bonding, the In surfaces received a solvent clean to remove photoresist and plasma clean residue. Afterward, a second plasma clean for the removal of oxide and surface passivation of the indium was performed in either an RIE or a downstream plasma surface treatment (DPST) process. This was done to promote bumping between the indium since it will grow a thick, tough oxide layer when exposed to air. Bump resistance is known to depend strongly on this oxide, decreasing once it is removed [6]. Using a flip-chip bonder set to 0.4 g per bump, the chips were bumped together, compressing the height of the bump pairs by about half. We also bump-bonded one 10 μm bump chip to one 1 μm bump chip using the DPST process on the In surfaces.

Our resistive transition measurements of the 528 bumped pairs in series are shown in Fig. 5. Such curves display a distribution of T_c with the onset of resistance temperature T_0 corresponding to the lowest T_c in the In bump circuit. The reported T_c is given by the resistive midpoint of the steepest part of the transition, a commonly accepted method to measure average T_c . We also estimate the normal resistance per In bump pair (R_n) using the resistance measured at 7 K. The resistance of the circuit is observed to increase gradually, and roughly linearly, from 3.5 to 8 K, the range over which the In transitions occur. By using the resistance measured at 7 K to estimate the resistance per bump, we attempt to minimize the resistance-reducing effect caused by the enhanced conductivity of superconducting MoN leads. Parameters characterizing the observed behavior for the two types of circuits are compiled in Table 1.

The observed transition widths indicate that all the bumps become superconducting, with comparable critical currents; however, the bumps' transitions do not occur simultaneously. We observe broadening in the critical current of the 10:1 chip, as indicated by a lower T_0 than in the 10:10 chips. With the 1 μ m bumps, their smaller In volume experiences less flow during bumping. This reduces the cross section of the bump-to-bump interface and extrusion of the In into its mating bump, as compared to the 10:10- μ m bump pairs. The full transitions show fluctuations in conductivity between 4 and 8 K, above the indium transition but below the MoN transition. The decrease in resistance at these intermediate temperatures suggests that an S-S'-S link is formed by the MoN:In. Since the In bump pairs have a low normal state resistance, the link is expected to have high critical current [7].

We are currently investigating how to calculate the critical current when we apply higher excitation currents to the bumped structures, as well as how to conduct measurements at those currents. In the future, we will experimentally determine the critical current at 50 mK, the operating temperature for the ATHENA X-IFU focal plane, where these structures will be deployed.

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Fig. 1.

Computer-aided design rendering of a prototype ATHENA focal plane with a 90-mm hexagonal detector chip (HEX) mounted to a six-sided fixture with bias and readout on each side. The indium bumps will be located along the edges of the HEX in square arrays of about 640 bumps. Flexible superconducting lines (FLEX) suitable for wirebonding are shown connecting each side of the HEX to an electronics card (superconducting quantum interference devices, SQUIDs). Image courtesy Randy Doriese (Color figure online)

Fig. 2. SEMs of 10 μm In bumps showing the effects of differing cleans. Left: The photograph shows a shallow bump shape and lower adhesion to the MoN layer after the 250 V clean. Right: Photograph of indium liftoff deposition preceded by the 800 V clean

Fig. 3.

Left: Prototype chip demonstrating the indium bump process integrated with Nb microstrip on flexible circuitry. Indium bumps located in the center of the square chip. Right: 90 mm diameter HEX wafer with indium bump mating circuits near each edge. These chips are sized for installation in the assembly shown in Fig. 1 (Color figure online)

Fig. 4. Resistance versus temperature for top (lead 2) and bottom (lead 1) niobium layers on a flexible polyimide substrate. Due to regions of sloped or roughened polyimide, T_c suppression is observed as a function of bias (measured from 3 μ A to 1 mA) (Color figure online)

Fig. 5.

Top: Transitions for 528 pairs of 10:1 μm In bumps in series showing T_c at low bias elevated above that of bulk In. Bias current is indicated on the legend. The measured trend of I_{bias} versus T_0 predicts that sufficient I_c is achieved at lower temperatures. Bottom: A gradual transition from superconducting to normal was observed in the bump-bonded chips. To estimate the average normal resistance per indium bump, we select the resistance at 7 K to find the normal resistance of the indium prior to the MoN transition at 8 K (Color figure online)

Table 1

We report the T_c (at the resistive midpoint) and T_o (onset of superconductivity, 100% of bumps transitioned) at 3-mA excitation and estimate the normal state resistance per bump pair R_n for several assemblies

Bump thicknesses (μm)	MoN; In sample cleans	$T_c; T_o$ @ 3 mA(K)	R_n @ <8 K (m Ω)
1:10	800 V; DPST	3.40; 3.14	0.59
10:10	250 V; RIE	3.44; 3.43	0.13
	800 V; DPST	3.45; 3.43	0.084