FPGA-Based Interface of Digital DAQ System for Double-Scattering Compton Camera

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Abstract

Purpose The double-scattering Compton camera (DSCC) is a radiation imaging system that can provide both unknown source energy spectra and 3D spatial source distributions. The energies and detection locations measured in coincidence with three CdZnTe (CZT) detectors contribute to reconstructing emission energies and a spatial image based on conical surface integrals. In this study, we developed a digital data acquisition (DAQ) board to support our research into coincidence detection in the DSCC.

Methods The main components of the digital DAQ board were 12 ADCs and one field programmable gate array (FPGA). The ADCs digitized the analog 96-channel CZT signals at a sampling rate of 50 MHz and transferred the serialized ADC samples and the bit and frame clocks to the FPGA. In order to correctly capture the ADC sample bits in the FPGA, we conducted individual sync calibrations for all the ADC channels to align the bit and frame clocks to the right positions of the ADC sample bits. The FPGA logic design was composed of IDELAY and IDDR components, six shift registers, and bit slip buffer resources.

Results Using a Deskew test pattern, the delay value of the IDELAY component was determined to align the bit clock to the center of each sample bit. We determined the bit slip in the 12-bit ADC sample using an MSB test pattern by checking where the MSB value of one is located in the captured parallel data.

Conclusions After sync calibration, we tested the interface between the ADCs and the FPGA with a synthetic analog Gaussian signal. The 96 ADC channels yielded a mean R^2 goodness-of-fit value of 0.95 between the Gaussian curve and the captured 12-bit parallel data.

Keywords Double-scattering Compton camera (DSCC) · Prompt gamma imaging · FPGA-based digital DAQ system · Sync calibration of interface between ADC and FPGA

Introduction

Tomographic imaging has an important role in oncology and neurology for helping doctors see inside a patient's body and monitor therapeutic effects noninvasively [1–5]. A Compton camera is a radiation tomographic imaging system that can generate a three-dimensional image from coincident measurements from multiple detectors. Conventionally, a Compton camera consists of two

detectors in which the main detector interaction phenomena are Compton scattering and photoelectric absorption. The Compton camera forms a radiation image from the measured signals through electronic collimation of incident gamma rays [6–8]; thus, the camera has a potentially high sensitivity. In addition, the Compton camera can be manufactured to a compact size that can be mounted onto remotely controlled vehicles such as drones, helicopters, or boats. These vehicles provide mobility and enable monitoring to be conducted without human exposure to very hazardous sites [9, 10]. The appropriate detector type for Compton imaging is a semi-conductor with a good energy resolution [11–14]. Furthermore, multi-radiotracer imaging can be a good application of the Compton camera [15–18]. Without knowledge of the emission energies involved in the measurement, it is necessary to build the Compton camera with more than three detector layers. Such a device would be beneficial for monitoring the therapeutic effect and irradiation accuracy to target organs

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by detecting the secondary prompt radiations that arise during radiation therapy [20, 21].

In this study, we focus on the double-scattering Compton camera (DSCC), which is capable of simultaneous detection of multiple radiotracers. The DSCC can also recover a three-dimensional image of radiation distribution and an emission energy spectrum [22–24]. As shown in Fig. 1, the DSCC consists of three detector layers, and the camera measures detector positions ($\mathbf{P}_n$) and deposited energies (ΔE_n) related to three successive interactions with the detector layers within a coincidence time. The dominant interaction in each detector layer is Compton scattering. The energies and detection locations measured in coincidence contribute to computing the Compton scattering angles and recovering both the emission energy spectrum and the spatial image of the radiation source distribution based on conical surface integrals. The scattering angle at the n -th detector is computed by the energetic relation of incident and scattered gamma rays or the geometrical relation of two position vectors as

$$\cos(\omega_n) = 1 - m_e c^2 \left(\frac{1}{E_n} - \frac{1}{E_n + \Delta E_n} \right) = \frac{(\mathbf{P}_{n-1} - \mathbf{P}_n) \cdot (\mathbf{P}_n - \mathbf{P}_{n+1})}{\|\mathbf{P}_{n-1} - \mathbf{P}_n\| \cdot \|\mathbf{P}_n - \mathbf{P}_{n+1}\|}, \quad (1)$$

where m_e is the electron rest mass and c is the speed of light. Then the initial emission gamma energy, E_0 , can be recovered by

$$E_0 = \frac{1}{2} \left(\Delta E_1 \pm \sqrt{\Delta E_1^2 + \frac{4m_e c^2 \Delta E_1}{1 - \cos(\omega_1)}} \right) \quad (2)$$

We could define a cone with the computed scattering angle (ω) at the first detector and the interaction positions

($\mathbf{P}_1$ and $\mathbf{P}_2$) for each measured coincident event from the DSCC. The half angle, apex, and axis of each cone are ω , $\mathbf{P}_1$, and $\mathbf{P}_1\mathbf{P}_2$, respectively. The spatial image of source distribution can be reconstructed by mathematical approaches based on the inverse conical surface integrals of the Compton data [24–26].

For the prompt gamma imaging, the performance of DSCC should be improved in terms of low energy ($< 10\%$), fast timing (< 1 ns), and fine spatial (< 6 mm) resolutions. Here, for the coincidence detection of the DSCC, we developed a digital data acquisition (DAQ) board to extract detection information such as interaction positions and energies. One key component of our DAQ board is a field programmable gate array (FPGA), which is a programmable chip that can easily modify the implemented digital circuit design. In biomedical applications, FPGAs are widely used for handling interfaces among sensor signals and extracting necessary information from these signals [27]. In this study, we implemented FPGA-based interfaces for coincident digital data acquisition from the DSCC. Among other FPGA functions, we tested the interface calibration between 96 ADC channels and the FPGA.

Materials and Methods

Digital DAQ Board for Coincidence Detection of DSCC

Figure 2 shows the procedure we developed for sensor signal transfer to the digital DAQ board. We constructed a DSCC with three CdZnTe (CZT) detector layers, and each CZT has 32 output channels for a total of 96 output

Fig. 1 Imaging principle of double-scattering Compton camera which operates in coincidence detection of three detectors

Fig. 2 Diagram of double-scattering Compton camera consisting of three CZT detectors (96 channels), pre-processing analog circuits, ADCs, and FPGA functions

signals. The active area of each CZT is $50 \times 50 \text{ mm}^2$ with a pitch size of 3.125 mm. The reference pulse height and the rise time of the CZT output signal are 60 mV (^{241}Am , 5.486 MeV) and 200 ns. The reported energy and timing resolutions are 75 keV and roughly 340 ps. These analog channel signals sensed in the coincidence detection are pre-processed as pre-amplified, amplified, and Gaussian-shaped signals. These pre-processed analog signals are transferred to the digital DAQ board and processed to extract the necessary information for the Compton imaging.

As shown in Fig. 3, the main components on the digital DAQ board are 12 analog-to-digital converters (ADC) and one FPGA chip. We selected the ADC model ADS-5281 by Texas Instruments; this model has eight channels, and each channel outputs 12-bit serialized digital samples at a sampling rate of 50 MHz [28]. The 96 analog signals transferred to the digital DAQ board are fed first into the corresponding ADC channels. For the FPGA, we chose the model Artix7-200T by Xilinx [29]. The FPGA plays three main roles: controlling the interface between the ADCs and the FPGA, digital signal processing to extract the detection information (energy and detection locations) from the coincident measurements, and providing the transfer interface between the FPGA and the PC.

Interface between ADCs and FPGA

The following is a description of the setting we developed for the interface between the ADCs and the FPGA. The ADC samples the Gaussian-shaped analog CZT signals at the sampling rate of 50 MHz and digitizes each captured sample value to 12 bits. Each ADC channel

outputs the serialized samples synchronized with two clocks: a bit clock and a frame clock. As shown in Fig. 4, after capturing the sample values, the ADC sends each bit in order from the least significant bit (LSB), D0, to the most significant bit (MSB), D11, at twice the rate of the bit clock. The ADC generates the bit clock at six times faster than the sampling rate and synchronizes this clock to the center of each serialized 12-bit sequence. The rising and falling edges of the frame clock are synchronized to the start and the end bits of the n -th ADC sample at the sampling rate, respectively.

Next, the FPGA receives the serialized ADC sample bits, the bit clock, and the frame clock from each channel of the ADC. The FPGA first conducts an individual sync calibration of the serialized sample bits with the bit and frame clocks for each channel input and recovers a parallel digital value from the transferred ADC sample bits. Figure 5 shows the logic design of one channel for capturing and deserializing the sample bits. The logic design is composed of IDELAY, IDDR, shift registers, and a bit slip buffer. The arriving ADC bits are passed through the IDELAY, IDDR, and shift registers for capturing with the bit and frame clocks. In order to synchronize the bit clock to the center of each serialized bit of the ADC sample value, we added IDELAY components to the 96 input ports of the FPGA. Figure 6 shows an example of capturing parallel data from 12 serial bits according to the bit and frame clocks. The IDELAY component delays the input signal by pre-determined delay taps, then the IDDR component captures the delayed bits (Q1 and Q2) at the rising and falling edges of the bit clock. The captured bits are preserved through six shift registers (SR)

Fig. 3 Digital data acquisition board of double-scattering Compton camera consisting of two main components, 12 ADCs (ADS-5281, Texas Instruments) and a FPGA (Artix7-200T, Xilinx)

until all of the 12 bits are completely captured. At the falling edge of the frame clock, the captured bits (Pdata) are corrected by the bit slip.

In order to deserialize the correct ADC sample bits into 12-bit parallel data, we needed to align the bit and frame clocks to the right capturing position of the serialized ADC sample bits. Because the 96 ADC channels have different transfer latencies, the individual sync calibration was essential prior to capturing the parallel data for each channel. As shown in Fig. 7, we used two special test patterns, Deskew (0101010101)

and MSB (100000000000), that were generated by changing the ADC register values for the sync calibration. Using these test patterns, we determined the delay taps and bit slips needed to align the bit and frame clocks.

The delay value of the IDELAY component was calibrated by the Deskew signal pattern. In the variable delay mode of the IDELAY component, we incremented the delay tap from zero to 31 to see how much transfer latency was in the input port. One delay tap size is 78 ps, and a delay tap set to zero means there is no delay. For example, if the bit clock is not

Fig. 4 Serialization operation scheme of 12-bit ADC samples digitized from the analog signal with bit and frame clocks

Fig. 5 Digital logic diagram to capture 12-bit parallel data from the ADC serial data transferred to FPGA

aligned to the center of the sample bits, the bit clock should appear as a red clock, as shown in Fig. 7. When the captured Deskew pattern value is reversed from the initial one at the zero-delay tap (e.g., from 0101010101 to 1010101010) by incrementing the delay tap, the delay tap number becomes the delay value of IDELAY and then the IDELAY component changes to the fixed delay mode.

The bit slip is determined with the MSB test pattern. The rising and falling edges of the frame clock are not aligned to the right LSB and MSB positions of the ADC sample value, as indicated by the blue clock in Fig. 7. Due to this mismatch, the parallel data is composed of mixing

the $(n-1)$ -th and n -th sample bits. After fixing delay tap of the IDELAY component, the bit slip was determined by checking where the MSB value of the test pattern should be located in the captured 12-bit parallel value. The bit slip was used to align the rising edge of the frame clock to the right MSB bit of the 12-bit parallel data.

Results

In order to test the interface between the ADCs and the FPGA for handling the 96-channel CZT signals, we generated an

Fig. 6 Procedure to capture 12-bit parallel data with IDDR and shift registers with well-aligned bit and frame clocks

Fig. 7 Sync calibration of interface between ADCs and FPGA with two test patterns, Deskew and MSB

analog Gaussian signal with a pulser (ORTEC 480) and a shaper (ORTEC 572A) and equally distributed the signal to the 96 ADC input ports. Figure 8a shows the Gaussian analog input signal with a height of 800 mV and a shaping time of 1 μ s. Figure 8b compares the deserialized ADC samples of the analog Gaussian curve before (red curve) and after (blue curve) sync calibration for one representative channel. The x-axis indicates the sampling time point to capture the 12-bit parallel ADC samples at every 20 ns. The y-axis is the captured parallel ADC sample values. Using the ChipScope debugging tool of the Xilinx ISE program, the 12-bit parallel

data were extracted. Before sync calibration, we observed errors in the captured parallel data due to mismatches among the ADC bits and the bit and frame clocks. However, through sync calibration, we were able to recover the parallel data, and we subsequently obtained the Gaussian curve in all of the ADC samples. Figure 9 shows the R^2 measure of the goodness-of-fit between the Gaussian curve and the captured ADC samples. The mean R^2 value of 0.95 over the 96 channels indicates a reasonable fit to the Gaussian curve. Figure 9 also shows that some of the ADC channels yielded worse fits due to outliers in the parallel data. Further research is needed

Fig. 8 **a** Mimic analog Gaussian-shaped signal generated from a pulse and a shaper. **b** Comparison of Gaussian ADC sample curves captured in FPGA before and after sync calibration

Fig. 9 R^2 goodness graph of Gaussian curve fit from captured 12-bit ADC samples over 96 channels

on ways to remove such outliers before extracting the peak values from the Gaussian curves.

Discussion

In this study, we have developed a digital DAQ board to support our research into coincidence detection in the DSCC. In its use as a radiation imaging system, the DSCC provides the emission energy spectrum and the 3D spatial image of the source distribution from the measured coincident data in three stacked CZT detector layers. The main components on the digital DAQ board are 12 ADCs and one FPGA. The ADCs digitize the analog 96-channel CZT signals at a sampling rate of 50 MHz and transfer the serialized ADC samples and the bit and frame clocks to the FPGA. In order to capture the ADC sample bits correctly in the FPGA, we conducted individual sync calibrations for the 96 ADC channels to align the bit and frame clocks to the right positions of the ADC sample bits. The FPGA logic design was composed of the IDELAY and IDDR components, six shift registers, and bit slip buffer resources. Using the Deskew test pattern, the delay value of the IDELAY component was determined to align the bit clock to the center of each sample bit. We determined the bit slip in the ADC sample bits using the MSB test pattern by checking where the MSB value of one is located in the captured parallel data. After sync calibration, we tested the interface between the ADCs and the FPGA with a synthetic analog Gaussian signal. The 96 ADC channels yielded a mean R^2 goodness-of-fit value of 0.95 between the Gaussian curve and the captured 12-bit parallel data. As shown in Figs. 8b and 9, some channels had worse fits due to some outliers in the parallel data and the limited timing resolution and the different clock time

skews of resources in the FPGA. In order to extract energy information from the peak values of the Gaussian curves, it is necessary to address the outliers in our future research.

Conclusion

We developed a digital DAQ board consisting of 12 ADCs and a FPGA for the double-scattering Compton camera. The ADCs digitized 96 CZT analog signals into 12 sample bits and transferred the serialized sample bits and the bit and frame clocks to the FPGA. In order to recover the parallel data from the sample bits, we conducted first a sync calibration of the interface between the ADCs and the FPGA using two special test patterns: Deskew and MSB patterns. With the calibrated delay tap and bit slip, the bit and frame clocks were aligned to the right positions of the serialized ADC sample bits. The test with a synthetic Gaussian analog signal yielded a reasonable fit to the Gaussian curves of the 12-bit parallel ADC samples after sync calibration.

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Compliance with Ethical Standards

Conflict of Interest Soo Mee Kim and Young Soo Kim declare that they have no competing interests.

Ethical Approval This article does not contain any studies with human participants or animals performed by any of the authors.

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