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A 15-channel 30-V Neural Stimulator for Spinal Cord Repair

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Abstract

This paper presents a 15-channel, 30-V, implantable current stimulator for restoring locomotion control after spinal cord injuries. The stimulator features performance specifications comparable to those of large desktop instrumentation: high linearity, high precision of the delivered currents, small channel-to-channel mismatches and a fast settling time of 0.3 μ s. An ADC-based active charge balancing scheme using a digital PI (proportional–integral) controller was implemented in firmware.

Index Terms

Neural stimulator; charge balancing; PI Controller

I Introduction

Electrotherapy systems using current-mode stimulation have been developed, for example, for retinal stimulation to partially restore vision, or for stimulation of peripheral nerves in attempts to restore limb functions [1] [2] [3] [4]. A wire-connected platform to restore locomotion control after spinal cord injuries was developed by project collaborators using off-the-shelf components [5]. Here we present the development of an implantable neural stimulation system, the embedded wireless telemetry of which was reported in [6]. The focus of this paper will be on the design of a 15-channel, 30-V, implantable current-mode neural stimulator that can deliver enough current to stimulate the spinal cord of small or potentially also larger animals while using different electrode configurations and placements.

The neural stimulator was designed to feature performance characteristics comparable to those of large desktop instruments. These specifications included linearity, a short settling time and good precision and reproducibility of the current outputs. In addition, we tried to overcome limitations of existing current stimulators that have been described in literature, for example, that the stimulation output current depended on the applied output voltage as a consequence of hot-carrier-injection effects (HCI effects) [1]. Other limitations included stimulation undershoots and slow output settling [2], or a limited supply voltage (18 V) owing to the adopted power supply scheme and fabrication process [3].

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We intended to improve the current stimulator performance through specific analog and digital circuit design measures: (1) preservation of the pulse width between positive and negative current pulses by using a digital method; (2) achieving fast settling by using a source-switching scheme in the high-voltage (HV) domain, which does not have device reliability issues; (3) implementing the current DAC in the high-voltage domain to achieve good linearity, which eases the implementation of active charge balancing; (4) improving output precision and reducing channel-to-channel mismatches by using a time-multiplexed trimming IDAC.

Charge balancing of the positive and negative portion of the generated biphasic stimulation current pulses is pivotal for longer-term implanted devices, since any accumulation of excess charges over time will lead to electrochemical reactions, which would cause damage to the electrodes and neural tissue. Charge balancing in a current stimulator can be implemented either in a passive or active way [1]. A general disadvantage of passive charge balancing is that success is neither guaranteed nor monitored. This issue can be addressed by employing active (or closed-loop) charge balancers. The performance of a comparator-based active charge balancing scheme presented in [1] featured limited speed of convergence. In this work, an ADC-based active charge balancing scheme using a digital PI (proportional–integral) controller has been implemented in firmware, together with an on-chip amplifier and an on-chip ADC (reused from the on-chip neural recording function) so that fast convergence could be achieved. In addition, by implementing the PI controller in the digital domain, design flexibility to accommodate different stimulation electrodes and electrical parameters is provided.

This paper is organized as follows. After the introduction, we present the system architecture and the implementation of the current stimulator in Section II. Section III illustrates the active charge balancing method. Section IV presents the measurement results, and Section V concludes this work.

II Implementation of Current Stimulator

Figure 1 presents the architecture of the current stimulator. This stimulator is powered by an off-chip 30-V supply, and the 15-V supply is connected to the reference electrode. Each stimulation channel can generate biphasic current pulses with current amplitudes of 3.15 mA full-scale and 6-bit DAC (Digital-to-Analog Converter) resolution.

After each biphasic stimulation pulse, the residual voltage is sensed by an on-chip amplifier and digitalized by an on-chip SAR ADC (Successive-Approximation-Register Analog-to-Digital Converter; reused from the on-chip neural recording function). The magnitude information of the residual voltage is fed to a PI controller (in off-chip firmware), which controls an 8-bit auxiliary IDAC (Current DAC) and compensates the charge imbalance between the “positive IDAC” and the “negative IDAC”.

Figure 2 shows the implementation details. The most important innovative aspects include (i) the efficient trimming scheme using only one current reference generator and one IDAC for delivering precise current outputs in all 15 channels, (ii) the realization of IDACs and

source-switching scheme in the HV (High Voltage) domain, and (iii) the use of a digitally-assisted analog design for the LV (Low Voltage) to HV level-shifting to reduce charge imbalances. Details will be described in Sections A and B below. All LV analog and digital circuits are powered by a 1.8-V supply. DMOS (Double-Diffused MOS) transistors [7] are adopted for HV protection. Each stimulation channel consists of a dynamic current-copier (M_{cp} and C_{cp}), a floating current mirror (M_{fca} and M_{fcb}), a positive IDAC (P-IDAC) and a negative IDAC (N-IDAC).

A Trimming: Current Reference and IDAC

The current reference generator circuit delivers a current with low temperature dependence, which is needed, as the stimulator was initially not implanted in the animal to conduct first experiments. The implemented trimming scheme provides a low-cost realization for delivering precise current outputs per channel and for minimizing the channel-to-channel mismatches by using the same trimming IDAC for all channels. The trimming codes for each channel were determined by measuring the full-output-scale current of the N-IDAC during chip testing. The common IDAC regulates the reference current for each stimulation channel in a time-division manner and is disabled after usage. The dynamic current copier in each channel, consisting of M_{cp} and C_{cp} in Figure 2, receives the reference current and freezes the voltage across C_{cp} for current duplication immediately before a biphasic current pulse is generated. The leakage current across the capacitor is not an issue here, since the duration of the current pulses is usually less than 1 ms, and the operating temperature is limited to 40°C for implantable devices.

A floating current mirror, consisting of M_{fca} and M_{fcb} , is utilized to provide the same reference current to the P-IDAC and the N-IDAC, which reduces current mismatches and simplifies charge balancing [1]. Both P-IDAC and N-IDAC consist of a 6-bit main IDAC with an LSB of 50 μ A and another auxiliary IDAC for charge balancing. By implementing the IDAC function in the HV domain, high linearity is maintained in comparison to implementing the IDAC function fully or partially in the LV domain, which would consume less silicon area. This is due to the fact that the mismatches in the HV current mirrors are input-dependent and become difficult to handle upon feeding the HV current mirrors with varying currents from an IDAC in the LV domain. Good IDAC linearity eases the implementation of the active charge balancing by limiting the maximum amplitude of the initial residual voltage after stimulation.

As illustrated in Figure 2, the area consumed by the HV IDAC was reduced by using LV transistors for the IDACs and by using HV transistors to protect those LV transistors. Moreover, we developed a source-switching scheme in the HV domain, which offers two major advantages: First, normal LV transistors can be used to control the IDAC switches, which significantly reduces the consumed area for each HV IDAC. Second, the source-switching scheme speeds up the settling of the current output and eliminates overshoots/undershoots reported in [2]. The preserved pulse shapes facilitate charge balancing in biphasic current stimulations, as the maximum amplitude of the initial residual voltage after stimulation is limited.

For a current-mode stimulator, a large output impedance is critical to achieve constant current outputs across a wide range of output voltages. In references [1] [2], a regulated cascoding scheme with additional OTAs (Operational Transconductance Amplifier) was adopted, which slightly increased the voltage headroom of the current stimulator. However, it would be difficult to combine the regulated cascoding scheme [1,2] with our source-switching scheme.

Therefore, a simpler self-biased cascoding scheme, shown in Figure 2, has been adopted here. This implementation only slightly reduces the voltage compliance range of the stimulator, which is not so critical for our high-voltage stimulator with a supply voltage of up to 30 V. In addition, the self-biased cascoding scheme does not require additional biasing currents, so that the power consumption is reduced. As illustrated in Figure 2, HV diode-connected clamps have been used to protect the LV transistors, when the source switches were disabled.

B HV Level Shifting and Regulator

An HV dynamic level shifter, shown in Figure 3, has been adopted to translate control signals from the 1.8-V domain to the 30-V domain. It does not consume any static current, which is different from the level shifters in [1]. The largest drawback of this HV dynamic level shifter is the asymmetric rising and falling propagation delay [8]. This makes charge balancing difficult for biphasic stimulation pulses, if the level shifter is used to translate the enabling signal for the P-IDAC. For example, if the delay is 20 ns for the rising edge and 10 ns for the falling edge, a 500- μ s pulse width in the LV domain (which is also used to define the duration of the N-IDAC operation in Figure 2) will be translated to a 499.99- μ s pulse width in the HV domain (which is used to define the duration of the P-IDAC operation). The N-IDAC and P-IDAC will thus be enabled with slightly different pulse durations, which will lead to a charge imbalance. In [8], significant efforts were spent to minimize such differences. In order to resolve this issue, we selected a digitally-assisted analog design approach shown in Figure 4.

In the LV domain, both, the rising and falling edge of the enabling pulses for the P-IDAC (P_{LV} in Figure 4) are transformed into short pulses in P_{LV_t} (using a clock-based delay cell and an exclusive-or gate), which are then translated to the HV domain (in P_{HV_t}). Simple logic in the HV domain (a flip-flop and an inverter, implemented with 3-V transistors, which operate between the 30-V and 28-V power rails) is used to transform those two short pulses back to the desired enabling signal P_{HV} for the P-IDAC. Through this approach, only the rising edges of the short pulses carry critical transition timing information, so that the pulse duration of the P-IDAC is preserved. This eases the implementation of charge balancing. Note that the presented pulse reservation scheme is only applied to the P-IDAC enabling signal. The amplitude controlling signals for the P-IDAC and auxiliary P-IDAC are directly translated using the level shifter shown in Figure 3. In order to reduce the number of level shifters to 2 for the amplitude controlling signals, parallel-to-serial conversions are applied in the LV domain, and serial-to-parallel conversions are used to recover the HV signals. Since the amplitude-control signals are also stored in the serial-to-parallel converter in the HV domain, level shifting is only necessary,

when the corresponding amplitude registers are updated by firmware, which reduces power consumption. The presented level-shifting scheme is different from that in [1], as the authors of [1] used level shifters with static current consumption to translate the P-IDAC enabling signal and the amplitude-control signals, which were then stored in the HV domain.

To generate the ground potential for the HV domain, we implemented a regulator shown in Figure 5 [9]. This HV regulator features a push-pull output stage and an open-loop operating mode, which reduces power consumption and assures stability under all capacitive-load conditions. In addition, the generated regulator output voltage is based on the sum of the threshold voltages of the LV PMOS and HV-PDMOS transistors. This arrangement reduces the delay variations of the HV level shifters by tracking the fabrication-induced fluctuations between the HV level shifters and the regulator output. An off-chip 20 nF capacitor was used to stabilize the output voltage.

III Active Charge Balancing

In order to measure the residual voltage on the electrodes after each biphasic pulse, an amplifier shown in Figure 6 has been implemented with capacitors C_{in} of 160 fF and C_f of 80 fF. During the auto-zeroing phase, only the switches S_1 and S_2 are closed. During the sensing phase, only the switch S_3 is closed to provide an amplification factor of 2. The amplifier output representing the residual charge is fed to an on-chip 12-bit SAR ADC (re-used from on-chip neural recording function).

In [10], a comparator-based active charge balancing was presented, in which the residual voltage was compared to two safety limits, and where a controller regulated the stimulation current for charge balancing. The speed of convergence was slow, since the controller only had limited information on the residual charge. The two limiting comparators only provided 1.5-bit quantized information to the controller.

In this work, the averaged ADC output was fed to a PI controller (implemented in off-chip firmware) as shown in Figure 7, where I_{dx} is the initial current imbalance between the P-IDAC and N-IDAC in Figure 1, and V_{dy} is the sampled and quantized residual voltage after each biphasic stimulation pulse. The first delay-free integrator, attached to the V_{dy} node, is inherent to the voltage across a capacitor during current injection. The coefficient m is defined as,

$$m = \frac{T}{C}, \quad (1)$$

where T is the pulse width of the biphasic current stimulation, and C is the equivalent capacitance of the electrode. The scale factor a first translates the quantized residual voltage into a digital form to facilitate the control of the auxiliary IDACs in the P-IDAC or N-IDAC. The PI controller consists of a delay-free integrator and a direct pass-through path. Its output is used to adjust the auxiliary IDACs.

The closed-loop function of the proposed PI controller has been derived as follows:

$$\frac{V_{dy}}{I_{dx}} = m \frac{1 - z^{-1}}{1 - 2(1 - ma)z^{-1} + (1 - ma)z^{-2}} \quad (2)$$

To illustrate its stability, the maximal absolute radix of its poles versus the coefficient m^*a is plotted in Figure 8. It is obvious that the coefficient m^*a should not be too large in order to maintain stability, although a large m^*a may lead to faster convergence. For the *in-vivo* tests shown in Figure 13, the value of m^*a was set to 0.8.

Note, that the PI controller was implemented in firmware in this work, which can be easily migrated to hardware in the future. The implementation of the PI controller in the digital domain provides design flexibility in order to accommodate different stimulation electrodes and electrical parameters.

IV Measurement Results

The stimulator was implemented in a 0.18- μm HV CMOS process. The die photo is shown in Figure 9. The chip size (including the area for the HV PADs) is 3.8 mm x 2.8 mm. Each HV PAD has 8-kV HBM ESD robustness, which is desirable for implantable electronics. Note that some other functions like a neural recording channel were also integrated in this chip and were omitted in this paper.

The stimulator draws 6 μA (for the reference circuit and current mirrors) from the 1.8-V supply and 5 μA (for the HV LDO) from the 30-V supply in the standby mode, when the input clock is off. The system can be activated from this standby mode within one clock cycle. During continuous stimulation-mode operation with CLK ON, the controller draws 40 μA current from the 1.8-V supply.

To achieve high accuracy, the main IDAC also features a 3-bit thermometer decoder and a simplified random-walk layout style. The measured INL plots for the N-IDAC and P-IDAC are shown in Figure 10. The presented stimulator achieves 10-bit accuracy, which is considerably higher than that of the stimulator in [2]. The improved accuracy and linearity simplify the implementation of the active charge balancing.

The measured full-scale current vs. output voltage for the N-IDAC and P-IDAC are shown in Figure 11. There is no visible HCI degradation, which can be seen in [1]. The required headroom is around 1 V for both, P-IDAC and N-IDAC, and the maximum voltage compliance of this stimulator is 28 V. The mismatch in the full-scale current between the N-IDAC and P-IDAC in Figure 11 is 0.49%.

The stimulator output waveform through a 3.6 k Ω resistor for a current pulse with amplitude of 1000 μA is shown in Figure 12. The measured settling time (1%) is as low as 0.32 μs . The stimulation pulses are free of overshoots and undershoots, which were visible in [2].

The sampled electrode residual voltages from the conducted exemplary *in-vivo* tests (same set up as in [5, 12]) using rats are shown in Figure 13. The residual voltage after the first

biphasic current pulses is well within the safety limits, which is 100 mV in [10], owing to the optimized high-accuracy analog design. Fast convergence has been demonstrated. The impedance of the soft composite Pt-silicone electrodes amounted to $52.8 \pm 0.8 \text{ k}\Omega$ at 1 kHz [12].

The stimulator performance has been compared to the work of others as shown in Table I. In comparison to [2], our source-switching technique in the HV domain sped up settling and obviated undershoots. We also alleviated the HCI issue in [1] by using DMOS transistors. Our ADC-based active charge balancing features design flexibility and fast convergence. Our chip area is a bit larger than that of [2] owing to the implementation of additional circuits for neuronal recording.

V Conclusions

A 30-V, 15-channel, current-mode neural stimulator with a fast settling time of 0.3 μs has been presented. The proposed source switching scheme in the HV domain is key for fast settling. An ADC-based active charge balancing scheme has been also demonstrated. Fast convergence has been achieved.

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Figure 1.
Overall system architecture.

Figure 2.
Schematic of the current stimulator.

Figure 3.
Schematic of the dynamic level shifter (inside the P-IDAC).

Figure 4.
Pulse width reservation in level shifting (inside the P-IDAC).

Figure 5.
Schematic of the HV regulator (inside the P-IDAC).

Figure 6.
Schematic of the residual amplifier.

Figure 7.
PI controller for active charge balancing.

Figure 8.
Closed-loop function of the PI controller.

Channel 0~14
865 μ m x 295 μ m

Digital
3100 μ m x 280 μ m

HV-SW:
550 μ m x 330 μ m
(high voltage switch
for passive charge
balancing;
residual amplifier)

Ref:
180 μ m x 330 μ m
(reference generator,
HV-LDO, POR)

Clk:
150 μ m x 90 μ m

Figure 9.
Die photo of the current stimulator.

Figure 10.
IDAC INL plots for the neural stimulator.

Figure 11.
Measured IDAC full-scale current versus output voltage.

Figure 12.
Stimulator output waveform through a 3.6 kΩ resistor.

Figure 13.
Waveform for active charge balancing during in-vivo testing.

Table I

Comparison of the stimulator to the work of others.

Items	[1]	[2]	[11]	This Work
Channels	256	16	1	15
Voltage	20 V	15 V	22 V	30 V
Full-scale	1.0 mA	4.0 mA	5.12 mA	3.15 mA
Resolution	5-bit	8-bit	9-bit	6-bit
Max INL	N. A.	1.79 LSB	N. A.	± 0.03 LSB
Settling Time	N. A.	5.8 μ s	N. A.	0.3 μ s
Undershoot	No	Yes	N. A.	No
HCI Degradation	Yes	N. A.	N. A.	No
Charge Balancing	Active (CMP based)	DC blocking capacitor	Active (Analog Circuits)	Active (ADC based)
Chip Area (mm ²)	N.A.	2.9 $\times$ 2.3	N.A.	3.8 $\times$ 2.8