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Low Temperature CMUT Fabrication Process with Dielectric Lift-off Membrane Support for Improved Reliability

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Abstract

This paper reports an improved CMOS compatible low temperature sacrificial layer fabrication process for Capacitive Micromachined Ultrasonic Transducers (CMUTs). The process adds the fabrication step of silicon oxide evaporation which is followed by a lift-off step to define the membrane support area without a need for an extra mask. This simple addition improves reliability by reducing the electric field between the top and bottom electrodes everywhere except the moving membrane without affecting the vacuum gap thickness. Furthermore, the parasitic capacitance which degrades the CMUT receive performance is reduced. A 1-D CMUT array suitable for Intracardiac Echocardiography (ICE) imaging with 9MHz center frequency is fabricated using this method. Detailed electrical and acoustic testing indicates adequate performance of the devices for ICE in agreement with simulations. Long term output pressure testing with more than 2×10^{11} pulsing cycles and environmental testing demonstrate the efficacy of the approach for improved reliability as compared to devices without the additional membrane support layer.

Index Terms

CMUT low temperature fabrication; oxide lift-off; parasitic capacitance; reliable CMUT

I. Introduction

A significant premise of the capacitive micromachined ultrasound transducers (CMUTs) is electronics integration. Monolithic integration of CMUTs with CMOS electronics provides ultimately compact imaging systems where significant functionality of the front-end electronics can be realized right under the CMUT imaging array, practically eliminating parasitic capacitance to achieve near ideal signal to noise performance [1, 2, 3]. This enables single chip systems for high frequency applications like intravascular ultrasound (IVUS) imaging where the array elements have sub pF capacitances [4]. The key for monolithic integration is the low temperature CMUT fabrication process. Although low temperature wafer bonding [5, 6] is demonstrated, sacrificial layer based processes are also widely used [3, 7, 8, 9]. Sacrificial layer process does not need large areas for reliable bonding which can reduce the active area of the transducer element, and hence can be especially suitable for high frequency applications with smaller lateral membrane dimensions.

The cross section of the typical CMUT fabricated using a sacrificial layer process is shown in Fig. 1-a. In this process, a thin layer of dielectric separates the top electrode (TE) and the bottom electrode (BE) over the vacuum gap. CMUT efficiency depends on a high electric field over a thin vacuum gap and a dielectric isolation layer. Ideally, this high electric field should only exist over the membrane of the CMUT vibrating over the vacuum gap, but electrical connections between the membranes also pass over thin dielectric isolation layers. The resulting high fields on the thin isolation layer cause charging [10], dielectric breakdown and reduces the CMUT reliability. Furthermore, it increases the parasitic capacitance which is especially detrimental during the receive mode operation. Although some remedies such as LOCOS regions [11, 12] between the CMUT membranes have been proposed to decouple gap height from isolation layer thickness between CMUT membranes (Fig. 1-b), due to the high temperature processes including wet-oxide growth in 1050°C, high-temperature annealing, LPCVD silicon nitride deposition and using BOE for etching the oxide layer, the process is not suitable for monolithic CMOS integration.

Another approach to reduce the CMUT parasitic capacitance is using embedded patterned BE layers to minimize the overlap between top and bottom electrodes [13, 14]. Using embedded electrode method to make topography-free surfaces adds an extra etching step, significantly increasing the roughness of the dielectric surface due to etching. In addition, having 2 insulation layers on the top and bottom side of the sacrificial layer (sandwich method) increases the effective gap of the CMUT which degrades the CMUT performance. Cavity edge insulator extension method has been recently proposed in [15] to increase the reliability in CMUT cells for high ultrasound power transmission application. Although it significantly increases the breakdown voltage and CMUT's lifetime, using the sandwich method like [14], increases the effective gap resulting in degrading device performance. Besides, this approach adds an extra etching step and also height difference over the edges of the membranes - since the new PE-SiO₂ layer exclusively stays on the edge of the membranes - that makes the following deposition/patterning processes difficult. Furthermore, with large CMUT arrays (such as discussed here) where the active area needs to be maximized [7], the space between the membranes for electrical connections on the patterned BE needs to be small leading to thin electrical lines to reduce overlap. This leads to larger resistance over long CMUT elements such as in 1-D arrays. One may increase the BE electrode thickness, but that leads to large step heights which may be difficult to cover with metal layers in subsequent fabrication steps.

In this paper, we first describe a modified low temperature CMUT fabrication process (Fig. 2) where a lift-off step is introduced into the process flow. This step deposits a thick dielectric layer between the TE and BE except for the regions where there is a CMUT membrane. We then go over a specific CMUT device for intracardiac imaging applications fabricated with this process. We present electrical and acoustic measurements showing functionality with reduced parasitic capacitance. Finally, we compare the reliability of the devices with and without the lift-off step to demonstrate the improvement.

II. CMUT Design

The CMUTs fabricated with the lift-off membrane supports are designed in the form of 1-D imaging arrays (Fig. 3-a) for Intracardiac Echocardiography (ICE) application. The array is designed to have a center frequency of about 9MHz with a 60–70% fractional bandwidth. The fabrication is performed on 300- μm thick silicon wafers so that substrate thickness resonance is moved to 14MHz, which is beyond the transducer bandwidth [16].

In the CMUT design, the simulations are performed using a large signal model [17, 18] which predicts the output characteristics of a CMUT array operated in the non-collapse mode. In order to find the dynamics of the non-uniform electrostatic force accurately over the CMUT electrode, the membrane electrode is divided into patches shaped to match higher order membrane modes [18]. Based on this model, the lateral dimensions of the square membranes are determined to be $46\mu\text{m} \times 46\mu\text{m}$ with CMUT characteristics obtained through the design and modeling process are listed in Table 1. The optimized membrane thickness in bandwidth of interest is 2.2- μm , and the gap (95-nm) is optimized to obtain $\sim 1\text{--}2\text{MPa}$ peak-to-peak pressure with 30–60V pulses when operated in the non-collapsed mode [19]. Due to the residual stress and atmospheric pressure [9, 20, 21] on the Si_3N_4 membrane, the static deflection of about 15–18 nm is observed and as a result, the sacrificial layer (Cu) thickness which forms the CMUT's gap is designed to be around 110-nm.

III. Improved Low Temperature CMUT Fabrication Process

The processing steps involved in the improved CMUT fabrication are shown in Fig. 2. Note that all steps are performed at a temperature less than 250°C which leads to CMOS compatibility [20]. In the following figure, the fabrication process steps are described in detail and critical parameters are provided.

The process starts with 3- μm furnace oxide deposition for electrical isolation on a 4" $\langle 100 \rangle$ silicon wafer. In CMOS compatible version of the process, this oxide layer is replaced by low temperature PECVD oxide. To form the bottom electrode (BE) - (Fig. 2-a), Chromium (Cr) is deposited using unifilm sputterer tool; the sputtering system which deposits thin metal films in an argon-enriched low vacuum. The tool accurately monitors source distributions, by using a computer-controlled planetary system. Cr has strong adhesion to both metals and dielectric layers, and to have low resistance less than 100 ohm, the thickness is chosen to be in the 275–400-nm range. Copper (Cu) is used as the sacrificial layer as it can be etched very selectively with Cr and silicon nitride membrane layers. To pattern the sacrificial (gap) layer (Cu), the adhesion of the Cu and photoresist (PR) has to be enhanced by spinning a monolayer of P-20 HMDS Primer. The gap (Cu) thickness is optimized to generate maximum pressure based on a large signal CMUT model [17, 19]. Fig. 2-b shows the cross section after Cu is patterned. Note that the PR layer is not removed which is used for the lift-off process.

A. SiO_2 Lift-off Process

The critical addition to the fabrication process is the SiO_2 lift-off step shown in Fig. 2-c. In order to ensure that the leakage paths are completely blocked, a self-aligned process is

essential since inevitable misalignments in conventional optical mask aligner tools would create problems. The lift-off process helps achieve this goal by minimum additional effort. To lift-off the silicon dioxide, after patterning the sacrificial layer (Cu) and before stripping of the photoresist (PR), the silicon dioxide is evaporated using CHA Evaporator chamber at a pressure of about $5\text{e-}7$ Torr. In order to reduce the parasitic capacitance and increase the breakdown voltage, the silicon oxide layer thickness should be large. However, large topographical steps in the TE layer should be avoided as well. Therefore, the oxide thickness is chosen about two times the sacrificial layer thickness, which is typically 40–200-nm for the CMUTs considered here. The PR thickness in lift-off process has to be at least 3–4 times more than the deposited layer [20]. Shipley 1813 resist is sufficient for this process as it can form a 1.3- μm thickness when it is spun at 3000 rpm following by a 45-s dwell time. Photolithography is performed using 405-nm UV light with a dosage of $150\text{-mJ}/\text{cm}^2$, the wafers are developed in Microposit MF-319 for about 60-s with gentle agitation after 30-s, and followed by oxygen descum process in a Vision RIE (reactive ion etching) chamber with power of about 250-W. This ensures that the entire exposed PR is properly removed before the isolation layer deposition in a PECVD chamber at 250°C .

B. Isolation, Top Electrode and Membrane Formation

Low stress PECVD silicon nitride (Si_xN_y) is deposited as the isolation layer to ensure that the BE and TE are not electrically shorted when the membrane fully swings and touches the BE (Fig. 2-d). In order to minimize the pinhole effect in thin dielectric layer, the Si_xN_y is deposited in several steps; the plasma switches 3 – 4 times – each time deposits about 1/3–4 of total thickness. There is trade-off between process temperature and film thickness in Si_xN_y deposition and since the thermal budget is limited in CMOS compatible process, the thickness has to be adjusted to minimize the pinhole density [22]. A significant issue with thermal management during the isolation layer deposition is the oxidation of the sacrificial Cu layer after a short time (about 8–10 hours) and its delamination in the PECVD chamber. Therefore, the time interval between the sacrificial layer deposition and the isolation layer deposition should be minimized and the PECVD chamber temperature should be gradually increased up from 100°C to actual process temperature (250°C), so it has to be either load-lock system or a temperature-controllable tool.

After the isolation layer, aluminum is deposited to form TE of the device (Fig. 2-e). Aluminum also tends to be oxidized which affects the TE bond pad resistivity, so a thin layer of Cr (20–30-nm) is usually deposited on top to protect the Al TE surface. After TE formation, Si_xN_y is deposited to half of the eventual membrane thickness to seal the electrodes and sacrificial layers which is followed by sacrificial layer etch-hole patterning and etching using a CHF_3 based dry etch process to reach the sacrificial layer (Cu) that illustrated in Fig. 2-f and 3-d. The chip is then dipped into Cu etchant to release the membranes and the sample is dried in CO_2 super critical dryer chamber. The super critical dryer has to be extremely clean; since contamination can negatively affect the device performance through dielectric charging problems.

Alternatively, drying can be performed in oven with temperature of about $85\text{--}90^\circ\text{C}$ for about 1 hour. As the final step, Si_xN_y is deposited to reach the desired membrane thickness

(Fig. 2-g). The BE/TE bond pads are then opened followed by 200–300-nm gold lift-off for wirebonding to test PCBs.

IV. Results and Discussion

A. Process Characterization

Fig. 3-a and b show the micrograph of the completed 1-D CMUT array including 64 single element consisting of two rows of 40 square membranes. The middle image (Fig. 3-c) shows two membranes after the oxide lift-off step where only the oxide between the square membranes remains. The bottom image (Fig. 3-d) shows the same area after the process is completed. TE traces between the membranes, which earlier passed over only the isolation dielectric, now clearly go over the oxide steps. A scanning electron micrograph (SEM) was also obtained to provide detailed information on the cross sectional structure by cleaving the device along the dashed lines shown in Fig. 4-a. Fig. 4-b shows the SEM which clearly indicates 95 nm the vacuum gap, and ~200nm thick lift-off oxide layer. The vacuum gap as well as the ~200nm thick oxide layer in between membranes are clearly seen, showing the successful lift-off process. (Table 1).

Fig. 5 shows the Atomic Force Microscopy (AFM) measurements on the fabricated membrane which shows about 15-nm of bending at the center of the membrane mainly due to atmospheric pressure as expected. The collapse voltage of the CMUT with this gap is simulated to be 32V.

B. Electrical Characterization

To quantify the improvement in parasitic capacitance and coupling coefficient, the device capacitance for CMUT array elements with and without oxide lift-off supports are measured using a Signatone probe station. Fig. 6 shows the capacitance as a function of applied DC bias, the C-V curve. The capacitance is minimum at 0V DC bias for both devices and by increasing the DC bias close to collapse voltage, the capacitance value increases about 4.5 pF as expected in our model [17]. The capacitance value for oxide lift-off device is 2pF (15%) less, because the parasitic capacitance due to unnecessary TE-BE overlap areas is reduced. The difference between overlap area capacitance in Fig. 1-a and Fig. 1-b which is about $6000\text{-}\mu\text{m}^2$ for all 80 membranes, is also calculated about 2pF which proves the stray capacitance reduction in the Fig. 6.

When the DC bias is changed to 30V (93% of collapse voltage) and brought back to 0V, there is significant hysteresis in C-V characteristics for the regular CMUT and the capacitance minimum shifts to a positive voltage indicating that there is charging [10]. In contrast, charging for the CMUT with oxide support is significantly reduced, indicating that the dielectric layer between the TE-BE overlap areas is primarily responsible for charging. This is achieved without increasing the collapse voltage of the device. The C-V curve can also be used to measure the electromechanical coupling coefficient ($\kappa\gamma^2$) of the CMUT through the following relations:

$$\kappa_T^2 = 1 - \frac{C_{static}}{C_{free}}$$

where C_{static} and C_{free} are defined as:

$$C_{static} = \frac{Q(x)}{V}; x_{DC}, V_{DC}$$

$$C_{free} = \frac{dQ(x)}{dV}; x_{DC}, V_{DC}$$

As a consequence of reduced parasitic and static capacitance, κ_T^2 is calculated with capacitance method and for the CMUT with oxide support is around 0.5 while the regular CMUT coupling factor is about 0.4 for 25V DC. The coupling coefficient calculation with resonance frequency method (Fig. 7) demonstrates similar results.

The AC device impedance, functionality and characteristics of the CMUT was also measured with network analyzer (Agilent 8753ES). Fig. 7 depicts the impedance of the CMUT in air under different DC bias voltages from 0V to 25V. The resonance frequency of the device is around 12MHz in the air that is expected based on our model [17] and it is lowered with increasing DC bias due to spring softening effect.

C. Acoustic Characterization

The devices with oxide support were also tested in water tank to verify functionality as an acoustic transducer. Fig. 8 shows the output pressure measured by a hydrophone (HGL-1000 series hydrophone, ONDA Corp., Sunnyvale, CA 94089) when the CMUT array element was used as a transmitter and was excited with a 50ns long 30V pulse with no DC bias. The measured center frequency is about 9 MHz with 65% fractional bandwidth, in very good agreement with the simulations [18, 17] and suitable for the ICE application. The dip around 5.3MHz predicted in the simulations is due to crosstalk resonance that would be more pronounced in a perfectly uniform array, whereas in the fabricated device it is less pronounced due to unavoidable non-uniformities [23]. The disturbance seen around 14MHz is due to the silicon substrate ringing which is not considered in the simulations.

D. Reliability Testing

Repetitive pulsing and DC bias in CMUTs can accumulate charge in the isolation layer which degrades the device performance and will reduce the hydrophone output pressure [13]. Since reducing this non-ideal behavior was one of the goals of the lift-off oxide support CMUT structure, the devices were subjected to a long term transmit pressure measurement test. Both CMUTs with and without the oxide support were excited with 55ns long, 30V pulse over 10V DC bias with 100kHz repetition rate and the pressure output at 5mm distance from CMUT is recorded hourly. The measurements were repeated on 16 array elements coming from 4 different wafer locations with lift-off oxide support and 20 array elements coming from 4 different wafer locations without oxide support. All the array elements with oxide support were functional over 2×10^{11} vibration cycles. A typical result for an oxide lift-off device showing about 5% output pressure change in 72 hours is shown

in Fig. 9. For devices without oxide support, the time to failure was below 5×10^{10} cycles or about 10 hours with the best case shown in Fig. 9. This set of results demonstrates the improvement in reliability achieved by using the lift-off oxide supports in CMUT fabrication. In order to demonstrate the environmental robustness of the newly designed CMUT, the output pressure of the CMUT has been recorded while the water tank temperature is set to 50°C and the device is continually excited with 55ns long, 30V pulse over 10V DC bias with 1MHz repetition rate. Note that the peak voltage level is 125% of the collapse voltage of the CMUT which may be needed for practical transmit operation [19]. Fig. 10 illustrates the hydrophone output voltage of the CMUT during this particular experiment. The pressure output changes less than 4% over about 4.5×10^{10} cycles during this period, corresponding to 2,500 hours of use which is suitable for a single use catheter based imaging application.

V. Discussion

The presented results demonstrate a feasible approach that can be applied to CMUTs fabricated with sacrificial release process. The two key advantages of this approach are the use of low-temperature fabrication technique and minimum manipulation in the device structure. In terms of the dielectric material and thickness used for the lift-off process several issues need to be considered. Since the added capacitor is in series with the isolation layer capacitor (Fig. 1-b), a dielectric with lower relative permittivity is preferred. Low temperature deposited dielectrics such as HfO_2 , TiO_2 , Si_3N_4 have relatively large dielectric constants. Although some polymers [24] like Teflon, Polyimide and Fluorinated polyimide have smaller (2.5 – 3) dielectric constants as compared to SiO_2 (3 – 3.5), the ease of fabrication and CMOS compatibility indicates that silicon dioxide is a suitable material. The silicon dioxide deposition temperature is limited to less than 110°C because of the photoresist thermal sensitivity. This reduces the quality of the oxide layer with high pinhole density, but sputtering and atomic layer deposition (ALD) systems which may provide higher quality films could not be used due to the side wall coverage. It is worth noting that although lift-off is a usual fabrication technique for patterning metal films, some successful attempts have been accomplished in dielectric and PZT materials patterning [25, 26, 27]. Overall, the results show that evaporated silicon dioxide is a suitable material.

The benefit of lift-off over the regular deposition and patterning is the self-alignment and ease of fabrication. The thickness of lift-off dielectric is chosen to reduce the step height that is caused by bottom electrode (Fig. 2-c). The edge effect in dielectric lift-off is less than the metal lift-off due to the low density [27]. Besides, considering relatively low thickness of the oxide and 75% top electrode coverage on the membrane, edge effect does not significantly impact the fabrication process.

The breakdown voltage of the thin isolation layer limits the maximum voltage applied to CMUTs. This should be higher than the transient high voltages which may exceed the static collapse voltage. The experiments reported here show that the reliability is maintained with total transient voltage levels as high as 125% of the collapse voltage. Even the gap is increased to enable higher collapse and pulse voltages the dielectric layer thickness used here should suffice. For example, using a lift-off step with a 200–220 nm of SiO_2 on top of

200nm silicon nitride (4MV/cm breakdown field) [28] would provide a breakdown voltage of 170V, sufficient for typical CMUT applications, and it does not introduce a large topography causing any TE step coverage issues.

VI. Conclusion

A low temperature, sacrificial layer based fabrication process for CMUTs is modified for improved reliability and higher coupling efficiency. This is achieved by depositing a dielectric layer (SiO₂) in the region where bottom and top electrodes overlap except for the membrane region and using a lift-off process without an additional mask. Measurements on identical devices with and without the lift-off silicon dioxide support indicated improvements in parasitic capacitance and consequently the coupling coefficient. The acoustic performance of the devices have been compared to simulations and long term output pressure measurements at room and elevated temperatures showed no significant degradation on performance indicating that this simple addition to the low temperature sacrificial CMUT fabrication process can help mitigate the charging issues for catheter based CMUT imaging devices.

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Fig. 1.

a) Cross section of a conventional surface micromachined CMUT with thin isolation layer over TE-BE overlap area. b) Proposed lift-off based process where an extra layer of dielectric is deposited over TE-BE overlap area without impacting the gap thickness.

Fig. 2.

Schematic of fabrication process flow, (a) starting with a silicon wafer, thick oxide following by a BE layer are deposited. (b) Sacrificial layer (Cu) is deposited and pattern. (c) A dielectric layer is evaporated and lifted-off (d) Isolation dielectric is deposited using PECVD. (e) Top electrode layer is sputtered. (f) Dielectric layer is deposited and etched, the sacrificial layer is entirely removed, and the CMUT is dried up using super critical dryer or oven. (g) Membrane is thickened to the final thickness.

Fig. 3.

Optical image of oxide lift-off process, Fig. (a) is the 1-D CMUT array suitable for intracardiac echocardiography, (b) is a single 1-D element. In the Fig. (c), the green parts are the regions where the oxide is lifted-off on top of copper sacrificial layer. Fig. (d) is the final CMUT fabricated using the improved method.

Fig. 4.

Top: Black line shows the cross section used for SEM. Bottom: I) oxide between BE-TE overlap, II) BE (Cr), III) dielectric isolation, IV) gap (Cu). The SEM cross section showing a deposition of silicon dioxide ($\sim 217\text{nm}$) between 2 adjacent membranes. The color of silicon dioxide is different from silicon nitride under the SEM.

Fig. 5. AFM measurement on the membrane. The maximum displacement of 15.6-nm occurs at center of the membrane.

Fig. 6.
The C-V curve of the two CMUT array elements which are identical except for the oxide support.

Fig. 7. Measured electrical input impedance of the devices in air, (a) real part and (b) imaginary part. The resonance frequency is about 12 MHz in air and it reduces with increasing DC bias.

Fig 8.

Comparison of simulated and measured pressure signals (a) in time domain, (b) in frequency domain, for 1-D CMUT element with 80 membranes. The input is 50ns long 30V pulse.

Fig. 9. Long-term operation test results. Hydrophone output is measured over 72 hours while the devices were excited with 55ns long, 30V pulse over 10V DC bias with 100kHz repetition rate.

Fig. 10.

Environmental reliability test results. Hydrophone output is recorded while the devices were excited with 55ns long, 30V pulse over 10V DC bias with 1MHz repetition rate.

TABLE I

CMUT Properties

Parameter	Value
Membrane size	46-um * 46-um
Electrode area	38-um * 38-um
Device center frequency in immersion	9 MHz
Vacuum gap (d)	95-nm
Dielectric relative permittivity (ϵ_r)	6.3
Si ₃ N ₄ isolation thickness	200-nm
SiO ₂ relative permittivity	2
SiO ₂ thickness	220-nm
No. of membrane per element	80
Collapse voltage	32v
BE (Cr) thickness	250-nm
TE (Al) thickness	200-nm
Sacrificial layer (Cu) thickness	110-nm
Membrane Thickness	2.2 um