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2048 Action Potential Recording Channels with 2.4 μV_{rms} Noise and Stimulation Artifact Suppression

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Abstract

Here, we present 2048 low-noise, low-offset, and low-power action-potential recording channels, integrated in a multi-functional high-density microelectrode array. A resistively loaded open-loop topology has been adapted for the first-stage amplifier to achieve 2.4 μV_{rms} noise levels at low power consumption. Two novel pseudo-resistor structures have been used to realize very low HPF corner frequencies with small variations across all channels. The adjustability of pseudo resistors has been exploited to realize a “soft” reset technique that suppresses stimulation artifacts so that the amplifiers can recover from saturation within 200 μs . The chips were fabricated in a 0.18 μm 6M1P CMOS process, and measurement results are presented to show the performance of the proposed circuit structures and techniques.

I Introduction

The possibility to simultaneously record from many individual neurons or a network, and to electrically stimulate specific neurons are desirable features of microsystems targeted at studying neuronal networks, their interconnections and electrophysiology [1] [2]. However, extracellular electrodes have to pick up weak analog signals, so that neural amplifiers with sufficient gain, appropriate bandwidth, high signal-to-noise ratio (SNR), high common-mode and power-supply rejection ratios (CMRR and PSRR) are needed. Furthermore, to enable the realization of thousands of units on the same chip, an individual neural amplifier should feature low power consumption and small chip real estate. Another highly desirable feature includes stimulation artifact suppression in order to reveal spikes right after stimulation or to improve the efficacy of closed-loop stimulation.

This paper presents work on recording channels, which have been integrated in a multi-functional microelectrode array (MEA) system featuring 59,760 microelectrodes, as shown in Fig. 1 [3]. Different recording channel architectures have been integrated for capturing two types of neural signals, action potentials (APs, with typical amplitudes $< 1\text{ mV}$, bandwidth: 300 Hz $\sim$ 6 kHz) and local field potentials (LFPs, amplitudes $< 5\text{ mV}$, bandwidth: 1 Hz $\sim$ 300 Hz). Here, we focus on the action-potential recording channels and circuits. Each channel consists of four stages. The first-stage amplifier features a resistively loaded open-loop topology to achieve low noise levels. Two novel pseudo-resistor structures with low resistance variations across channels have been devised. These pseudo resistors

have been used to realize the high-pass filtering in the first two stages, which removes low-frequency drifts of electrode potentials and keeps the offset of the recording channels within an acceptable range without the need of dedicated offset calibration circuitry. Furthermore, the corner frequencies of the high-pass filters (HPFs) can be tuned through their bias currents to compensate for process variations. During stimulation, these bias currents can be set to much larger values, which yields kHz-range HPF corner frequencies and enables a fast recovery of the recording channels from saturation due to stimulation artifacts.

II Design of Action Potential Recording Channels

A Gain Stages

As shown in Fig. 2, all four stages of the AP recording channel adopt fully differential structures to suppress interferences from power supplies and the substrate. The total gain of each channel can be programmed in steps of 6 dB from 29 dB to 77 dB to accommodate a broad variety of experimental scenarios. The first-stage amplifier (A1) features a resistively loaded open-loop topology. Traditional neural amplifiers employ closed-loop topologies with high-gain OTAs, which normally use NMOS transistors as active loads. However, NMOS transistors typically have a much higher $1/f$ -noise level than PMOS transistors. In contrast, resistors do not contribute $1/f$ noise, and generate less thermal noise. Therefore, the open-loop topology can achieve a similar noise level with less power consumption. To tune the gain of A1, its differential pair and tail current source have been divided into four equal parts. In the normal configuration, all four parts are turned on, and a maximum gain is achieved. The gain can be reduced to $1/2$ or $1/4$ of its maximum value by turning off 2 or 3 parts of the differential pair and tail current source, and adjusting the load resistance (R_L) accordingly. To alleviate possible large gain variations of the open-loop topology, a constant-gm biasing circuit has been used to generate the tail current of A1. By matching the resistors and PMOS transistors in both, the biasing circuit and A1, a uniform gain can be achieved across all channels.

The second-stage amplifier features a closed-loop structure, as shown in Fig. 2. This structure provides an accurate gain of $A_{V2} = C_1 / C_2$ and can handle larger signal swings than the first stage. In comparison to the first stage, the gm of the input transistors can be reduced, as the noise requirement is largely relaxed. Therefore, less capacitance is needed to realize anti-aliasing filtering in this stage. The load capacitor C_3 can be tuned to set the LPF corner frequency to be around 6 kHz.

Both, the third and fourth stages have been implemented with switched-capacitor amplifiers, which are able to achieve low distortion levels for large signal swings. Using the switched-capacitor structure, it is also easier to implement multiplexing (8-to-1 in front of both, the third and fourth stage) in comparison to continuous-time amplifiers. Thus, 64 neural signals can be sampled at 20 kS/s and digitized by a 10-bit 1.28 MS/s successive-approximation-register (SAR) ADC. As 8 or 64 channels share the third or fourth stages and ADCs, the corresponding circuitry area and power consumption are relatively small, as compared to the first two amplification stages.

B Pseudo-Resistors and High-Pass Filtering

As shown in Fig. 2, a first-order high-pass filter (HPF) has been implemented in the first two stages. In the first stage, the HPF removes low-frequency drifts of the electrode potentials. In the second stage, the HPF removes the offset of A1. Due to the DC feedback through the pseudo-resistors, R_{PR2} , the offset of A2 is reduced by its closed-loop gain. This offset is further reduced by the gain of the first stage when referred to the electrode. Measurement results showed that the maximum input-referred offset of all AP channels was less than 0.011 mV without additional offset compensation/calibration circuitry (Fig. 4.b).

However, a huge resistance ($T\Omega$) is required to build the two HPFs with very low corner frequencies ($f_{HPF} < 10$ Hz). In conventional neural amplifiers, so called “pseudo-resistors” (MOS transistors biased in the weak-inversion region) have been widely used, but they usually feature large process- and temperature variations, and poor linearity. In this work, two new pseudo-resistor structures have been devised (Fig. 2). For the pseudo-resistor used in the first stage (R_{PR1}), the gate voltages of both, PMOS and NMOS transistors are generated by the PMOS and NMOS current mirrors. For the pseudo-resistor in the second stage (R_{PR2}), a structure as proposed in [4] has been adopted. However, an NMOS-only level shifter has been used to generate the gate voltages of the transistors M1 and M2 instead of a PMOS level shifter in [4]. In both pseudo-resistor structures, the first-order dependence of the overdrive voltages of the transistors inside R_{PR1} and R_{PR2} on their threshold voltage has been cancelled out. Thus, their resistance variations were substantially smaller than those of conventional structures. In addition, both R_{PR1} and R_{PR2} were designed to be symmetrical around their common-mode voltage, which entails a good linearity.

The resistance of the two pseudo resistor structures was found to be almost inversely proportional to their bias currents. This feature provides the additional benefit that f_{HPF} can be easily tuned by varying the bias currents, which can be used to accommodate different experimental scenarios or reduce process and temperature variations. Here, the bias current was digitally tuned with a 7-bit current DAC, which adopts a MOSFET-only R-2R ladder structure [5], results in a very compact design. As the DAC is shared among 16 channels, the area overhead is negligible.

C Stimulation Artifact Suppression

As stimulation signals are on the order of hundreds of mV, the amplifier chain can easily saturate during stimulation. Moreover, the very large time constant associated with the HPF prolongs the recovery process. Some designs include reset switches in parallel to the pseudo resistors in order to speed up recovery, but the charge injection and leakage current caused by the reset switches set a lower limit for the recovery [6]. Other designs disconnect the recording circuits from the electrode and reconnect them after the stimulation artifact vanishes [7]. However, this procedure assumes that the electrode voltage returns to its original value prior to stimulation, which is not always true.

In this work, the adjustability of the pseudo-resistors was exploited to realize a so-called “soft” reset technique. Within a small time-window before and after the stimulation pulse has been applied, the bias currents of the pseudo-resistors were set to much larger values

than those during normal operation so that the f_{HPFS} were increased to the kHz range. As the associated time constants became much smaller and the amplifier gain got reduced, the first two stages did not saturate during stimulation. This enabled fast amplifier recovery and the detection of APs within less than 200 μ s after stimulation.

III Layout and Fabrication

The 2048 recording channels have been divided into two groups and placed at the top and bottom sides of the electrode array in the multi-functional MEA, whose micrograph is shown in Fig. 3. Then, every 64 channels were grouped in one block with shared logic and bias circuits. Shielded lines were placed between two neighboring channels to reduce cross-talk. The multi-functional MEA was fabricated in a 0.18 μ m CMOS process (6M1P). Platinum electrodes were post-processed at wafer level by using ion-beam deposition and etching. The die measures 12 $\times$ 8.9 mm², while the 2048 recording channels including ADCs occupied 44.8 mm². The silicon area of one individual channel was about 0.022 mm².

IV Measurements

A custom software was developed to generate different settings and download them to the chip through an SPI interface. The output data frames from the chip were acquired using an NI PXIe-6544 high-speed DAQ card. A LabVIEW program was implemented to visualize/save the acquired bit stream of every channel, and the data were post-processed in MATLAB.

The input-referred noise PSD of the whole recording channel including the ADC is shown in Fig. 4.a. The integrated noise in the AP band was 2.4 μ Vrms. The SAR ADC achieved an SNDR of 56.2 dB at a sampling rate of 1.28 MS/s and an input signal frequency of 1.1 kHz. The measured maximum gain of the recording channel was 76.4 dB. The spread of the gain across all channels was characterized by applying a common sinusoidal signal to all inputs. The presented open-loop topology with constant-gm biasing achieved a very good gain uniformity with a standard deviation of 0.14 dB. The measured maximum input-referred offset ranged from -110μ V to 70 μ V as shown in Fig. 4.b. The gain and transfer function of the recording channels are shown in Fig. 4.c. The histogram plot shows the uniformity of f_{HPF} , which indicates a good matching of the pseudo resistors across all 2048 channels.

For bio-measurements, dissociated cortical cells of embryonic-day-18 Wistar rats were cultured during 3-4 weeks on the chip. Recorded neuronal APs are shown in Fig. 5.a. Extracellular APs of an identified neuron shows an $SNR; [\max(V_{rec}) - \min(V_{rec}) / 2 \times \sigma_{noise}] > 100$. All experiments were conducted inside an incubator at a constant temperature of 37 °C and at 5% CO₂.

Biphasic voltage pulses (positive first) with 40 μ s per phase and a peak-to-peak amplitude of ± 500 mV were generated by an on-chip DAC and then applied to the stimulation electrode using a voltage buffer. The effect of this large stimulation amplitude is clearly visible on the neighboring electrodes. In Fig. 5.b, the signals recorded from four adjacent electrodes (distance of 13.5 μ m) are shown with and without applying the “soft” reset technique. The reset signal was applied 100 μ s before and 100 μ s after the stimulation pulse.

Without “soft” reset, the amplifier was saturated for about 13 ms, and no action potential could be recorded during this period. With “soft” reset, the amplifier signals came back immediately, and APs could be recorded as soon as 200 μ s after the stimulation pulse. This recovery time is shorter than that reported in [8], which amounted to 500 μ s on 400 μ m-distant electrodes.

V Conclusions

The AP readout channels featured competitive noise characteristics of 2.4 μ Vrms in the AP band (300 Hz - 10 kHz) with a low power consumption of 16 μ W per channel. The channels achieved an offset range of less than 0.11 mV without any additional offset compensation/calibration circuitry. To the best of our knowledge, the stimulation artifact recovery time of 200 μ s is faster than anywhere reported to date [6] [7] [8].

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Figure 1.
Microelectrode array system

Figure 2.

Amplifier gain stages, schematic of the first stage OTA (A1) and the pseudo-resistors.

Figure 3.
Chip micrograph

Figure 4.

a) Noise PSD of the amplifier including ADC. b) Offset distribution of the 2048 AP channels. c) Gain, transfer function and f_{HPF} distribution of all readout channels.

Figure 5.

a) Extracellular action potential of an identified neuron on the high-density electrode array. Top: 10 traces averaged, bottom: raw single signal traces recorded from the electrode marked with the arrow. b) Recorded raw traces around the stimulation site with (blue) and without (red) "soft" reset applied. Amplifier gain setting: 58.3 dB.