Video Article

Electric-field Control of Electronic States in WS₂ Nanodevices by Electrolyte Gating

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Abstract

A method of carrier number control by electrolyte gating is demonstrated. We have obtained WS₂ thin flakes with atomically flat surface via scotch tape method or individual WS₂ nanotubes by dispersing the suspension of WS₂ nanotubes. The selected samples have been fabricated into devices by the use of the electron beam lithography and electrolyte is put on the devices. We have characterized the electronic properties of the devices under applying the gate voltage. In the small gate voltage region, ions in the electrolyte are accumulated on the surface of the samples which leads to the large electric potential drop and resultant electrostatic carrier doping at the interface. Ambipolar transfer curve has been observed in this electrostatic doping region. When the gate voltage is further increased, we met another drastic increase of source-drain current which implies that ions are intercalated into layers of WS₂ and electrochemical carrier doping is realized. In such electrochemical doping region, superconductivity has been observed. The focused technique provides a powerful strategy for achieving the electric-field-induced quantum phase transition.

Video Link

The video component of this article can be found at <https://www.jove.com/video/56862/>

Introduction

Control of the carrier number is the key technique for realizing the quantum phase transition in solids¹. In the conventional field effect transistor (FET), it is achieved by use of the solid gate^{1,2}. In such a device, electric potential gradient is uniform throughout the dielectric materials so that induced carrier number at the interface is limited, shown in **Figure 1a**.

On the other hand, we can achieve the higher carrier density at the interface or bulk by replacing the solid dielectric materials with ionic gels/liquids or polymer electrolytes^{3,4,5,6,7,8,9,10,11} (**Figure 1b**). In the electrostatic doping by use of the ionic liquid, electric double layer transistor (EDLT) structure is formed at the interface between ionic liquid and sample, generating strong electric field (>0.5 V/Å) even at low bias voltage. Resultant high carrier density (>10¹⁴ cm⁻²) induced at the interface^{10,12,13} cause the novel electronic properties or quantum phase transition such as electric-field-induced ferromagnetism¹⁴, Coulomb blockade¹⁵, ambipolar transport^{16,17,18,19,20,21,22,23,24,25,26,27}, formation of p-n junction and resultant electroluminescence^{28,29,30}, large modulation of thermoelectric powers^{31,32}, charge density wave and Mott transitions^{33,34,35}, and electric-field-induced insulator-metal transition^{36,37} including electric-field-induced superconductivity^{9,10,11,38,39,40,41,42,43,44,45,46,47,48,49}.

In the electrolyte gating (**Figure 1c**), ions are not only accumulated at the interface to form EDLT, but can be also intercalated into layers of two-dimensional materials via thermal diffusion without damaging sample under applying the large gate voltage, leading to the electrochemical doping^{8,9,11,34,38,50,51,52,53}. Thus, we can drastically change the carrier number compared to the conventional field effect transistor using the solid gate. In particular, the electric-field-induced superconductivity^{9,11,34,38,50} is realized by use of electrolyte gating in region of large carrier number where we cannot access by the conventional solid gating method.

In this article, we introduce this unique technique of carrier number control in solids and overview the transistor operation and electric-field-induced superconductivity in semiconducting WS₂ samples such as WS₂ flakes and WS₂ nanotubes^{54,55,56,57}.

Protocol

1. Dispersion of WS₂ Nanotubes (NTs) on substrate

1. Disperse WS₂ NT powders into isopropyl alcohol (IPA, concentration more than 99.8%) with proper diluted ratio (about 0.1 mg/mL) by sonication for 20 min.
NOTE: The long-time sonication helps to make WS₂ NTs uniformly suspended in IPA liquid and to separate well-formed individual WS₂ NTs from amorphous WS₂ or other junks, as well as to remove the garbage accumulating on WS₂ NTs surface. **Figure 2b** shows the final suspension of WS₂ NTs. Since the suspension might be heated up during the sonication process, it is better to stop sonication at every 5 min and continue sonication after 1 min.
2. Spin-coating procedure to disperse WS₂ NTs on substrate.
 1. Start the spin-coater machine and vacuum pump. Put a Si/SiO₂ (3000 Å) substrate (1 cm x 1 cm) on the center of the chuck and fix it by vacuum with pumping speed of 80 L/min and ultimate pressure of 20 kPa.
NOTE: There is a hole located at the center of the chuck connecting to the vacuum pump, thus the substrate is fixed by vacuum pressure (pumping speed is 80 L/min and ultimate pressure is 20 kPa). The vacuum pressure can be different depending on the pump.
 2. Set relevant parameters of the procedure by control panel of the spin-coater machine.
NOTE: There are three steps during the spin-coating procedure: (1) slowly speed up to 500 rpm within the first 3 s, (2) rapidly speed up to 4000 rpm and continue for 50 s, (3) slow down and stop spinning for the last 3 s. Those parameters can be different depending on the use of spin-coater.
 3. Put one droplet (about 0.01 mL) of the suspension of WS₂ NT made in (1.1) by a pipette onto the substrate until the substrate is fully covered by the suspension (if not, put more droplets). Then start spin-coating with relevant parameters in (1.2.2).

2. Preparation of thin flake on substrate via scotch tape method

1. Put a small bulk sample of WS₂ (grown via chemical vapor transport method) on scotch tape. Fold the scotch tape and unfold it slowly to mechanically exfoliate the thin layer from the bulk. Repeat this procedure for several times, until the exfoliated samples are thin enough.
NOTE: **Figure 2g** and **2h** show the initial tape with little bulk sample of WS₂ and the final tape after multiple folding procedures, respectively.
2. Paste the scotch tape on the top of substrate upside down, slightly press the tape, and carefully remove the tape from the top of substrate.
NOTE: After removing the tape, there are many thin flakes left on the substrate.

3. Device fabrication by electron beam lithography.

1. Spin-coating process to cover the resist for electron beam lithography.
 1. Follow the same spin-coating procedure described in (1.2.1) and (1.2.2).
 2. Put one droplet (about 0.04 mL) of polymethyl methacrylate (PMMA) by a pipette onto the substrate until the substrate is fully covered by PMMA. Then start spin-coating procedure to uniformly cover PMMA on WS₂ sample to prevent it from being exposed in air.
Note: PMMA is one of the resists for electron beam lithography.
 3. After spin-coating, put the substrate on hot-plate at 180 °C and heat it for 1 min.
NOTE: Those parameters can be different depending on resist types.
2. Sample selection by optical microscopy.
 1. Start the optical microscopy and camera. Put the substrate on the stage.
 2. Move stage and scan the whole region of the substrate with proper magnification (20X) and in the meantime, select isolated samples with suitable size.
Note: In total, 6 to 10 isolated samples can be usually selected for each substrate of 1 cm x 1 cm.
 3. Take photos of each selected sample with different magnification of 5X, 20X, and 100X. Those photos are used to identify the location of each sample.
3. Design of the large-scale device pattern.
 1. Activate the AutoCAD software, and load the format of substrate lattice. Insert photos taken in (3.2) and identify the size and location of each photo depending on the marks on the substrate.
 2. Insert a large square with length of 1200 μm and a small square with length of 300 μm which should surround each sample.
 3. Design large-scale patterns including gate, source, drain, and other pads in the large square except for fine structures near the sample. Design small marks close to the sample to precisely identify the location of the samples in the later process of design for the small-scale device pattern.
 4. Repeat (3.3.2) to (3.3.3) for every sample.
 5. Record the coordinates of the center of each large and small square, respectively.
 6. Delete inserted photos, large and small squares, and substrate lattice format, leaving only the designed large patterns and small marks. Export large patterns and small marks as dxf files, respectively.
4. First electron beam lithography.
 1. Put the substrate on the stage and fix it, and insert the stage into the main chamber of electron beam lithography machine.
 2. Activate ECA program (a program for generating a file used in electron beam process). Set field size as 300 for the lithography of small marks. Use tool of dxf converter to transfer dxf file to cell file.
 3. Load the cell file generated in (3.4.2), enter the file name, identify origin and identify points with coordinates of small squares noted in (3.3.5). Finally, identify the coordinates of large A and B marks and small A and B marks for each point.

Note: The large A and B marks are used to correct the direction of stage, while small A and B marks are used to identify the mismatch between designed pattern and printed pattern, during the process of small-scale pattern design.

4. Save the file as con file and wait until the pressure inside the main chamber is lower than 5×10^{-5} Pa.
NOTE: Because the electron beam is high energy (50 kV of accelerating voltage), the high quality of vacuum is needed.
5. When the pressure of the main chamber becomes low enough for the electron beam lithography process, activate electron beam control program ESL-7500 and subsequently turn on the electron gun.
6. Turn on the scanning electron microscope (SEM) and move the stage to the position where the substrate is in the screen. Tune the brightness, contrast, and focus.
7. Adjust the angle of the stage by judging from the relative position of large A and B marks originally designed on the substrate until the error of direction is negligible at magnification of 5000X. After correcting the direction of the stage, register the position of the large A mark.
8. Set the amplitude of electron beam for lithography; 100 pA is for small marks lithography. Move the stage to the position for amplitude tuning and select the spot mode for the camera, change the amplitude of electron beam until it reaches 100 pA by ampere meter. After setting the amplitude of electron beam, tune the brightness, contrast, and focus.
9. Load saved con file in (3.4.4) in the ECA program. Set relevant parameters: 2 s for dose time and 300 for field size. Finally start the exposure process.
Note: Dose time can be different depending on the resist.
10. Back to electron beam control program ESL-7500, set 5000X of magnification and move the stage to the registered position of the large A mark. Confirm the position of the large A and B marks.
11. Set 30000X of magnification and confirm the position of small A and B marks for the lithography of the first small marks designed in (3.3.3).
Note: The lithography starts after conforming small marks and takes several second.
12. After finishing the lithography, repeat this procedure for all samples. At the last, quit the exposure process and close the ECA program.
13. Follow the same process from (3.4.2) to (3.4.10) with different parameters for the lithography of the large pattern designed in (3.3.3). In (3.4.2), set field size as 1200. In (3.4.3), only identify coordinates of large A and B marks except for small A and B marks. In (3.4.8), set the amplitude of electron beam as 1000 pA for the lithography of the large pattern. In (3.4.9), select 1200 of field size.
Note: After the process of (3.4.10), the lithography of the large pattern starts and takes several hours.
14. After finishing the lithography of the large pattern, move the stage to the original position, turn off the electron beam, and quit the exposure process and the ECA program. Open the main chamber and take out the substrate.

5. First developing.

1. Make a solution of methyl isobutyl ketone (MIBK) and IPA with the ratio of MIBK: IPA = 1: 3. Dip the substrate in the solution for 30 s, and wash it by IPA liquid and dry it by nitrogen gun.
NOTE: Developing time may change depending on the environmental conditions such as temperature and humidity.
2. Take photos by optical microscopy for each printed pattern with different magnification of 5X, 20X, and 100X.

6. Design of small-scale device pattern.

1. Follow the same process in (3.3). In (3.3.1), load the pattern of substrate lattice including the designed small marks in (3.3.3), and insert photos taken after first developing.
NOTE: The size and location of each photo depends on the small marks designed in (3.3.3), instead of marks on the substrate.
2. Design the fine structure of device pattern with source, drain and other electrodes in small squares in a Hall bar configuration, which is connected to the printed large pattern. After designing small patterns for all the devices, record the coordinates of small squares.
3. Delete inserted photos, small squares, and substrate pattern, leaving only the designed small patterns. Export the small pattern as dxf file.

7. Second electron beam lithography.

1. Follow the same process from (3.4.1) to (3.4.11) with the same parameters for the lithography of the small pattern designed in (3.6); set 300 for field size and select 100 pA for the amplitude of electron beam.
NOTE: The lithography process takes several minutes for each small pattern.
2. After the lithography of small pattern, move the stage to the original position, turn off the electron beam, quit the exposure process and close the ECA program. Open the main chamber and take out the substrate.

8. Second developing.

1. Follow the same process in (3.5) with the same developing time as 30 s.
2. Take photos by optical microscopy for each pattern with different magnification of 5X, 20X, and 100X.

4. Deposition of electrodes

1. Deposition of gold electrodes.

1. Fix the substrate on substrate holder, put the substrate holder on transfer rod, and insert it into the main chamber of the evaporator. Start rotating the substrate holder.
2. First deposit Cr of 5 nm in thickness as the adhesion layer. When the pressure inside the main chamber becomes less than 10^{-4} Pa, turn on the high voltage source.
3. Increase the current of electron gun carefully with the fixed accelerating voltage of 4 kV, until the depositing rate measured by thickness monitor becomes stable about 0.5 Å/s (usually pre-evaporate Cr of about 5 nm).
4. Open the shutter and deposit Cr until it reaches 5 nm in thickness. Close the shutter, slowly decrease the current of electron gun to zero, and turn off the high voltage source.

5. Subsequently deposit Au of appropriate thickness. Turn on the current source and slowly increase the current up to 30 A. Evaporate Au by keeping the current of 30 A, until the depositing rate measured by thickness monitor becomes stable about 1 Å/s (usually pre-evaporate Au of about 10 nm).
 6. Open the shutter and start depositing Au. After reaching the intended thickness, close the shutter, slowly decrease the current to zero, and turn off the current source.
Note: We use 60 nm for thin flake and 90 nm for NT. The appropriate thickness is depending on the sample.
 7. Since the substrate is heated up during deposition process, remain the substrate inside the chamber for 1 h in order to cool down its temperature to near room temperature. Stop rotating the substrate holder and take it out by transfer rod.
2. Deposition of SiO₂ protection layer.
 1. With the help of optical microscopy, cover the pads and the gate electrodes by tape.
NOTE: In principle, only the fine structures of electrodes are exposed to deposit SiO₂ layer for the protection of electrodes against the chemical reaction during the electrolyte gating.
 2. Follow the same process from (4.1.1) to (4.1.4) to deposit Cr of 5 nm in thickness as adhesion layer.
 3. Subsequently follow the same process from (4.1.1) to (4.1.4) to deposit SiO₂ of 20 nm in thickness.
Note: The depositing rate of SiO₂ is about 1 Å/s, while pre-evaporating SiO₂ of about 10 nm.
 4. Cool down the substrate inside the chamber for 1 h. Stop rotating the substrate holder and take it out by the transfer rod. Remove the tape under microscopy.

5. Completion of the device

1. Substrate scribing.
 1. Turn on the scribing machine and vacuum pump with pumping speed of 50 L/min and ultimate pressure of 30 kPa. Fix the substrate on the stage by vacuum chuck and adjust the angle and position of the substrate.
 2. Scribe the substrate into small pieces (usually about 3 mm x 3 mm).
Note: The size of each piece is depending on the location of each selected sample and the designed pattern.
2. Device lift-off.
 1. Select one device and immerse it into acetone (concentration more than 99.5%) for 1 h at room temperature to remove the redundant PMMA and gold. Only the fabricated electrodes are left on substrate.
 2. After the lift-off process, wash the substrate by IPA and dry it by nitrogen gun.
3. Wire-bonding.
 1. Turn on the wire-bonding machine. Fix the substrate on the chip-carrier via sliver paste.
NOTE: For WS₂ NT case, we use horizontal rotator shown in **Figure 2n**.
 2. With the help of wire-bonding machine, connect each electrode pad and electrode of chip carrier one by one with a gold wire.
4. Electrolyte droplet putting.
 1. Put a droplet of electrolyte (less than 0.5 μL) on the top of device by a tweezer after dipping in the electrolyte liquid.
NOTE: The amount of electrolyte is very little; it covers the fine structure of device and gate pad but avoids covering the electrode pads. We use the electrolyte of KClO₄ (concentration more than 99%) dissolved in polyethylene glycol (PEG; Mw = 600) with a [K]:[O] ratio of 1:20 according to the previous publication³⁸.

6. Transport measurements

1. Fix the chip-carrier on the sample holder, and put it inside the chamber of physical properties measurement system by the transfer rod. Pump the chamber by the high vacuum mode.
2. Connect measurement system including lock-in amplifiers, nano-voltmeter, source meter, and amplifier. Apply a constant alternating current (AC) with the frequency of 13 Hz to perform the AC-lock-in measurements.
3. Run the Keysight VEE program (measurement programs).
4. In the measurement of gate response, when the gate voltage is applied to the electrolyte (*i.e.*, between source and gate electrodes), sweep the gate voltage with speed of 50 mV/s at 300 K, under high-vacuum condition to reduce the influence of the air on the gating performance.
5. In the measurement of temperature dependence of resistance, first cool down to 200 K with the cooling rate of 1 K/min in high-vacuum condition, and then change to the He-purged condition and keep cooling down to 10 K with the cooling rate of 1 K/min. When the temperature is lower than 10 K, cool down and warm up with the rate of 0.2 K/min.
Note: In the He-purged condition, the thermal conductance and resultant temperature stability is better than those in high-vacuum condition.

Representative Results

The typical transistor operations of an individual WS₂ NT and a WS₂ flake devices are shown in **Figure 3a** and **3b**, respectively, where the source drain current (I_{DS}) as a function of the gate voltage (V_G) nicely operates in an ambipolar mode, showing a remarkable contrast to the unipolar gate response by the conventional solid gated FET in previous publication⁵⁸. Considering the ambipolar behavior is reversible and repeatable, these transistor operations are likely due to the electrostatic doping. In the electrostatic doping, ions are accumulated on the surface of the samples, which leads to the large electric potential drop and resultant carrier doping at the interface (**Figure 1b**).

Electrochemical doping by the intercalation (**Figure 1c**), on the other hand, is realized in large gate voltage region, causing much higher electron concentration in the bulk of the sample, instead of on the surface of the sample by electrostatic doping. A typical intercalation process is shown in the **Figure 3c**. When the gate voltage is firstly increased up to 8 V with a constant rate of 50 mV/s, I_{DS} displays a saturation behavior indicating the electrostatic doping, similarly to the 2D WS_2 case as shown in **Figure 3b**. When the gate voltage is kept at 8 V for a couple of minutes, another drastic increase of I_{DS} by more than two orders of magnitude has been observed as shown in **Figure 3c**. This source drain current increase is presumably attributed to intercalation of K^+ ions diffusing into WS_2 layers without damaging the crystal structure. This process causes much higher carrier concentration in the bulk compared with the electrostatic doping at the surface.

As shown in **Figure 3d**, the similar intercalation process is also realized in WS_2 flake. When the gate voltage is firstly increased up to 6 V, I_{DS} displays a similar saturation behavior. On the other hand, carrier density estimated by Hall effect does not significantly change, displaying the similar saturation behavior. When the gate voltage becomes higher than 6 V, I_{DS} increases again because of the occurrence of intercalation which is proofed by the clear increase of the carrier density.

Temperature dependences of the resistance of WS_2 NTs and flakes after electrochemical doping are shown in the **Figure 3e** and **3f**, respectively. In both cases, the resistance shows the metallic behavior and superconductivity appears in low temperature region.

Figure 1: Illustration of electrolyte gating. (a) The schematic figure of conventional field effect transistor by solid gate. (b) The schematic figure of electrostatic doping by electrolyte gating. By take placing the solid dielectric intermedium into electrolyte, the electrostatic doping effect is more efficient since the dielectric constant of liquid is much larger than solid. A large number of carriers are accumulated on the surface of sample. (c) The schematic figure of electrochemical doping by electrolyte-gating-induced intercalation. The positive ions are intercalated into sample, inducing much more carriers in the bulk. [Please click here to view a larger version of this figure.](#)

Figure 2: Device fabrication of WS₂ nanotube and flake. (a) and (b) WS₂ NT, which was first powder configuration, are dispersed into IPA liquid. (c) The photograph of an individual WS₂ NT selected by optical microscopy after dispersion of WS₂ NT onto the substrate and covered by PMMA. (d) The schematic figure of the designed pattern for WS₂ NT by AutoCAD. (e) The photograph of the device pattern of an individual WS₂ NT after electron beam lithography process and developing process. (f) The photograph of the device of an individual WS₂ NT after deposition of electrodes. (g) and (h) The photograph of WS₂ bulk samples on a tape, and the photograph of exfoliated WS₂ samples after folding and unfolding tape several times. (i) The photograph of a WS₂ flake selected by optical microscopy after transferring it onto the substrate and covered by PMMA. (j) The schematic figure of the designed pattern for a WS₂ flake by AutoCAD. (k) The photograph of the device pattern of a WS₂ flake after electron beam lithography process and developing process. (l) The photograph of the device of a WS₂ flake after deposition of electrodes. (m) The photograph of an isolated device after scribing process and lift-off process. The typical device pattern of the device for electrolyte gating is shown. In addition to electrodes for transport measurements, a side gate was positioned near the sample. (n) The photograph of the device on the horizontal rotator after wire-bonding process. (o) The photograph of the device after wire-bonding process. (p) The photograph of device for electrolyte gating with a droplet of ionic liquid on the top covering both sample and the side gate electrodes. (q) The photograph of typical measurement systems (PC and physical properties measurement system). [Please click here to view a larger version of this figure.](#)

Figure 3: Transistor operation, electrochemical intercalation, and electric-field-induced superconductivity in WS₂ nanotube and flake device. (a) The ambipolar transfer curve of WS₂ NT at 300 K. Source-drain voltage V_{DS} is 0.2 mV and sweeping speed of gate voltage V_G is 50 mV/s. (b) The ambipolar transfer curve of WS₂ flake at 300 K. V_{DS} is 0.1 V and sweeping speed of gate voltage is 20 mV/s. (c) Source-drain current I_{DS} as a function of V_G and waiting time during the electrochemical intercalation in WS₂ NT. A saturation behavior of I_{DS} has been observed when increasing V_G , and a second dramatically increase of I_{DS} has been observed at fixed V_G during waiting couple of minutes. (d) I_{DS} at 300 K (left) and carrier density estimated by Hall effect at 200 K (right) as a function of V_G in the WS₂ flake. Saturation and second increase of I_{DS} has been also observed in the flake. The carrier density shows the large increase in large V_G region, indicating the intercalation process. (e) Temperature dependence of resistance of WS₂ NT after intercalation process. Superconducting transition has been observed at 5.8 K. (f) Temperature dependence of resistance of WS₂ flake after intercalation process. Superconducting transition has been observed at 8 K. All the figures have been reproduced and modified from Qin, F. *et al.* and Shi, W. *et al.*^{38,50} [Please click here to view a larger version of this figure.](#)

Discussion

In both WS₂ NTs and flakes, we have successfully controlled the electric properties by electrostatic or electro chemical carrier doping.

In electrostatic doping region, ambipolar transistor operation has been observed. Such ambipolar transfer curve with a high on/off ratio ($>10^2$) observed in low bias voltage indicates the effective carrier doping at the interface of electrolyte gating technique for tuning the Fermi level of these systems.

Although this method is as advantageous for tuning large amount of carrier number in small gate bias compared with the conventional solid gating method, there are several limitations of this technique. First, because the carrier number control is realized via liquid gate, it is not able to tune the carrier number below the frozen temperature of electrolyte/ionic liquid^{12,28,29,30}. Conventional solid gate, on the other hand, is valid for even low temperature, although it is not as efficient as electrolyte/ionic liquid gate in high temperature (near room temperature). Second, many materials are known to show the chemical reaction with electrolyte/ionic liquid in specific conditions^{59,60,61,62,63}. Such chemical reaction easily breaks the devices and limits the successful ratio of experiments or application to the materials.

However, people have recently recognized that the chemical reaction might help for the future application, such as chemical etching for thinning films^{59,60} and electrochemical intercalation for heavily electron doping^{9,11,34,38,50,51,52,53} and phase transformation^{61,62,63}. A similar technique has been also adapted for solid ion conductor^{51,52,53} and even photoactive EDLT has been developed⁶⁴.

In the electrochemical doping region, we have observed the electric-field-induced superconductivity. The difference of the superconducting transition temperature between WS₂ NTs and flakes, which is possibly due to the lower dimensionality of NTs, should be further pursued in the future.

As clearly demonstrated in the results of this study, carrier number control by the ionic liquid gating provides a powerful method for searching the quantum phase transition in nanomaterials.

Disclosures

The authors have nothing to disclose.

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