Published in final edited form as:

Proc SPIE Int Soc Opt Eng. 2011 January ; 7901: . doi:10.1117/12.874729.

Ultra-miniature wireless temperature sensor for thermal medicine applications

Ahmad Khairi^a, Shih-Chang Hung^a, Jeyanandh Paramesh^a, Gary Fedder^a, and Yoed Rabin^a

^aCarnegie Mellon University, 5000 Forbes Ave., Pittsburgh, Pa, 15213

Abstract

This study presents a prototype design of an ultra-miniature, wireless, battery-less, and implantable temperature-sensor, with applications to thermal medicine such as cryosurgery, hyperthermia, and thermal ablation. The design aims at a sensory device smaller than 1.5 mm in diameter and 3 mm in length, to enable minimally invasive deployment through a hypodermic needle. While the new device may be used for local temperature monitoring, simultaneous data collection from an array of such sensors can be used to reconstruct the 3D temperature field in the treated area, offering a unique capability in thermal medicine. The new sensory device consists of three major subsystems: a temperature-sensing core, a wireless data-communication unit, and a wireless power reception and management unit. Power is delivered wirelessly to the implant from an external source using an inductive link. To meet size requirements while enhancing reliability and minimizing cost, the implant is fully integrated in a regular foundry CMOS technology (0.15 μm in the current study), including the implant-side inductor of the power link. A temperature-sensing core that consists of a proportional-to-absolute-temperature (PTAT) circuit has been designed and characterized. It employs a microwatt chopper stabilized op-amp and dynamic element-matched current sources to achieve high absolute accuracy. A second order sigma-delta ($\Sigma\Delta$) analog-to-digital converter (ADC) is designed to convert the temperature reading to a digital code, which is transmitted by backscatter through the same antenna used for receiving power. A high-efficiency multi-stage differential CMOS rectifier has been designed to provide a DC supply to the sensing and communication subsystems. This paper focuses on the development of the all-CMOS temperature sensing core circuitry part of the device, and briefly reviews the wireless power delivery and communication subsystems.

Keywords

Wireless; CMOS; temperature sensor; inductive power delivery; minimally invasive surgery; cryosurgery; hyperthermia; thermal ablation

1. INTRODUCTION

As a part of an ongoing effort to develop devices and technique to improve the outcome of thermal surgery, this study focuses on an early-stage development of a miniature, wireless, and battery-less temperature sensor. Thermal surgery applications are conveniently classified with respect to temperature, with cryosurgery as the destruction of tissue by freezing, and hyperthermia and thermal ablation as the destruction of tissue at moderately and extreme elevated temperatures, respectively. While tissue injury mechanisms and criteria for thermal

surgery success vary with temperature, the difficulties associated with reconstructing the temperature field in the minimally invasive thermal procedure are essentially the same.

1.1 Minimally Invasive Cryosurgery

Cryosurgery has been developed since the 1930's, when technological advances led to commercial production of liquefied air and nitrogen. It was introduced as an invasive procedure for the first time in 1961, with the development of the cryoprobe by Copper and Lee. As a minimally invasive procedure, cryosurgery experiments were conducted in the mid 1980's, following technological developments in medical imaging.

While cryosurgery has been applied to virtually any tissue of the body as a method of treatment, prostate cryosurgery was the first minimally invasive cryosurgical procedure to pass from the experimental stage to become a routine surgical treatment [14–16]. The minimally invasive approach created a new level of difficulty in cryosurgery, in which a well defined 3D shape of tissue must be treated, while preserving the surrounding tissues. To overcome this difficulty, an array of minimally invasive cryoprobes is inserted into the target region. With recent technological developments in Joule-Thomson cooling, the diameter of the cryoprobe has been dramatically decreased and the number of cryoprobes has been increased so that more than a dozen cryoprobes can be applied simultaneously. If localized effectively, one of the potential benefits of the use of a large number of miniaturized cryoprobes is superior control over the freezing process.

With the dramatic increase in the number of cryoprobes, two new challenges in cryosurgery have arisen: (i) how to shape the frozen region and restrict the destructive freezing effect to the target area, and (ii) how to correlate the developing thermal field with established criteria for cryosurgery success. Currently, surgery control relies upon ultrasound imaging, where one or two hypodermic thermocouples may be used for additional temperature feedback. However, hypodermic thermocouples are cumbersome to operate, and display high uncertainty due to heat conduction along the hypodermic needle, which makes the wired sensors during prostate cryosurgery unpopular. The current study addresses these challenges by developing a superior means for real-time feedback on the developing thermal field.

1.2 Minimally Invasive Hyperthermia and Thermal Ablation

Tissue exposure to elevated temperatures leads to a sequence of events, depending on the temperature level and exposure time, essentially resulting in thermal injury. Unlike cryosurgery, there is no clear and immediate demarcation of the injured region—such as the correlation with the freezing front in cryosurgery—and evaluation of thermal injury is more complicated. Exposure to temperatures above 43°C is commonly referred to as “hyperthermia”, whereas exposure to temperatures above 56°C is frequently referred to as “thermal ablation.” In an effort to provide a unified and representative value to the time-temperature exposure to heat, the concept of thermal dose has been introduced, which represents the equivalent exposure time to 43°C [20]. While comparison of different values of thermal dose may be debatable, as different injury mechanisms may be involved at various temperatures, the thermal dose remains the single most used parameter in the context of hyperthermia and thermal ablation. The thermal dose can either be computed from

bioheat simulations of the thermal ablation procedure, or compiled from experimental data; either way it is proportional to the integral of the elevated temperature over time.

A common treatment of thermal ablation to prostate cancer is by means of high intensity focused ultrasound (HIFU; sometimes FUS or HIFUS). This application is typically performed under MRI guidance. Current clinical trials are underway, examining the possible use of the technique in the treatment of cancers of the brain, breast, liver, bone, and prostate.

One of the most significant hurdles in controlling hyperthermia is the lack of knowledge of thermal dose distribution in general, and in real time in particular. While thermal dose could be computed in real time with no significant computation cost, it is the temperature data that is missing for this task. The current study offers a solution to this hurdle by distributing an array of miniature temperature sensors in the domain to be treated.

1.3 Miniaturization of Implantable Microelectronics

The scaling of on-chip electronics and the attendant reduction in size and power consumption has led to a variety of miniature implantable systems for medical applications. Perhaps the most famous ultra-miniature implantable is the BION, developed by the Alfred Mann Foundation (AMF) [9]. The BION is a 15.6 mm-long by 2.3 mm in diameter ceramic-encased implantable neuro-stimulator system, which has the potential to improve conditions from stroke and spinal cord injuries, as well as migraines, epilepsy, and obesity. The latest AMF hermetically sealed unit includes a rechargeable battery, a wound coil for recharging at 125 kHz, and the stimulator integrated circuit [22]. The system also includes a temperature sensor, using the principle of transistor junction dependency, similar to the one integrated in the current study.

Another type of implantable is the neural recording array, which has been recently developed by several groups across the U.S. [11,19]. The collaborative effort between the University of Utah and Stanford University has resulted in the development of the Hermes-B [19] system, which employs the Utah Microelectrode array [12] to probe neural signals at locations 400 μ m apart. The array measures ~8mm $\times$ 8mm and houses 100 probes. An integrated circuit [8] mounted on the rear side of the array performs the following functions: (1) amplification, conditioning, and thresholding of the recorded “spikes”; (2) spike sorting; and, (3) wireless transmission of the recorded data to a remote interface. Power is delivered to the chip by inductively coupling power at 2.64MHz from an external coil to an on-implant 5mm $\times$ 5mm coil. Data communication employs a separate antenna in the 433MHz range. Electrical stimulation and multi-channel high-bandwidth neural interface applications consume far more power than required for the developed low-bandwidth temperature sensing application in the current study.

2. TEMPERATURE SENSOR OVERVIEW

With the exception of the thermocouple, electronic temperature sensors exploit the temperature-dependency of physical devices and use electronic conditioning circuitry to produce a temperature reading in analog or digital form. Such devices range from passive

resistive devices to active MOSFET and bipolar devices. This section provides an overview of several temperature-sensor circuits, which could be considered design alternatives.

2.1 Metal-oxide-semiconductor (MOS) delay-based temperature sensor

The digital temperature sensor utilizes a time to digital converter (TDC) to measure the temperature-dependent delay of a digital inverter and provide a digital reading proportional to the temperature. The delay of a CMOS inverter with equal pull-up and pull-down strengths is given in Eq. (1) [7], where D is the inverter delay, L and W are the length and width of either the NMOS or PMOS device, μ and V_{TH} are the mobility and threshold voltage of the same device, C_L is the load capacitance, C_{OX} is the gate capacitance per unit area and V_{DD} is the supply voltage.

$$D = \frac{L}{W} \frac{C_L}{C_{OX}} \frac{1}{\mu} \frac{\ln(3 - 4V_{TH}/V_{DD})}{V_{DD}(1 - V_{TH}/V_{DD})} \quad (1)$$

The work by Woo *et al.* shows that the delay displayed in Eq. (1) is temperature-dependant and is proportional to $T^{-\alpha}$, where T is the temperature and α is proportionality constant. That design uses two delay locked loops (DLLs): the first locks a chain of inverters to an external crystal temperature-independent oscillator, and the second locks a temperature-dependant delay generated by a chain of inverters to a known multiple of the temperature-independent delay of the first DLL. As a result, the temperature reading is proportional to the number of delay stages locked. Using standard cells commonly available in foundry CMOS technologies, the same concept has been demonstrated but with a different circuit topology [3,4].

2.2 Complementary MOS (CMOS) temperature sensor

A CMOS temperature sensor utilizes temperature-dependant parameters of a MOS device. Here, temperature-sensing is based on the temperature-dependence of the threshold voltage V_{TH} and gain factor $\beta = \mu_{eff} C_{OX} W/L$ of a MOS device [21,24]. Figure 1 displays the four-transistor circuit used in [21]. If this circuit is biased so that the following potentials are equal V_{OUT1} , V_{OUT2} , V_{OUTX} , and also the following currents are equal I_1 , I_2 , I_X , then the output voltage V_{OUTX} becomes:

$$V_{OUTX} = \sqrt{\frac{2I_X}{\beta_2}} + V_{TH2} + \sqrt{\frac{2I_X}{\beta_3}} + V_{TH3} \quad (2)$$

When I_X/β is designed to be temperature-independent, the output voltage V_{OUTX} is directly proportional to the threshold voltage of the two devices M_2 and M_3 , which is temperature-dependant. Here, the threshold voltage V_{TH} is:

$$V_{TH} = \phi_{ms} + 2\phi_f + \frac{Q_d}{C_{OX}} + \frac{\sqrt{2q\epsilon_s N_{sub}(2\phi_f - V_{BS})}}{C_{OX}} \quad (3)$$

In Eq. (3), Φ_{ms} is the difference in the work function between the silicon substrate and the polysilicon gate of a MOS transistor, Q_d is the diffusion charge, C_{OX} is the gate capacitance per unit area, N_{sub} is the substrate doping concentration, V_{BS} is the bulk source junction voltage, q is the electronic charge, and ϵ_s is the electrical permittivity of silicon. The main temperature dependence of V_{TH} comes from the Φ_f term, which is equal to:

$$\phi_f = \frac{kT}{q} \ln \frac{N_{sub}}{n_i}; n_i \propto T^{\frac{3}{2}} e^{-\frac{E_g}{2kT}} \quad (4)$$

2.3 Bipolar Junction Transistor (BJT) temperature sensors

A simple BJT temperature sensor is displayed in Figure 2, consisting of PNP BJT's Q_1 and Q_2 . The terminals are marked on each BJT: C for collector, B for base and E for emitter. In a PNP BJT, the emitter-base voltage (V_{BE}) is a function of temperature and collector current (I_C) as shown in Eqs. (5) and (6), where k is Boltzmann's constant, q is the elementary charge, E_g is the band-gap energy, A is the emitter's cross sectional area, N_D is the donor concentration in the base, W_B is the base width from the base-emitter depletion layer edge to the base-collector depletion layer edge, m^* is approximately $-3/2$ for lattice scattering, and b is a constant factor that depends on the doping and the geometry of the device.

$$V_{BE}(T, I_C) = V_T \ln \frac{I_C}{I_S}; V_T = \frac{kT}{q} \quad (5)$$

$$I_S(T) = \frac{qAD_p n_i^2}{W_B N_D} = bT^{4+m^*} e^{-\frac{E_g}{qV_T}} \quad (6)$$

The difference between $V_{BE1}(T)$ and $V_{BE2}(T)$ —labeled as V_{BE} in Figure 2—is proportional to absolute temperature (PTAT) with a proportionality constant n , which is dependent upon the ratio of the collector currents in the two transistors and upon the ratio of the saturation currents m of the two transistors labeled:

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = V_T \ln \frac{nI_C}{I_S} \times \frac{mI_S}{I_C} = V_T \ln nm \quad (7)$$

A basic circuit implementation of a BJT temperature sensor is depicted in Figure 3. The circuit consists of two equally sized bipolar devices (Q_1, Q_2) whose emitter currents are equal to nI_B and I_B , respectively. This current ratio is set equal to n through the ratio of the

two PMOS devices and the negative feedback loop created by operational amplifier. The unit bias current I_B , indicated in the figure, will be equal to V_{BE}/R_B , assuming an ideal op-amp. If R_B is temperature-independent, then I_B is PTAT. Since the unit-bias current for this circuit is PTAT, the collector currents of the two BJT's are also PTAT. For a PTAT collector current, $V_{BE}(T)$ of both devices has the temperature coefficient shown in Eq. (8) [18].

$$\frac{\partial V_{BE}(T)}{\partial T} = \frac{V_{BE} - 3 + m * V_T - E_g/q}{T} \quad (8)$$

$$V_{BE}(T_2) = \left(1 + \ln \frac{T_1}{T_2}\right) V_{BE}(T_1) + \frac{E_g}{q} \ln \frac{T_1}{T_2} + \frac{k}{q} 3 + m * (T_1 - T_2) \quad (9)$$

Equation (8) shows that the temperature coefficient is dependent upon the magnitude of V_{BE} and the temperature. For example, for $V_{BE} = 650$ mV at room temperature, the temperature coefficient is -1.7 mV/K. By applying Eq. (9), it can be deduced that V_{BE} will approximately equal 850 mV at 200 K and that the temperature coefficient will equal -1.5 mV/K. From the above discussion, it is further deduced that $V_{BE}(T)$ is negatively proportional to absolute temperature. One can approximate $V_{BE}(T)$ as having a linear dependency on temperature, as shown in Figure 4.

Figure 4 also depicts the positive temperature coefficient of $V_{BE}(T)$ indicated by Eq. (7). Furthermore, Figure 4 shows that a temperature-independent voltage (V_{ref}) can be achieved by taking the sum $\alpha V_{BE}(T) + V_{BE}(T)$, where α is a scaling factor equal to the ratio of the slopes of $V_{BE}(T)$ and $V_{BE}(T)$ functions. This voltage is called the *bandgap voltage* since it has a value equal to the bandgap voltage of silicon (E_g/q) at absolute zero.

A BJT can be realized in a CMOS process as depicted in Figure 5. The emitter is a $p+$ region similar to that used for the source and drain of a PMOS device. The base is an n-well, which is accessed through an $n+$ implant in the n-well similar to that used to bias the bulk of a PMOS device. The collector is the p-substrate. This device suffers from two major disadvantages: (i) the p-substrate collector connects to the chip's ground and cannot be controlled in an n-well-only CMOS process, and (ii) this device suffers from a limited forward current gain β , which is defined as the ratio of the collector current to the base current. Methods to overcome this limitation are discussed in Section 3.

3. TEMPERATURE SENSOR DESIGN

An illustration of a typical temperature sensor suggested by Bakker *et al* [2] is displayed in Figure 6. The circuit consists of three components, the analog temperature sensor, the reference voltage, and the analog to digital converter (ADC). This overall structure is generic and can be applied to any of the circuits discussed in the Section 2 of this paper. For voltage-based temperature sensors, such as CMOS and BJT temperature sensors, the bandgap voltage (V_{ref}) introduced in the previous section, is an excellent candidate for a reference voltage.

A novel temperature sensor with a digital output that eliminates the explicit generation of the reference voltage has been proposed by Petrijs *et al* [17] and is shown in Figure 7. This circuit uses the BJT temperature sensor as its front end. The inputs to the circuit are the same $\alpha V_{BE}(T)$ and $V_{BE}(T)$ discussed in the previous section. It can be shown that, due to charge balancing at the input, the output μ is equal to:

$$\mu = \frac{\alpha \Delta V_{BE}}{\alpha \Delta V_{BE} + V_{BE}} = \frac{\alpha \Delta V_{BE}}{V_{ref}} \quad (10)$$

The following subsection analyzes the errors in the digital temperature readout μ , caused by different sources of uncertainty in the BJT temperature sensing core of Figure 3, generating $V_{BE}(T)$ and $V_{BE}(T)$. The resulting μ can be re-written as follows:

$$\mu = \frac{\alpha \Delta V_{BE}}{\alpha \Delta V_{BE} + V_{BE}} = \frac{\alpha \ln n}{\alpha \ln n + \ln[\gamma I_B / I_S]} = \frac{\alpha k \ln n}{q V_{ref}} T \quad (11)$$

where α is the scaling factor introduced in section 2.3, n is the current ratio of the two PNP transistors, I_S is the saturation current of the PNP transistors, I_B is the unit bias current as specified in Figure 3, and $\gamma = \beta(1 + \beta)$, where β is the forward current gain of the PNP transistors.

3.1 Sensitivity Analysis

The digital output μ of the temperature sensor, given by Eq. (11), is a function of several circuit parameters and can be written as $\mu(\alpha, n, \gamma, I_B, I_S)$, where each argument represents a physical circuit parameter that has a known (typically normal) statistical distribution. Therefore, the nominal value $\mu_{NOM} = \mu(\alpha_{NOM}, n_{NOM}, \gamma_{NOM}, I_{BNOM}, I_{SNOM})$. The sensitivity of $\mu(\alpha, n, \gamma, I_B, I_S)$ with respect to its independent variables can be studied by evaluating the

normalized difference $\varepsilon_\mu = \frac{\Delta \mu}{\mu_{NOM}} = \frac{\mu_{NOM} - \mu(\alpha, n, \gamma, I_B, I_S)}{\mu_{NOM}}$, where ε_μ has contributions from five normalized differences ($\varepsilon_\alpha, \varepsilon_n, \varepsilon_\gamma, \varepsilon_{IB}, \varepsilon_{IS}$). In the expression for the resulting difference ε_μ , given by Eq. (12), the values of the terms $\mu_{NOM}^2 / \alpha_{NOM} \ln n_{NOM}$ and $\ln[\gamma_{NOM} I_{BNOM} / I_{SNOM}]$ are about 0.01 and 25 at room temperature, respectively. Normalized differences in γ, I_B and I_S (i.e., $\varepsilon_\gamma, \varepsilon_{IB}, \varepsilon_{IS}$) will result in a $0.01 \times$ normalized difference in μ . On the other hand, the normalized differences in α and n (i.e., $\varepsilon_\alpha, \varepsilon_n$) will result in a $0.25 \times$ normalized difference in μ . This means that the circuit is more sensitive to α and n than it is to γ, I_B and I_S .

Since the unit-bias current I_B is a function of the primitive circuit parameters as expressed in Eq. (13) where R_B and V_{OS} are the bias resistor and offset voltage, respectively (Figure 3), A_{DM} is the finite differential DC gain of the op-amp, $CMRR$ is the finite common-mode rejection ratio of the op-amp (defined as A_{DM}/A_{CM} where A_{CM} is the common mode gain), V_{DD} is the supply voltage, and V_{TH} is the threshold voltage of the PMOS device M_I . When the nominal I_B is equal to $V_{BE,NOM}/R_{B,NOM}$, the current difference term (ε_{IB}) can be

expressed as presented by Eq. (14). This equation indicates that a difference in resistance R_B from its nominal value, translates to an equal difference in the bias current from nominal. The equation does not include the difference between the nominal resistance $R_{B,NOM}$ and the actual value which is dependent on spreads due to the CMOS manufacturing process. However, this difference is corrected by batch calibration, after which, only mismatch differences need to be considered. Resistance is also a function of temperature so, there will be a spread in resistance due to temperature. The current implementation uses low temperature coefficient resistors to allow for minimization of this difference.

$$\varepsilon_\mu \approx \frac{\mu_{NOM}^2}{\alpha_{NOM} \ln n_{NOM}} \left(\varepsilon_\gamma + \varepsilon_{I_B} + \varepsilon_{I_S} + \varepsilon_\alpha + \varepsilon_n \ln \left[\gamma_{NOM} \frac{I_{B,NOM}}{I_{S,NOM}} \right] \right) \quad (12)$$

$$I_B \approx \frac{\Delta V_{BE}}{R_B} + \frac{V_{OS}}{R_B} + \frac{V_{DD} - |V_{TH}|}{A_{DM} R_B} - \frac{1}{CMRR} \left(\frac{V_{BE1} + V_{OS}}{R_B} \right) \quad (13)$$

$$\varepsilon_{I_B} \approx \varepsilon_{R_B} + \frac{V_{OS}}{\Delta V_{BE}} + \frac{V_{DD} - |V_{TH}|}{A_{DM} \Delta V_{BE}} - \frac{1}{CMRR} \left(\frac{V_{BE1} + V_{OS}}{\Delta V_{BE}} \right) \quad (14)$$

In addition to resistance, variations in I_B arise from op-amp input referred offset due to mismatches in the op-amp. The last two terms in Eq. (14) relate to the gain of the op-amp and common mode rejection ratio. Since these parameters are normally maximized in a circuit for given power budget and circuit topology, and due to their large variability, the analysis of these parameters implies setting a constraint on their minimum values. This will effectively ensure that mismatch differences after calibration will also meet the I_B overall accuracy requirement.

Variations in μ effectively translate into uncertainty in temperature reading (T). From Eq. (11), the temperature T is derived from μ by using the nominal values for V_{ref} , n , and α , resulting in the overall sensitivity expression given in Eq. (15).

$$\varepsilon_T \approx \frac{V_T}{V_{ref}} \left(\varepsilon_\gamma + \varepsilon_{I_S} + \varepsilon_{R_B} + \frac{V_{OS}}{\Delta V_{BE}} + \frac{V_{DD} - |V_{TH}|}{\Delta V_{BE} A_{DM}} - \frac{1}{CMRR} \left(\frac{V_{BE1} + V_{OS}}{\Delta V_{BE}} \right) \right) + \frac{V_{BE}}{V_{ref}} \varepsilon_\alpha + \varepsilon_n \quad (15)$$

Results generated by means of Eq. (15) may be better appreciated by evaluating the absolute errors in temperature measurement calculated as the product of T_{NOM} and ε_T , as displayed in Table 1.

3.2 Error Mitigation techniques

3.2.1 Dynamic Element Matching—Dynamic element matching (DEM) is a method to reduce errors in the current ratio n [1,8], which are caused by transistor mismatches in the current sources implemented by the PMOS devices (Figure 8). Applying a common-centroid layout technique can reduce device mismatches. However, Eq. (15) indicates that current ratio error needs to be less than 0.1%. in order to bring the temperature error to less than 0.1K. DEM can help achieve that target by periodically redistributing the current from $(n+1)$ nominally identical current sources to the BJT pair (n being the desired current ratio). At each clock cycle, a different current source is used to supply the I_B and the remaining current sources are used to supply the nI_B .

Assuming that all current sources (PMOS devices in Figure 8) supply a current equal to nominal current value and an offset $I_B + \delta I_{Bk}$ ($k = 0 \dots n$) over $n+1$ clock cycles, the average current flowing into the emitter of Q_4 is equal to $I_B + 1/n \sum_k \delta I_{Bk}$ and the average current flowing into the emitter of Q_3 is equal to $nI_B + \sum_k \delta I_{Bk}$. The average current ratio is equal to n irrespective of the offset terms, as long as the offset terms are fixed or slowly changing compared to the DEM period.

3.2.2 Chopping—As discussed in section 2.1, the major contributor to temperature uncertainty is the offset voltage of the op-amp. Op-amp offset is defined as the required input differential voltage to produce a zero-output differential voltage. Op-amp offsets are of two kinds: systematic and random. Systematic offsets are functions of the structure and biasing of the op-amp and can be minimized by careful design. On the other hand, random offsets are the result of device mismatches during manufacturing. While such errors can be reduced by an improved layout, they may still be significant and a must be minimized using special techniques.

In order to reduce the contribution of V_{OS} to the overall temperature uncertainty, a chopping technique is used. Chopping consists of periodically interchanging the positive and negative terminals of the differential input and outputs of a circuit. This operation is depicted in Figure 9 $V_{OUT} = -A(V_{IN} + V_{OS})$ during phase Φ_1 , and $V_{OUT} = -A(V_{IN} - V_{OS})$ during phase Φ_2 . Hence, $V_{OUT} = -A(V_{IN} + V_{OS} \cos(2\pi f_0 t))$, where f_0 is the chopping frequency.

Figure 10 depicts the effect of chopping in the frequency domain. The input signal is chopped by commutating at frequency f_0 . The input referred offset voltage of the op-amp add to the chopped input. The output of the op-amp is chopped yielding two results: (1) the output corresponding to the input signal is down-converted to the input signal's band, and (2) the output corresponding to offset (and to the low-frequency components of the input-referred noise the op- amp) is up-converted into f_0 . Effectively, chopping moves low frequency noise to a higher frequency part of the spectrum, which can be filtered out. It is important to note that since thermal noise is white noise, chopping does not affect it.

Figure 8 displays the chopping architecture adopted in the current design. This chopping architecture does not only chop the input referred low-frequency noise of the op-amp, but also chops the DC offsets due mismatches between Q_1 and Q_2 [1].

3.2.3 Adjusting for Limited Bipolar Gain—As stated in Eq. (11), the temperature reading depends upon the forward current gain β of bipolar devices. Spreads in β and its temperature dependency lead to uncertainties in the measured temperature. In order to reduce these uncertainties, the BJT's Q_3 and Q_4 in Figure 8 are biased with $I_B = V_{BE}(\gamma R_B)$, where $\gamma = \beta/(\beta+1)$ [1]. It follows that μ , and hence the temperature reading, are β -independent as presented in Eq. (16).

$$\mu_{\text{NOM}} = \frac{\alpha \ln n}{\alpha \ln n + \ln \gamma \frac{1}{I_S} \frac{\Delta V_{BE}}{\gamma R_B}} = \frac{\alpha \ln n}{\alpha \ln n + \ln \frac{\Delta V_{BE}}{I_S R_B}} \quad (16)$$

The circuit displayed in Figure 8 is based on the BJT pair Q_1 and Q_2 to generate such current. The resistor $R_{BETA} = R_B/n$ is connected between the base of nI_B bipolar device and the ground. Assuming an ideal op-amp, the voltage across the op-amp input terminals will have to be at 0 V (*i.e.*, a virtual short) and the resulting bias current will be β -independent:

$$I_B = \frac{\Delta V_{BE}}{\gamma R_B} \quad (17)$$

4. POWER DELIVERY

An inductively-coupled power delivery interface will provide power to the electronics on the implant. An external battery-powered transmitter acts as the power source. An inductive power delivery link simplifies the implantation of the sensors and allows the sensors to act as standalone devices. The circuit in Figure 11 displays a model of the wireless link.

The power efficiency of the link, η , defined as the ratio of the DC power delivered to the load to the power supplied to the transmitter, (*i.e.*, the power amplifier (PA) in Figure 11) is a convenient metric to evaluate its performance. η is the product of three factors: (1) the power efficiency of the rectifier, (2) the power efficiency of the inductive link, and (3) the power efficiency of the power amplifier.

The efficiency of the power amplifier is the ratio of the power it delivers to the primary coil to the power it draws from the battery and the input source. Due to the “constant-envelope” nature of its input, a highly efficient switching topology may be envisioned.

The efficiency of the wireless power link depends on several factors including the geometry of the coils, the mutual geometry between the coils, their quality factors at the operating frequency and the source and load resistances seen at the terminals of the inductive link. The efficiency η_{link} is shown in Eq. (18), where R_p , R_s , L_p , and L_s are the primary and secondary coil resistances and inductances, respectively, and where R_L is the load impedance looking into the rectifier as indicated in Figure 11, R_i is the source impedance looking back into the power amplifier as indicated in Figure 11, ω is the angular frequency, k is the coupling factor—equal to $M/L_p L_s$, where M is the mutual inductance and Q is the quality factor defined in Eq. (19).

$$\eta_{\text{link}} = \frac{1}{1 + \underbrace{\frac{(1+R_i/R_p)}{k^2 Q_p Q_s} \left[2 + \frac{R_s}{R_L} + \frac{\omega^2 L_s^2}{R_L R_s} + \frac{R_L R_s}{\omega^2 L_s^2} \right]}_{\text{TERM1}} + \underbrace{\frac{1}{Q_s} \left[\frac{\omega L_s}{R_L} + \frac{R_L}{\omega L_s} \right]}_{\text{TERM2}}} \quad (18)$$

$$Q = \frac{\omega L}{R} = \frac{2\pi f L}{R} \quad (19)$$

As can be inferred from Eq. (18), the efficiency is a function of the frequency, even when ignoring the frequency dependence of the resistances. In this application, the secondary coil is integrated on chip hence it has a much lower quality factor than the primary coil. However, the coupling factor k can be very low. Hence if $k^2 Q_p \gg 1$, *TERM2* will dominate in Eq. (18); when $k^2 Q_p \ll 1$, the *TERM1* will dominate Eq. (18). When *TERM1* dominates, the term $k^2 Q_p Q_s$ needs to be maximized at $\omega = (R_L R_s)/L_s$. Since R_s/R_L will also need to be maximized, the optimal frequency is expected to be very low in this case. The efficiency in this case will approximately be $k^2 Q_p Q_s / (4 + k^2 Q_p Q_s)$. If *TERM2* is dominant, then Q_s needs to be maximized at the frequency $\omega = R_L/L_s$, at which case the efficiency will approximately equal $Q_s / (2 + Q_s)$. In both cases, the ratio R_i/R_p should be minimized. In both cases, maximizing the quality factors and the coupling coefficient is desirable. In this application, methods to improve the quality factor of the integrated coil are investigated including micromachining methods of substrate etch and metal deposition in order to reduce the effective resistance of the on chip inductor.

A rectifier is often realized in a CMOS process using diode-connected transistors. The efficiency of the rectifier is proportional to the difference between the input amplitude and the turn-on voltage due to switch resistance and reverse conduction. The power efficiency also depends on the output voltage and it often is necessary to have multiple stages of rectifiers to achieve a certain required output voltage given an input signal amplitude. Figure 12 shows the single stage of the differential-drive CMOS rectifier circuit [10]. The circuit forms by a cross-coupled differential CMOS configuration. The operation of the single stage rectifier is described below. V_{RF}^+ and V_{RF}^- are differential AC signals which are large enough to turn the cross-coupled transistors on and off. When V_{RF}^+ goes high and V_{RF}^- goes low, a small on-resistance of M_2 and M_3 and larger off-resistance of M_1 and M_4 results. The current steers into V_{OUT}^+ through M_3 and out V_{OUT}^- through M_2 . When changing polarity for V_{RF}^+ and V_{RF}^- , the current steers into V_{OUT}^+ and out V_{OUT}^- through the opposite path but in the same direction. Therefore, a DC voltage is developed across the load resistance between V_{OUT}^+ and V_{OUT}^- that is equal to $2V_{RF} R_L / (R_{ON} + R_L)$.

5. WIRELESS COMMUNICATION

Backscatter has been used in the field of radio frequency identification devices (RFIDs) [5,23]. Backscatter changes the characteristics of the reflected wave seen by the transmitter at the input to the power transmitter by modulating the load at the sensor. This operation can

take place while the transmitter is transmitting power in continuous wave form. Figure 14 shows the high-level schematic of this circuit. A receiver at the sensor extracts a clock from the power signal's frequency and extracts any data transmitted alongside.

Data sent to the sensor is used to select one sensor to communicate at a time in an array of sensors. The data is transmitted from the power transmitter to the sensor in the form of output power modulation. The power transmitted is modulated between full scale continuous wave and no power transmission. The period of this communication link has to be designed carefully to allow the sensor to maintain enough power storage for operation.

The digital temperature reading is coded to improve the communication quality by lowering the bit error rate. The coded output is mixed with an IF frequency. The IF frequency is locked to the extracted clock for accuracy and minimal variation due to temperature. The mixed signal is transmitted using backscatter telemetry. The signal is sensed by the power transmitter, down converted to baseband and then decoded. Figure 14 shows this operation in time domain [13]. The continuous wave is maintained at all times apart from when the power transmitter is transmitting data. Backscatter is observed during power transmission.

6. CONCLUSION

An ultra-miniature, implantable, wireless temperature-sensor, with applications in thermal medicine has been presented. The need for such sensors in thermal medicine applications to overcome current technology limitations in the field of cryosurgery and, independently, to overcome hurdles in applications of hyperthermia and thermal ablation has been established. The paper focuses on temperature-sensing circuit design, shedding light upon different circuits that can be utilized. A thorough study of a two-transistor BJT based temperature-sensor is performed to account for the circuit's sensitivity to different circuit non-idealities and mismatches. Several techniques to overcome those design barriers are presented, which include a chopper stabilized op-amp and dynamic element-matched current sources. Wireless power delivery is a major component of the temperature-sensor's system. An overview of the different components of the wireless power delivery sub-system has been presented and the most significant design considerations for each component have been addressed. A wireless communication sub-system has been presented. The system uses backscatter telemetry and the corresponding communication protocol has been introduced.

Acknowledgments

This project has been supported by Award Number R21EB009370 from the National Institute of Biomedical Imaging and Bioengineering. The content is solely the responsibility of the authors and does not necessarily represent the official views of the National Institute of Biomedical Imaging and Bioengineering or the National Institutes of Health.

References

1. Aita AL, Pertijs M, Makinwa K, Huijsing JH. A CMOS smart temperature sensor with a batch-calibrated inaccuracy of $\pm 0.25^\circ\text{C}$ (3σ) from -70°C to 130°C IEEE International Solid-State Circuits Conference (ISSCC). Digest of Technical Papers. 2009:342–343.
2. Bakker A. CMOS smart temperature sensors - an overview. Proc IEEE Sensors. 2002; 2:1423–1427.

3. Chen P, Mon-Chau S, Zi-Fan Z, Chun-Yan C, Mao-Hsing C, Zhi-Yuan Z. A Fully Digital Low Cost Time Domain Smart Temperature Sensor with Extremely Tiny Size. Proc IEEE Asian Solid-State Circuits Conference(ASSCC). 2006:147–153.
4. Chen P, Chen SC, Shen YS, Peng YJ. All-Digital Time-Domain Smart Temperature Sensor With an Inter-Batch Inaccuracy of -0.7°C – $+0.6^{\circ}\text{C}$ After One-Point Calibration. IEEE Transactions on Circuits and Systems I: Regular Papers. 2011; PP(99):1–8.
5. Curty JP, Joehl N, Dehollain C, Declercq MJ. Remotely powered addressable UHF RFID integrated system. IEEE Journal of Solid-State Circuits. 2005; 40:2202(11):2193.
6. Harrison RR, Watkins PT, Kier RJ, Lovejoy RO, Black DJ, Greger B, Solzbacher F. A low-power integrated circuit for a wireless 100-electrode neural recording system. IEEE Journal of Solid-State Circuits. 2007; 42(1):123–133.
7. Woo K, Meninger S, Xanthopoulos T, Crain E, Ha D, Ham D. Dual-DLL-based CMOS all-digital temperature sensor for microprocessor thermal monitoring. IEEE International Solid-State Circuits Conference (ISSCC) - Digest of Technical Papers. 2009:68–69.
8. Li YW, Lakdawala H, Raychowdhury A, Taylor G, Soumyanath K. A 1.05V 1.6mW 0.45°C 3σ -resolution Σ -based temperature sensor with parasitic-resistance compensation in 32nm CMOS. IEEE International Solid-State Circuits Conference (ISSCC) - Digest of Technical Papers. 2009:340–341.
9. Loeb GE, Richmond FJ, Baker LL. The BION devices: injectable interfaces with peripheral nerves and muscles. Neurosurgical Focus. 2006; 20(5):E2. 15.
10. Mandal S, Sarpeshkar R. Low-Power CMOS Rectifier Design for RFID Applications. IEEE Transactions on Circuits and Systems I: Regular Papers. 2007; 54(6):1177–1188.
11. Mohseni P, Najafi K, Eliades SJ, Wang X. Wireless multichannel biopotential recording using an integrated FM telemetry circuit. IEEE Transactions on Neural Systems and Rehabilitation Engineering. 2005; 13(3):263–271. [PubMed: 16200750]
12. Nordhausen CT, Maynard EM, Normann RA. Single unit recording capabilities of a 100-microelectrode array. Brain Res. 1996; 726:129–140. [PubMed: 8836553]
13. Nikitin PV, Rao KVS. Theory and measurement of backscattering from RFID tags. IEEE Antennas and Propagation Magazine. 2006; 48(6):212–218.
14. Onik G, Gilbert J, Hoddick W, Filly R, Callen P, Rubinsky B, Farrel L. Sonographic monitoring of hepatic cryosurgery in an experimental animal model. AJR Am J Roentgenol. 1985; 144(5):1043–7. [PubMed: 3885689]
15. Onik G, Cobb C, Cohen J, Zabkar J, Porterfield B. US Characteristics of frozen prostate. Radiology. 1988; 168(3):629–631. [PubMed: 3043544]
16. Onik GM, Cohen JK, Reyes GD, Rubinsky B, Chang ZH, Baust J. Transrectal ultrasound-guided percutaneous radical cryosurgical ablation of the prostate. Cancer. 1993; 72(4):1291–1299. [PubMed: 7687922]
17. Pertijs MAP, Huijsing JH. Precision interface electronics for a CMOS smart temperature sensor. IEEE Sensors. 2005:4–.
18. Razavi, B. Design of Analog CMOS Integrated Circuits. McGraw-Hill; New York: 2001. p. 381–400.
19. Santhanam G, Linderman M, Gilja V, Afshar A, Ryu S, Meng T, Shenoy K. HermesB: a continuous neural recording system for freely behaving primates. IEEE Transactions on Biomedical Engineering. 2007; 54(11):2037–2050. [PubMed: 18018699]
20. Sapareto SA, Dewey WC. Thermal dose determination in cancer therapy. Int J Radiat Oncol Biol Phys. 1984; 10(6):787–800. [PubMed: 6547421]
21. Sasaki M, Ikeda M, Asada K. A Temperature Sensor With an Inaccuracy of $-1/+0.8^{\circ}\text{C}$ Using 90-nm 1-V CMOS for Online Thermal Monitoring of VLSI Circuits. IEEE Transactions on Semiconductor Manufacturing. 2008; 21(2):201–208.
22. Schulman JH. Human implantable wireless microstimulators and microsensors. Proc Solid-State Sensors, Actuators and Microsystems Workshop. 2008:56–59.
23. Stockman H. Communication by Means of Reflected Power. Proc IRE. 1948; 36(10):1196–1204.
24. Szekely V, Marta C, Kohari Z, Rencz M. CMOS sensors for on-line thermal monitoring of VLSI circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems. 1997; 5(3):270–276.

Figure 1.
A four-transistor schematic for CMOS temperature sensor

Figure 2.
A two-transistor schematic for a BJT temperature sensor

Figure 3.
Simple PTAT Circuit

Figure 4.
 V_{BE} , V_{BE} and V_{REF} as a function of temperature

Figure 5.
Bipolar device realization in a CMOS process

Figure 6.
Temperature sensor with digital readout

Figure 7.
Self referenced 1-bit sigma-delta modulator for digital temperature reading

Figure 8. Temperature sensor core with (1) chopping to reduce offset and flicker noise from the op-amp, and (2) dynamic element matching to reduce mismatch errors from the current sources.

Figure 9.

Chopper stabilized fully differential op-amp (a) overall circuit (b) during clock phase Φ_1 , and (c) during clock phase Φ_2

Figure 10. Frequency domain representation of chopping: (a) input signal (b) chopped input (c) added noise, and (d) chopped output prior to filtering

Figure 11.
Full model of power conducting link used in simulation with resonance capacitors and source resistance

Figure 12.
Single stage rectifier

Figure 13.
Multi-stage rectifier for higher output voltage

Figure 14.
High-level schematic of communication link using backscatter

Figure 15.
Communication link operation

Table 1

Temperature differences due to different non-idealities at (T=325K) assuming only device mismatches

Non ideality	Typical Values	Temperature ϵ (K)
V_{os}	10 mV	2.00
A_{DM}	10000 (80 dB)	0.02
$CMRR$	10000 (80 dB)	0.02
ϵ_n	5%	4.00
ϵ_{RB}	0.5%	0.04
ϵ_γ	5%	0.40