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Towards a Reduced-Wire Interface for CMUT-Based Intravascular Ultrasound Imaging Systems

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Abstract

Having intravascular ultrasound (IVUS) imaging capability on guide wires used in cardiovascular interventions may eliminate the need for separate IVUS catheters and expand the use of IVUS in a larger portion of the vasculature. High frequency capacitive micro machined ultrasonic transducer (CMUT) arrays should be integrated with interface electronics and placed on the guide wire for this purpose. Besides small size, this system-on-a-chip (SoC) front-end should connect to the back-end imaging system with a minimum number of wires to preserve the critical mechanical properties of the guide wire. We present a 40 MHz CMUT array interface SoC, which will eventually use only two wires for power delivery and transmits image data using a combination of analog-to-time conversion (ATC) and an impulse radio ultra-wideband (IR-UWB) wireless link. The proof-of-concept prototype ASIC consumes only 52.8 mW and occupies 4.07 mm² in a 0.35- μ m standard CMOS process. A rectifier and regulator power the rest of the SoC at 3.3 V from a 10 MHz power carrier that is supplied through a 2.4 m micro-coax cable with an overall efficiency of 49.1%. Echo signals from an 8-element CMUT array are amplified by a transimpedance amplifier (TIA) array and down-converted to baseband by quadrature sampling using a 40 MHz clock, derived from the power carrier. The ATC generates pulse-width-modulated (PWM) samples at 2 $\times$ 10 MS/s with 6 bit resolution, while the entire system achieved 5.1 ENOB. Preliminary images from the prototype system are presented, and alternative data transmission and possible future directions towards practical implementation are discussed.

Index Terms

Capacitive micro machined ultrasonic transducers (CMUT); impulse radio ultra-wideband (IR-UWB); intra-vascular ultrasound (IVUS); pulse width modulation (PWM); transimpedance amplifiers (TIA)

I. Introduction

Since it provides real-time and high resolution images of the arteries with negligible side effects, intravascular ultra-sound (IVUS) has been a common imaging modality for cardiovascular interventions [1]–[3]. Current solid-state IVUS catheters (3 F–8.2 F in diameter), shown in Fig. 1(a), are bulky, cannot reach to lesions in narrow arteries, and require an additional catheter exchange, prolonging the critical cardiovascular procedures. As a result, these catheters are mostly used after, but not during, the main intervention, limiting their use to only 20.3% of all cases [4].

In contrast, flexible guidewires with diameters ranging from 0.36 to 0.89 mm (1.1 F–2.67 F) are commonly used in coronary interventions along with balloon and stent catheters, as well as IVUS catheters, which are threaded over these guidewires [Fig. 1(a)] [5]. Integrating IVUS imaging directly on the guidewires would lead to a paradigm shift, i.e., IVUS can be used “during” interventions without an extra catheter exchange. Moreover, the IVUS can reach narrow arteries where most of the lesions are occurring. This potential has been recognized and envisioned for two decades and guidewire IVUS systems based on rotating single transducer have been proposed [6], [7]. These early approaches, however, were not pursued most probably because of difficulties in mechanical implementation. In the meantime, non-rotating solid-state IVUS arrays [8], and integration of ultrasonic transducer arrays and their interface electronics, such as CMUT-on-CMOS technology, have been realized [9], and in fact pressure sensors for fractional flow reserve (FFR) and Doppler flow sensors have been successfully integrated on guidewires [10]. These advances indicate the need and potential for guidewire IVUS based on phased arrays. Fig. 1(b) presents a conceptual diagram of the proposed guidewire IVUS imaging system which depicts 4 CMUT-on-CMOS phased arrays, each imaging a separate sector of the arterial wall, to form a complete cross-sectional image without rotation. In the final system, 3D-IC technology will be adopted in addition to CMUT-on-CMOS to accommodate all the necessary SoC components within the guidewire.

Several aspects of the IVUS systems need to be considered to specify the design targets on the SoC and the CMUT array. To achieve sufficient resolution similar to the conventional phased array IVUS catheters, which operate in the 20 MHz range, the smaller CMUT array on the 0.36 to 0.89 mm guidewire should operate in the 40 MHz frequency range. Because, the axial and lateral resolutions of the ultrasound image are defined by

$$\text{Axial resolution} = \frac{0.5c}{\text{Bandwidth}} \quad (1)$$

$$\text{Lateral resolution} = \frac{\text{Depth} \times \lambda}{\text{Array Size}} \quad (2)$$

where $c = 1484$ m/s is the speed of sound in tissue medium and $\lambda = 37 \mu\text{m}$ is the ultrasound wavelength [11]. Furthermore, the number and cross-sectional area used for electrical wires needs to be reduced as much as possible so that the impact on the mechanical properties, particularly flexibility, of the guidewire is minimized. Considering the average length of the guidewire, reaching ~ 2.6 m, parasitic resistance of the thin and highly flexible wires would be considerable and not only limit the analog signal bandwidth for data readout but also increase their vulnerability to noise and interference. Therefore, either digitized or pseudo-digital raw data transfer across the guidewire should be considered. Since the target guidewire IVUS operates around 40 MHz with a bandwidth of 10 MHz, digitizing raw data should be performed at least at 90 MS/s, generating data rates close to 1 Gb/s. In addition to such a high sampling rate, an even higher clock frequency is needed, leading to more power consumption and more complexity in the interface SoC. On the other hand, since the system will be placed inside arteries, where blood perfusion helps with heat dissipation to a certain extent, power consumption can be up to 100 mW [12].

Given the above design targets, we have implemented a proof-of-concept IVUS imaging SoC prototype to explore the possibility of a guidewire IVUS that significantly reduces the number of interconnects, down to only two. The system uses minimum bandwidth required by quadrature sampling, where the received echo signal from the CMUT transducer is down-converted to baseband to decrease the required sampling rate by a factor of four [13] and employs analog to time conversion (ATC) technique to convert the raw data to a pseudo-digital pulse width modulated (PWM) signal [14], which is robust against noise while requiring much lower clock rate compared to a traditional ADC solution.

To reduce the number of wires for data transmission to two, we implemented an impulse radio ultra-wideband (IR-UWB) transmitter (IR-Tx) that is combined with our PWM raw data in a new approach to reduce power consumption on the RF data Tx side [15]. To reduce the SoC power consumption and system complexity, we adopted the synthetic-aperture imaging method that uses only one pair of transmitting (U-Tx) and receiving (U-Rx) CMUT elements for each ultrasound firing event [16]. The following section described the CMUTs used in this IVUS imaging system. Section III describes the overall guidewire IVUS system architecture as well as circuit design details, including transimpedance amplifier (TIA), single-to-differential converter, quadrature sampler, clock multiplier, power-management (PMIC), PWM generator, and IR-UWB Tx. The measurement results are presented in Section IV, followed by a detailed discussion about feasibility of the proposed system and future steps, and finally the concluding remarks in Sections V and VI, respectively.

II. 1-D CMUT Array for IVUS Imaging

The elevation width of the guidewire severely limits the aperture size of the imaging array. This requires designing high frequency transducer arrays to meet the specified resolution,

according to (1) and (2). We utilized a custom-designed large signal simulation tool, described in [17], to model and design the CMUT arrays that meet the 40 MHz center frequency and 10 MHz bandwidth specifications. Since simulating the whole CMUT array is computationally intensive, only an array of 15×15 membranes was modeled in these simulations. As shown in Fig. 2(a), square shaped silicon nitride membranes, $20 \mu\text{m} \times 20 \mu\text{m}$ in size and $2 \mu\text{m}$ in thickness, were suspended over a 30 nm vacuum gap to satisfy the desired operating spectrum. A second 200 nm thick silicon nitride layer was used as the dielectric isolation layer above the gap. The CMUT array was fabricated using a low temperature CMOS-compatible micromachining process, described in [18]. To minimize the grating lobe effects in the image, we designed a 12-element 1-D array with a pitch of $25 \mu\text{m}$ ($2/3 \cdot \lambda$) which can fit in 300 μm width. Each CMUT array element is composed of 40 membranes in the azimuth direction along a length of 1 mm. We targeted 40 MHz center frequency with bandwidth of 35–45 MHz, and the resulting CMUT array had a -3 dB bandwidth of about 40 MHz around a 37 MHz center frequency, as shown in Fig. 2(b). Therefore, it was suitable for our preliminary measurements.

III. IVUS Imaging Front-End System Architecture

Block diagram of the prototype guidewire IVUS interface SoC is shown in Fig. 3(a). A complete IVUS front-end would consist of a U-Tx driver block with high voltage pulsers and transmit logic in addition to the U-Rx block [19]. The focus of this article is on the U-Rx side of the IVUS front-end because, first, designing the U-Rx block is relatively more complex than the U-Tx block. Secondly, the Tx block requires high voltage transistors (> 60 V), which were not available in our 5 V standard CMOS process. The presented front-end SoC has all the U-Tx and U-Rx functionality except for the high voltage pulsers, which are implemented off-chip using commercially available off-the-shelf (COTS) components, but can be easily integrated with the rest of the SoC in an HV-CMOS process.

A. Overall System

The guidewire IVUS system is powered by a 10 MHz power carrier signal provided by an external power amplifier (PA) and delivered through a pair of thin (58 μm diameter, AWG 42.5) wires, 2.4 m in length, running over the guidewire which are the only electrical interconnects needed to operate the proposed system. An on-chip full-wave rectifier, similar to [20], generates 3.7 V DC voltage from the power carrier, which is regulated down to 3.3 V to supply the IVUS SoC. In order to use a standard CMOS process with COTS pulsers, the CMUT array is divided into two groups, 6 U-Tx and 6 U-Rx elements, which are interlaced. Although this arrangement results in undesired grating lobes, it was adequate for our preliminary imaging demonstration purpose.

As shown in Fig. 3(a), the top electrodes of the Rx CMUT array are connected to an array of transimpedance amplifiers (TIA) to convert the CMUT output current into a voltage output. To reduce power consumption and system complexity, we utilized synthetic-aperture imaging method, in which only one U-Rx CMUT and its associated TIA are activated at any time. A control circuit that is run by a signal derived from the power carrier, selects each U-Tx-Rx pair at 25.6 μs intervals based on the anticipated round-trip pulse-echo travel time

from a target at 1 cm imaging depth [16]. To achieve better noise performance in the following stages, a single-to-differential converter was implemented to follow the TIA. Two identical direct down-conversion mixers constitute a quadrature sampler, while a local oscillator (LO) provides in-phase clock (I) and quadrature phase (Q) clock signals for each mixer. A clock multiplier was implemented to generate the I and Q clocks at 40 MHz from the 10 MHz power carrier, since the CMUT center frequency is at 40 MHz. The 40 MHz clocks are also fed into a pair of pulse width modulators (PWM) that convert the down-converted I and Q signals to sequential PWM data at 10 MS/s. Finally an AND-gate combines the two PWMs, in a way that the overall sampling rate becomes 20 MS/s. An IR-UWB transmitter then generates sharp pulses at the rising and falling edges of each PWM data pulse, according to the method described in [15], and transmits them through a 0.4–1 GHz wideband antenna to outside of the body.

B. Power Management IC

A full-wave rectifier, shown in Fig. 3(b), with a threshold-compensated diode-connected PMOS pair and a cross-coupled NMOS pair receives AC input voltage through the guidewire interconnects and generates an unregulated DC output voltage. This topology improves the power conversion efficiency (PCE) at 10 MHz and reduces the voltage drop across the rectifier while providing enough output power for the SoC. The rectifier supplies a 3.3 V regulator and a resistor-free band gap reference (BGR) that occupies less area than a regular BGR [21].

C. Transimpedance Amplifier

We used resistive feedback, shown TIAs in Fig. 3(c), for area efficiency because the area of the required resistor in this process was smaller than that of a feedback capacitor [22]. The resistive feedback TIA was designed with a transimpedance gain and bandwidth of 28.5 k Ω and 20 MHz, respectively. Although this bandwidth is smaller than the center frequency of the CMUT, these values have been optimized for the overall performance considering the power of the echo signal and the input referred noise with various TIA feedback resistor values, while limiting the power consumption to 6 mW.

Since the expected thermal mechanical noise of the targeted CMUT is larger than 2 pA/ Hz, we designed the TIA for an input-referred current noise of 1.5 pA/ Hz at 40 MHz. Moreover, the TIAs that are not in use are turned off, using enable switches (En), to save power. We also implemented another switch (Preset) that significantly reduces the input impedance of the TIA during pulse transmission to prevent possible TIA saturation due to pulse feed through from the high voltage drive signals applied to the U-Tx CMUTs.

D. Single-to-Differential Converter

The IVUS SoC front-end utilizes direct down-conversion, in which the local oscillator (LO) leakage can affect the system performance. Therefore, a double-balanced passive mixer with differential input is preferred. As shown in Fig. 3(d), a single-to-differential converter (STDC), consisting of a source follower, a source-degenerated common source, and a fully-differential amplifier, converts the single-ended TIA output to a differential signal. The source follower and CS amplifier are designed to improve positive and negative output

balancing, and both have large bandwidth (100 MHz) and low gain (-1.5 dB) to keep the phase constant at 0° and 180° in the echo signal frequency range (30–43 MHz). To reduce distortion, the overall bandwidth of the STDC is designed to be 25–90 MHz with a gain of 6 dB.

E. Clock Multiplier

Fig. 4(a) shows the dual-loop delay-locked loop (DLL) that generates in-phase (I) and quadrature (Q) 40 MHz clocks from the 10 MHz power carrier. To achieve 7 effective number of bits (ENoB), the target resolution of this prototype, from the PWM, root-mean-square (RMS) of the clock jitter should be less than $1/256$ of the maximum PWM pulse width, which is 50 ns at 20 MS/s, i.e., 99.9 ps [23]. This was the basis of the phase-frequency detector (PFD) and charge pump (CP) designs [24]. The DLL delay blocks are composed of current-starved inverter chains, for which the operating range was selected based on the region where the current variation is less sensitive to the charge pump output voltage variations. Moreover, to compensate the effect of PFD dead time, we added another delay circuit after the delay chain. The delay chain generates 16 delayed signals, in which the rising and falling edges are combined, as shown in Fig. 4(b), to generate the 40 MHz I and Q clock signals.

F. Quadrature Sampler

Since passive mixers have good noise performance and high linearity, and double-balanced mixers have low LO leakage, we adopted a double-balanced passive mixer architecture, which operation and schematic are depicted in Fig. 5. The quadrature sampler converts 35–45 MHz band, which covers the spectrum of the received echo signal, to DC–5 MHz baseband, such that the quadrature-sampler output actually shows the envelope of the echo signal. A fully-differential operational trans-conductance amplifier (OTA) converts the differential input voltages which are generated from the STDC to a pair of differential currents, and the following switches mix the current signals and the LO signals from I and Q outputs of the clock multiplier. Biquad TIAs following the mixer switches not only convert the mixed currents to differential voltage signals but also remove the high frequency image signals. Since the expected STDC output range is ± 200 mV and a valid input range for the PWM block is ± 400 mV, as explained in Section II-G, the mixer has a conversion gain of 6 dB. To achieve 7-bit resolution, the output noise of the mixer should be less than 0.5 LSB (1.56 mV), which defines the noise specification for the mixer design and performance.

G. Triple-Slope Pulse Width Modulator and Impulse-Radio Ultra-Wideband Transmitter (PWM-UWB)

Fig. 6(a) shows the triple-slope pulse-width modulator and the IR-UWB transmitter. As shown in Fig. 6(b), in the 25 ns pre-charge phase ($\Phi 1$), inputs of an OTA are connected to reference voltages, resulting in $Cap+$ and $Cap-$ to be charged with a fixed slope at the output of the OTA. In the 25 ns evaluation phase ($\Phi 2$), the OTA charges or discharges the caps at a rate that depends on the input voltage, and finally, in the 50 ns discharge phase ($\Phi 3$), the OTA discharges $Cap+$ and $Cap-$ with the opposite slope of $\Phi 1$. The onset of each PWM pulse is synchronized with the beginning of $\Phi 3$ and ends at the point where $V_{cap+} = V_{cap-}$, resulting in a pulse width directly proportional to the input voltage.

The high sampling rate (20 MS/s) requires the OTA to have a considerable current driving capability, requiring us to avoid the resulting voltage dropout across switches in our earlier design [22]. To maintain high resolution at this sampling rate, the PWM should be highly linear, which is achieved by using a source degenerated input differential pair, adopted at the input of the OTA. If the voltage difference at the input of the differential pair is large, one of the input devices is turned off and the OTA tail current (I_{ss}) flows entirely through the other device [25]. Therefore, input voltage difference at the input of the PWM block is limited to ± 400 mV to prevent such a non-linearity. The I -PWM and Q -PWM signals are combined to double the wireless link bandwidth, before being fed into the IR-UWB block in Fig. 6(a), which generates sharp pulses (0.8 ns in width) at the rising and falling edges of the combined PWM signal [15]. An all-digital PA drives the UWB antenna with the IR-UWB impulses, which alternately represent the beginning and the end of the I -PWM and Q -PWM pulses.

H. Digital Controller

The digital control block for the IVUS front-end is illustrated in Fig. 7(a). The TIAs are multiplexed since we use only one U-Rx channel at a time in this particular implementation of the synthetic-aperture imaging method. Considering that a CMUT transmits a pulse and we receive the echo signal reflected from the target, the active channel duration should be longer than the round trip duration of the acoustic wave. Since $c = 1484$ m/s, the travel time for imaging a target at 1 cm would be $13.47 \mu\text{s}$. Considering the 10 MHz reference clock of this system, we set the channel duration at $25.6 \mu\text{s}$ (CH clock), which is easy to generate by dividing the 10 MHz power-carrier signal by 256 using eight D-type flip flops. The divided clock selects the U-Rx and U-Tx channels from 1 to 8, utilizing a 3-bit counter to control the U-Rx channels followed by another 3-bit counter to control the U-Tx channels. Enable signals for U-Rx and U-Tx are connected to each TIA and pulser that control the activated CMUTs, respectively. The U-Tx control logic generates U-Tx pulses with 12.5 ns width, which are suitable for 40 MHz CMUTs, as well as a preset signal with 400 ns width at the rising edge of the CH clock.

To recognize switching between channels on the IR-Rx side, a preamble is added to the PWM data stream at the onset of every channel. Since PWM pulses are always narrower than 50 ns during normal operation, we have designed the pattern of preamble signal as a combination of two 50 ns pulses with a 50 ns interval. In addition, channel-1 is assigned a unique preamble, as shown in Fig. 7(b), to be differentiated from the other channels on the IR-Rx side.

IV. Experimental Results

A proof-of-concept guidewire IVUS SoC prototype was fabricated in the TSMC $0.35\text{-}\mu\text{m}$ 5 V standard CMOS process, occupying 4.07 mm^2 , as shown in Fig. 8. Here we present key measurement results.

A. Transimpedance Amplifier

To characterize the TIAs, we used a series RC (1 M Ω and 100 pF), shown in Fig. 9, to generate current signals from a voltage source. Since the 1 M Ω resistor is much larger than the TIA input impedance, the TIA input current is proportional to input voltage and inversely proportional to the series resistance. We added on-chip buffers following TIAs to reduce the effects of measurement tool parasitics and improve the accuracy of measurements. Fig. 9 shows frequency response of all 8 on-chip TIAs, their average, and post-layout simulation results, which indicate an average transimpedance and bandwidth of 28.5 k Ω and 20 MHz, respectively.

To measure the actual spectrum of the pressure to voltage conversion ratio of the TIA + U-Rx CMUT, an ultrasonic pressure signal was generated using a precision piezoelectric transducer (V358-SU, Olympus) in water, as shown in Fig. 10(a), and the pressure input at the CMUT position was calibrated using a broadband hydrophone (HGL-0085, Onda, Sunnyvale, CA). Measurements shown in Fig. 10(b) indicate that the CMUT + TIA has a -3 dB bandwidth of 33–42 MHz with peak pressure to voltage conversion ratio of -86.8 dBV/Pascal. Therefore, even though the TIA by itself had a narrow bandwidth (DC–20 MHz), TIA + CMUT have enough bandwidth to cover the echo signal spectrum (35–40 MHz).

We measured the output noise of the TIA + CMUT in water with a spectrum analyzer (N1996A, Agilent) using the setup described in Section IV-D. We also measured the noise spectral density at the CMUT center frequency, 40 MHz, without and with a CMUT to be 28 nV/Hz and 89 nV/Hz, respectively. Considering the transimpedance of the TIA, which is ~ 12 k Ω at 40 MHz (see Fig. 9), the input referred current noise of the TIA is about 2.3 pA/Hz, which is 53% larger than simulation results. We anticipate that with better packaging and proper integration of the CMUT + SoC, and improved shielding around the measurement setup, this difference that is attributed to the external interference to be reduced.

B. Clock Multiplier

The DLL-based clock multiplier, which generates 40 MHz square wave from the 10 MHz power carrier, was tested through an on-chip buffer. The measured clock jitter peaked at $+280$ ps/ -200 ps with an RMS value of 114 ps. This was larger than the 100 ps peak jitter design target, which is needed to achieve 7-bit resolution in the ATC block. We attribute this to non-uniformity of the inverters in the delay chain of the DLL. The 40 MHz square wave duty cycle varied from 49.2%~50.8%.

C. Analog-to-Time Conversion and Pulse Width Modulator

In order to avoid additional parasitic capacitance at the mixer output, which loads the mixer and results in additional noise in the ATC (PWM generator) block, we implemented an identical ATC block on the prototype ASIC with the exact same layout for characterization only. We measured the integral nonlinearity (INL) and differential nonlinearity (DNL) errors of the ATC block by applying a ramp input to the separate ATC block and capturing the resulting PWM pulse width, using a 1.5 GHz wideband oscilloscope at 20 GS/s. The PWM pulse width was then calculated in MATLAB, and led to measurement results in Fig. 11,

which show peak INL of $+0.48/-0.39$ LSB and peak DNL of $+0.485/-0.45$ LSB with 6-bit resolution at 20 MS/s (less than 0.5 LSB). Therefore, the equivalent data rate out of the ATC block is ~ 120 Mb/s. The effect of noise on reference voltages and limitations in the linearity of the OTA in the ATC block (see Fig. 6), and the jitter of the clock multiplier seem to be the main reasons for limiting the ATC resolution to 6 bits.

D. System Level Measurements

Fig. 12 shows the experimental setup used to verify the overall system functionality. It includes a function generator (AFG3102, Tektronix), which generates the 10 MHz power carrier and delivers it through a wideband transformer for isolation, followed by a pair of AWG 42.5 wires ($58\ \mu\text{m}$ in diameter) taken from a 7-wire 2.4 m long commercial IVUS catheter (Eagle Eye Platinum Catheter, Volcano, San Diego, CA). A 100-pin QFN package houses both the interface SoC and 12-element CMUT imaging array, where the wirebonds near the perimeter of the package are covered with epoxy to prevent them from bending and creating short-circuits. The entire package is then made water resistant by a $3\ \mu\text{m}$ layer of Parylene-C coating by placing the PCB in the Parylene coating chamber for 60 min at room temperature. A cylindrical plastic ring, 8 cm in diameter, was also glued on the PCB around the QFN package to create a small water or oil basin.

Because of the relatively large feature size of the $0.35\text{-}\mu\text{m}$ CMOS process, the SoC ability in generating narrow and sharp IR-UWB impulses in this proof-of-concept prototype was limited to lower frequency content in the 200–800 MHz range. Hence we used a large pair of log-periodic antennas (WA5VJB, Kent Electronics, Sugar Land, TX) with 20 cm separation between the SoC IR-Tx output and the external IR-Rx to cover this band. As mentioned earlier, to monitor the waveforms from each major block output while minimizing the effect of measurement tool on the system performance, we included several on-chip buffers, powered by a separate supply rail.

An $18\ \Omega$ current-sense resistor was added after the isolation transformer to measure its instantaneous output power by multiplying the current in this resistor and voltage difference across the transformer output. This value was then used to calculate the RMS power, which was measured 107.4 mW. The power and voltage at the output of the rectifier were 61.05 mW and 3.7 V, respectively. Out of these, the regulator supplied the rest of ASIC with 52.8 mW at 3.3 V, resulting in an overall power transfer efficiency of 49.1% across the IVUS catheter and PMIC block of the interface SoC. Power distribution of the system is shown in Fig. 13(a). To achieve required noise level, the mixer consumes about half of the system power consumption.

Primary system performance measurement was conducted with a single-tone test at 37 MHz, which is the center frequency of the CMUT under test. In MATLAB simulations, the peak current level from the CMUT was estimated at $3\ \mu\text{A}$, when the pulse echo signal reflects from the water-air interface at 5 mm depth, which shows a reflection coefficient of -0.005 dB. Hence, we generated a 37 MHz $3\ \mu\text{A}$ current signal using the voltage source and series RC ($1\ \text{M}\Omega$ and $100\ \text{pF}$) combination shown in Fig. 9(a). The SNR and SFDR were measured at the mixer output through its on-chip buffer. The PWM signal was probed on the IR-Tx side through a coaxial cable, while the PWM-IR-UWB signal was wirelessly transmitted

through the log-periodic antenna pair. The SNR (exclude harmonic distortion) of the signal at the mixer, PWM, and UWB outputs were 44.69 dB, 44.86 dB, and 42.84 dB SNR, respectively, without averaging, while the SFDR of the same signals were 38.73 dB, 35.32 dB, and 35.72 dB, respectively. The measured signal to noise and distortion (SINAD) ratio of the overall system was 32.45 dB that indicates 5.1-bit ENOB. Since PWM samples are taken by charging a pair of capacitors within 25 ns, the ATC block operates like a low-pass filter with 9 MHz bandwidth [26]. Therefore, the ATC reduces high frequency noise, and shows a higher SNR compared to the mixer output, as shown in Fig. 13(b). These results are significant as they show that when the interface is changed to a blood-tissue interface with -40 dB reflection coefficient [27], the system can still provide adequate SNR for imaging.

We designed an off-chip eight-channel pulser, shown in Fig. 12 using HV MOSFET drivers (MD 1213, Microchip), HV MOSFETs (TC6320, Supertex Inc.), and protection diodes (BAV99, NXP Semiconductor) to complement the U-Tx control logic on the interface SoC. The control logic generates a 12.5 ns pulse with 3.3 V amplitude, as mentioned in Section III-H, and the pulser boosts it to 60 V. One channel fires every $25.6 \mu\text{s}$ and after eight firings, the active U-Tx is switched to the next channel, as shown in Fig. 14.

E. Imaging a Four-Wire Phantom

Imaging experiments were performed using a setup as shown in Fig. 10. We used four 38-AWG metal wires ($101 \mu\text{m}$ in diameter), immersed in water and diagonally located above the CMUT array at different depths as the imaging phantom. Six elements of the array were used as U-Tx and the other 6 were used as U-Rx in a staggered 1-D array geometry, suitable for performing synthetic phased array processing to form the images. We reconstructed the images offline using both the PWM output signal through a coaxial cable [Fig. 15(a)], and the PWM-IR-UWB signal through the wireless link [Fig. 15(b)], showing the full functionality of the prototype guidewire IVUS SoC. The PWM-IR-UWB signal was transmitted across the identical log periodic antennas that were placed 20 cm apart. The received signal was recorded by a wideband oscilloscope and reconstructed in MATLAB, which also down converted the IR-UWB signal, detected the rising and falling edges of each pulse, and measured the width of each pulse with 50 ps resolution in the received PWM signal.

All images have 30 dB dynamic range and clearly show all four wires located up to a depth of 7 mm above the IVUS array. The dynamic range is lower than desired because of the non-ideal operation of the CMUT array and the mechanical and electrical noise in the experimental setup, limiting the SNR of the individual pulse-echo signals to only 15 dB. Beamforming, on the other hand, improved the dynamic range by ~ 15 dB [16]. In the images in Fig. 15, the axial spreading is more than expected due to extended ultrasonic echo signals following the main echo because of acoustic crosstalk and lateral resolution is limited by the staggered array structure. These drawbacks can be significantly reduced and the performance can be improved by applying a coating material to suppress surface acoustic waves in CMUT array design [28]. Specification of the first guidewire IVUS prototype SoC has been summarized in Table I, and compared with some of the recent ultrasound interfacing ASICs in the literature.

V. Discussion

Since the acoustic reflection at the blood-tissue interface is about -40 dB, the imaging system should have at least 50 dB of dynamic range [27]. If the readout system has 7 bit resolution, it can only provide a dynamic range of 40 dB for single-pulse echo signal. However, synthetic aperture imaging with N firings provides an additional $10\log(N)$ dB improvement in the overall SNR compared to a single-pulse and single channel [29]. Considering the width of the CMUT array ($300\text{ }\mu\text{m}$) and the width of each element, $\lambda/2 \approx 15\text{ }\mu\text{m}$ at 40 MHz, it is possible to have 120 independent firings to improve the overall SNR by about 20 dB over a single channel to achieve 60 dB dynamic range in the resulting image. Moreover, even though the 6-bit resolution of the ATC in the current prototype SoC is lower than the 7-bit design target, it is possible to improve this figure by reducing the noise on the reference nodes by more careful layout and additional capacitors or buffers. Migrating the SoC to a CMOS process with smaller feature size will reduce the setup and hold times of the flip-flop used in the DLL as a PFD, and increase the speed of the edge combiner, while reducing the clock jitter.

In this prototype, the size of the SoC does not meet the IVUS application requirements. However, after removing the signal monitoring buffers and pads, the SoC active area fits within 1.3 mm^2 . The SoC can be easily divided into three separate compartments: 1) PMIC, 2) analog front end (AFE), and 3) control logic + RF blocks. As shown in Fig. 1(b), four CMUT arrays are going to be integrated on the guidewire IVUS to cover the entire cross-section of the artery, limiting the size of each chip to about $300\text{ }\mu\text{m} \times 1\text{ mm}$. Even though each CMUT array needs its own AFE, all four AFEs can share the same PMIC, control logic, and RF blocks. Therefore, by thinning and stacking these compartments, using the 3D-IC technology [30] which employs through silicon via (TSV) for interconnects among three compartments, it is possible to shrink the interface SoC to the desired size for guidewire IVUS application.

The large and low frequency antennas used in the current prototype experimental setup can be replaced with either dipole or on-chip antennas in the next revision of the SoC, which will be implemented in a smaller feature size process with faster transistors that can generate sharper and narrower impulses within $3\text{--}5$ GHz band. Several mm-sized on-chip antennas for IR-UWB based short-range communication have already been reported in the literature [31], [32]. In the IVUS application, IR-Tx antenna will be inside of the body. Length of the dipole antenna is proportional to $1/\epsilon_r$, where ϵ_r is the relative permittivity of the transmission medium. In the tissue, $\epsilon_r \approx 50$ in $3\text{--}5$ GHz band [33]. Therefore, the optimal length of the dipole antenna will be 7 times shorter than a similar antenna in air. Since our target communication distance is quite short, from inside the heart to the surface of the chest, even a non-ideal antenna could be sufficient. The path loss across a 5 cm distance in human torso in this frequency range is about 40 dB [34]. Therefore the required IR-Tx output power in this case can be calculated from

$$P_{\text{TX}} = \text{SNR} + \text{Pathloss} + N + 10\log_{10}(\text{BW}) + \text{NF} + I \quad (3)$$

where N is the IR-Rx noise floor, BW is the channel bandwidth, NF is the noise figure, and I is the implementation loss, which has a nominal value of 1 dB [35]. A generic commercial UWB receiver [36], has NF = 7 dB and $N = -174$ dBm/Hz at room temperature. In terms of the required SNR, if we do not consider inter-symbol interference, the PWM-IR-UWB can be analyzed similar to on-off keying (OOK). If we set the maximum required bit-error-rate (BER) to 10^{-3} , which can be further improved using digital signal processing, the required energy per bit over noise power spectral density (E_b/N_0) would be 9 dB [37]. The time resolution of the ATC block with 7-bit resolution and 20 MS/s is 390 ps. Therefore, the PWM equivalent data rate with OOK modulation would be 2.5 Gb/s. Now we can use

$$\text{SNR} = 10 \log_{10} \left(\frac{E_b}{N_0} \cdot \frac{\text{DR}}{\text{BW}} \right) \quad (4)$$

where DR is the data rate [37], to calculate the required SNR for the PWM, which is 10.7 dB. In this case, the required IR-Tx output power would be -22.3 dBm. Fig. 16 shows the HFSS simulation of a dipole antenna in the tissue environment that extends from both sides of the interface SoC at the tip of the guidewire IVUS. Minimum gain of this antenna in the valid range of $20^\circ < \theta < 160^\circ$ is -18 dB. On the IR-Rx side, the external antenna can be a commercial patch or log-periodic antenna with the gain of 6 dBi [38]. Therefore, the required IR-Tx output power would be -10.05 dBm, which is well within the power budget for this block. These calculations show that a two-wire guidewire IVUS imaging system with IR-UWB wireless data link is feasible.

VI. Conclusion

We have presented a proof-of-concept prototype of a two-wire readout interface SoC for guidewire IVUS imaging system. It includes a quadrature sampler and a PWM-IR-UWB for IVUS imaging with only two long catheter wires, which deliver power to the SoC via a 10 MHz carrier signal. Despite missing some of the design targets, the prototype SoC, implemented in a standard large feature size ($0.35\text{-}\mu\text{m}$) CMOS process, demonstrated the overall functionality of the imaging system by reconstructing images of a 4-wire targets immersed in water using a 12-element CMUT array, as well as a low frequency (200–800 MHz) IR-UWB wireless communication link. A detailed discussion and analysis of size reduction and performance improvements of the proposed system indicates the feasibility of a guidewire IVUS application with wireless readout. Future work will focus on implementing these improvements on a practical thin, low wire-count, and highly flexible IVUS imaging system.

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Fig. 1.

(a) Conceptual rendering of the current piezoelectric transducer array based IVUS imaging system [1]. (b) Rendering of the proposed CMUT based guidewire IVUS, superimposed over a st Jude certus guidewire [2].

Fig. 2.

(a) Layout of the 1-D CMUT array with multiple membranes in each of the 12 CMUT elements. (b) Normalized CMUT pressure frequency response in the transmitter mode.

Fig. 3.

(a) Overall system block diagram of the IVUS imaging system. (b) Schematic of full-wave passive rectifier. (c) Transimpedance amplifier (TIA). (d) A single-to-differential converter.

Fig. 4. (a) Block diagram of a clock multiplier. (b) The operation of an edge combiner.

Fig. 5.

Operating waveforms and schematic diagram of the quadrature sampler. Two double-balanced passive mixers that share the same operational trans-conductance amplifier (OTA) are used in this quadrature sampler.

Fig. 6.

(a) Schematic diagram of a triple-slope pulse-width modulator and an impulse-radio ultra-wideband (PWM-IR-UWB). (b) An operational diagram of the PWM-IR-UWB showing the key waveforms in Fig. 6(a).

Fig. 7.

(a) Schematic of the controller block for the guidewire IVUS imaging system. (b) Waveforms of the preamble signals for the combined PWM output to mark the onset of every channel and for indicating channel-1.

Fig. 8.

Die photomicrograph of the prototype guidewire IVUS-SoC, fabricated in a 0.35- μm standard CMOS process.

Fig. 9.
(Inset) block diagram of the TIA measurement setup, and measurement results indicating the TIA frequency response.

(a)

(b)

Fig. 10.

(a) Measurement setup for testing the TIA along with CMUT. (b) CMUT + TIA measurement results.

Fig. 11. Measured (a) INL and (b) DNL of the analog-to-time converter (ATC) output.

(a)

(b)

(c)

Fig. 12.

(a) System level measurement setup for the prototype guidewire IVUS SoC. (b) Simplified diagram of setup from top and side views. (c) Top view of the SoC and CMUT assembly, wire-bonded together in QFN package.

Fig. 13.

(a) Power distribution of the system. (b) Single-tone measurement results of the mixer, ATC, and wireless PWM-IR-UWB output signals.

Fig. 14.

Measurement waveforms on the U-Tx side showing the burst of 8 pulses generated by the on-chip digital control block and amplified by the off-chip pulser to drive CMUT for two adjacent channels.

Fig. 15.

Reconstructed images from the received signal of the four wire target imaging experiment.

(a) PWM output directly probed through a coaxial cable. (b) PWM-IR-UWB signal received through the wireless link.

Fig. 16. Dipole antenna simulation model in the HFSS environment, extending from the interface SoC at the tip of the guidewire IVUS. Inset: Simulated antenna gain and its omnidirectional characteristic.

TABLE I**Guidewire IVUS Interface Electronics Benchmarking**

	[22]	[9]	This work
CMOS Technology	0.35 μm	0.35 μm	0.35 μm
Power consumption (mW)	26	0.8 *	52.8
Power-carrier frequency	-	-	10 MHz
Power-transfer efficiency	-	-	49.15%
Rectifier output voltage	-	-	3.7 V
Supply Voltage	3.3 V	3.3 V/25V	3.3 V
TIA Bandwidth	45 MHz	40 MHz	20 MHz
TIA Transimpedance	100 k Ω	200 k Ω	28.5 k Ω
Noise of TIA (nV/ Hz)	150 (@40 MHz) **	62 (@20 MHz)	28 (@40 MHz)
TIA + CMUT Bandwidth	-	-	33 ~ 42 MHz
TIA + CMUT Noise (nV/ Hz)	-	-	89 (@40 MHz)
Conversion gain of mixer	10.1 dB	-	6 dB
Mixer Bandwidth	2 MHz	-	7 MHz
RMS of clock jitter	443 ps	-	114 ps
PWM sampling rate (MS/s)	2 $\times$ 10	-	2 $\times$ 10
ATC Resolution	5 bits	-	6 bits
System ENoB			5.1 bits
IR-UWB Spectrum	-	-	0.2 – 0.8 GHz
System effective data rate	100 Mb/s	-	100 Mb/s

* Power consumption of one TIA.

** This work only provided simulation results on noise measurement.