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Abstract. We report the development of a modularized compact positron emission tomography (PET) detector that outputs serial streams of digital samples of PET event pulses via an Ethernet interface using the UDP/IP protocol to enable rapid configuration of a PET system by connecting multiple such detectors via a network switch to a computer. Presently, the detector is 76 mm × 50 mm × 55 mm in extent (excluding I/O connectors) and contains an 18 × 12 array of 4.2 × 4.2 × 20 mm³ one-to-one coupled lutetium-yttrium oxyorthosilicate/silicon photomultiplier pixels. It employs cross-wire and stripline readouts to merge the outputs of the 216 detector pixels to 24 channels. Signals at these channels are sampled using a built-in 24-ch, 4-level field programmable gate arrays-only multivoltage threshold digitizer. In the computer, software programs are implemented to analyze the digital samples to extract event information and to perform energy qualification and coincidence filtering. We have developed two such detectors. We show that all their pixels can be accurately discriminated and measure a crystal-level energy resolution of 14.4% to 19.4% and a detector-level coincidence time resolution of 1.67 ns FWHM. Preliminary imaging results suggests that a PET system based on the detectors can achieve an image resolution of ~1.6 mm. © 2016 Society of Photo-Optical Instrumentation Engineers (SPIE) [DOI: [10.1117/1.JMI.4.1.011006](https://doi.org/10.1117/1.JMI.4.1.011006)]

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1 Introduction

The advent of silicon photomultiplier (SiPM) has recently spurred a wave of innovation in positron emission tomography (PET).^{1,2} SiPM is a solid-state photodetector consisting of an array of Giger-mode avalanche photodiodes (GAPD) that are connected onto a common load via their respective quenching resistors.^{3,4} It has a photomultiplier tube (PMT)-like high gain for detecting individual light photons at room temperature. Compared to the PMT, it is much smaller (often available in 1 to 5 mm square pixels) and much more compact and rugged. Also, it operates at a low voltage (30 to 70 V), has low power consumption, can work in strong magnetic fields, and has an acceptable dark count rate. It is sufficiently fast to support time-of-flight (TOF) detection, capable of achieving a coincidence time resolution of ~100 ps FWHM.⁵ Its gain is sensitive to temperature/voltage variations, and there are issues with optical cross talk and after-pulse. However, these are not critical issues for PET applications. Researchers have exploited and are exploiting the favorable physical and performance characteristics of SiPM for developing PET detectors that are high resolution and/or capable of TOF or depth-of-interaction (DOI) measurement,^{6–12} that are compatible with magnetic resonance imaging (MRI),^{13–15} and that can lead to novel probes for endoscopic, endorectal, and intraoperative imaging.^{16–18}

For SiPM-based PET systems, readout/data-acquisition (DAQ) is a significant issue as a system can employ a vast number of SiPM pixels. To address the issue, multiplexing readouts that

can substantially reduce channel number^{19–23} and application-specific integrated circuits that can provide many readout channels on a small chip^{24–28} have been reported and remain active topics of research. Generally, devising an efficient readout/DAQ that can support high spatial resolution and time resolution is still a major challenge. In digital SiPM (dSiPM), per-pixel readout is achieved by embedding dedicated diode electronics in the SiPM pixel to sense individual GAPD voltage to obtain and output the pulse height and event time in digital form.^{29–31} In comparison with its analog cousin, dSiPM has superior time and energy resolution, and is less susceptible to temperature variation and electronic noise. A drawback of dSiPM is the diminished photon detection efficiency since the embedded electronics decrease the detection-sensitive area. Presently, analog SiPM is more readily available and is considerably less expensive than dSiPM.

Previously to address the readout challenge, we proposed the use of striplines (SL) for multiplexing readout^{23,32,33} and developed a sampling-based DAQ called the multivoltage threshold (MVT) method.^{34–37} SL readout is easy to implement and can maintain fast-time characteristics to support TOF detection. It is also scalable and allows the DAQ electronics to be placed significantly away from the scintillator/photodetector. As a result, it is very attractive for developing compact, TOF PET insert for simultaneous PET/MRI. The MVT DAQ digitally samples a signal with respect to a few voltage thresholds, and we have shown that signals generated by an SiPM coupled to lutetium-yttrium oxyorthosilicate (LYSO) can be adequately recovered from their

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digital samples acquired using a 4-level MVT DAQ. This DAQ can be cost-efficiently implemented using field programmable gate arrays (FPGA) to achieve a high channel density.³⁵

In this paper, we describe the use of a cross-wire/SL readout and the MVT DAQ to implement a modularized compact PET detector that has built-in electronics to output serial streams of digital samples of PET event pulses via Ethernet interface/protocol (or other industry-standard high-speed serial communication interfaces/protocols). Consequently, a PET system can be rapidly configured by connecting multiple such detectors via a network switch to a computer and employing postacquisition software-based event processing, energy qualification, and coincidence filtering. The remainder of this paper is organized as follows. In Sec. 2, we describe the designs and implementations of the detector and an electronics board for generating the synchronization clock. In Sec. 3, we report measured performance properties for the detector and a simple test system that employs two such detectors. Conclusions and discussion are given in Sec. 4.

2 Design and Implementation

Figure 1(a) shows the modularized detector that is comprised of an LYSO/SiPM unit, an SL readout unit, and a sampling/interface unit. It has three I/O connectors for power, a high-quality synchronization (sync) clock, and an RJ45 port for bidirectional serial communication following the UDP/IP protocol. Excluding the I/O connectors, the detector has a compact size of $\sim 50 \text{ mm} \times 76 \text{ mm} \times 55 \text{ mm}$. It contains 18×12 LYSO/SiPM pixels that have a pitch of 4.2 mm. The detector is function-complete: without needing additional electronics, it can output digital streams containing samples of PET event pulses up to one gigabits per second. These digital samples are to be numerically analyzed on a computer to identify the signal-generating detector pixel and to derive the event energy and time. Energy qualification and coincidence filtering are also performed on the computer.

In Secs. 2.1–2.3, we will separately describe the three main components of the detector. The design of a board for generating

a clock for synchronizing multiple detectors is described in Sec. 2.4.

2.1 LYSO/SiPM Unit

The LYSO/SiPM unit is made of three subunits, as shown in Fig. 1(b). Each subunit contains a 6×12 LYSO matrix, a 6×12 SiPM matrix, and a printed circuit board (PCB) that provides bias voltage to, and cross-wire readout of, the SiPMs. The LYSO matrix (from the Sanho Ostor Electronics Corp.) contains $3.9 \text{ mm} \times 3.9 \text{ mm} \times 20 \text{ mm}$ pixellated crystals with 0.3-mm crystal gaps that are filled with barium sulfate to reflect lights. The SiPM matrix is based on two SensL's FM30035 arrays, each of which contains 6×6 pixels and each pixel has an active detection area of $3.0 \text{ mm} \times 3.0 \text{ mm}$. The SiPM and LYSO matrices, both having a $4.2 \text{ mm} \times 4.2 \text{ mm}$ pitch, are carefully aligned and coupled using epoxy optical adhesive. The PCB implements the cross-wire method³⁸ for reading the SiPM outputs in row- and column-sums. Specifically, for each SensL FM30035 array, we connect the cathodes of the 6 SiPM pixels on a column/row together to obtain 6 column/row-sum signals (see Fig. 2). The overall detection area of the subunit is $\sim 25 \text{ mm} \times 50 \text{ mm}$.

The gap between the subunits is 0.5 mm. Thus, as a whole, the unit has an area of $\sim 50 \text{ mm} \times 76 \text{ mm}$, 18×12 one-to-one (1:1) coupled LYSO/SiPM pixels having a 4.2-mm pitch (except for two wider gaps between subunits), and a total of 72 outputs.

2.2 Striplines Readout Unit

Figure 2(a) shows the electronics board that implements the SL readout to further reduce the number of outputs of the LYSO/SiPM unit. The SL method is based on the idea that the injection of a signal at a certain point on the SL will create a pair of identical pulses traveling in opposite directions.³² Therefore, based on the arrival time of these pulses at the ends of the SL, the location and time of signal injection can be derived from their difference (called the SL differential time) and average (called

Fig. 1 (a) A modularized compact detector that outputs digital streams containing samples of PET event pulses. It consists of an LYSO/SiPM unit, an SL readout unit, and a sampling/interface unit that has three I/O connectors, including a power connector, a sync-clock input, and an RJ45 Ethernet port. It has an area of $\sim 50 \text{ mm} \times 76 \text{ mm}$. Excluding the I/O connectors, its thickness is about 55 mm. (b) A 6×12 SiPM matrix, a 6×12 LYSO matrix, and the assembled subunit consisting of 6×12 LYSO/SiPM pixels (from left to right). The SiPM matrix has a $4.2 \text{ mm} \times 4.2 \text{ mm}$ pitch, and each pixel has a $3.0 \text{ mm} \times 3.0 \text{ mm}$ active area. The LYSO matrix consists of $3.9 \text{ mm} \times 3.9 \text{ mm} \times 20 \text{ mm}$ crystals, with 0.3 mm crystal gaps filled with barium sulfate to reflect lights. The PCB provides the bias voltage to the SiPMs and implements a cross-wire method for reading the SiPM outputs in row- and column-sums. The SiPMs are directly assembled on the PCB. The LYSO/SiPM unit is made of three such subunits.

Fig. 2 (a) The SL readout board. (b) A schematic showing the reduction of the six row-sums and six column-sums of the cross-wire readout from an FM30035 array to four outputs (A to D) using two SLs. (c) The SL differential time between adjacent columns can be significantly increased using a convoluted SL path. The same is implemented for the other SL to increase the separation between adjacent rows.

the SL mean time), respectively. As illustrated in Fig. 2(b), we connect the six column-sums and six row-sums generated by the cross-wire readout for an FM30035 array to two SLs. Therefore, the 36 SiPM outputs of an FM30035 array are read using four DAQ channels at the ends of the two SLs, achieving a 9:1 multiplexing ratio. Since the 4.2-mm pixel pitch corresponds to an SL differential time of about 50 ps, to resolve adjacent rows/columns we would need a time resolution of ~ 25 ps. This level of time resolution is challenging to achieve. In addition, it is unnecessary with respect to the 200- to 700-ps TOF resolution presently achieved in the field. To relax the timing requirement, as illustrated in Fig. 2(c), we introduce the use of convoluted SLs to sufficiently increase the separation in the SL differential time between adjacent rows and columns.

Therefore, electronically the detector is comprised of 3×2 divisions, each of which contains 6×6 LYSO/SiPM pixels and, by use of cross-wire and SL readouts, produces four outputs, yielding a total of 24 outputs for the detector.

2.3 Sampling/Interface Unit

The sampling/interface unit provides 24 FPGA-only MVT sampling channels to match the number of outputs of the SL readout unit. The principle and implementation of this sampling DAQ was previously reported by Kim et al.³⁴ and Xi et al.³⁵ For the readers' convenience, they are briefly reviewed in this section, and readers are referred to Refs. 34 and 35 for details.

As depicted in Fig. 3(a), unlike the popular analog-to-digital converters (ADCs) that sample a signal at a regular time interval, the MVT method samples a signal with respect to a number of reference voltages. It has been demonstrated that, as the event pulse generated by a PET detector has a simple and known shape, the event time and energy can be accurately estimated from samples produced using four reference voltages. Figure 3(b) shows that this sampling method can be implemented using an FPGA. As shown, the input signal is split and connected to four voltage comparators implemented using the low-voltage differential signaling input pins of the FPGA. The reference voltages are programmably set using digital-to-analog converters (DAC). The time of the rising/falling transition of the comparator output is determined using FPGA-based

time-to-digital converters (TDC). These time values are paired with the known preset reference voltages to produce digital samples of the input signal. The FPGA implementation reduces the cost and power consumption of the sampling DAQ; modifications and upgrades can also be readily made.

Figure 4 shows that the TDC is comprised of a carry chain, a register, and a counter. The carry chain is implemented using a n -bit full-adder of which, from the least-significant bit (LSB) to the most-significant bit (MSB), the "carry-out" of each bit is connected to the "carry-in" of the next bit. For all bits, "addend" is set to logic "1." On the other hand, "augend" is set to logic "0," except the LSB, for which it is connected to "input." At each "clock," the "sum" values are latched onto the register and the counter increments by 1. Initially, input is "0," and hence sum and carry-out of the LSB will equal to "1" and "0," respectively. After a delay, carry-out of the LSB will appear on carry-in of the next bit, making its sum and carry-out to take values of "1" and "0," respectively, also. This action will propagate down the chain to the MSB. Therefore, if "input" stays at "0" for a sufficiently long duration, all sum and carry-out will be "1" and "0," respectively. Now, assume that input changes from "0" to "1" (a positive transition). Following the above discussion, we see that sum (carry out) will be inverted from "1" to "0" (from "0" to "1") in sequence, starting from the LSB toward the MSB. Likewise, when input later returns from "1" to "0" (a negative transition), sum (carry out) will be inverted back from "0" to "1" (from "1" to "0") in sequence. It is then not difficult to see that the number of leading zeros of the bits pattern in the register (starting from the LSB) is the number of propagation delays taking place between a positive transition of input and the clock after the transition when the sum values are latched. Therefore, it measures the elapsed time between a positive transition of input and the subsequent clock, called the "fine time" T_1 . On the other hand, the counter measures the time of the clock called the "coarse time" T_2 . Thus, the positive transition occurs at $T_2 - T_1$. In our present implementation, $n = 128$ and the clock is 200 MHz. The counter (the digital coarse time) has 40 bits, capable of counting up to about 91.7 min at 5-ns increment. The digital fine time, which stores the number of leading zeros, has 8 bits (which is sufficient because there are at most 128 leading zeros). The TDC, therefore, has a 48-bit output. Evidently, the precision of T_1 is

Fig. 3 (a) The MVT method samples a pulse (blue solid curve, acquired from an LYSO/SiPM) with respect to N reference voltages (4 shown) to produce at most $2N$ samples (red dots). The samples can be fitted to a mathematical description of the pulse (red dashed curve) to yield information about the start time, amplitude (or area), and time constant of the tail. We have previously shown that the use of four reference voltages is sufficient for pulses generated by LYSO/SiPM. (b) A schematic for a 4-level FPGA-only MVT sampler in which the voltage comparators and TDCs are implemented in the FPGA. The reference voltages are programmably set using DAC. A modern inexpensive FPGA has the capacity for implementing a large number of MVT channels.

Fig. 4 Implementation of the FPGA-based TDC.

determined by the propagation delays of the carry chain. Figure 5 shows the measured propagation delay (bin width) for the first 64 bins (bits), showing an average width of 81.5 ps and a standard deviation of 11.7 ps. According to Szplet et al.,³⁹ this corresponds to a time resolution of ~ 83.1 ps for the implemented TDC. We note that with the average fine-time bin width of ~ 81 ps, the 5-ns coarse-time interval corresponds to only ~ 62 delays. Therefore, we could have implemented the TDC using $n = 64$, but for future extension we choose to use $n = 128$.

Figure 6 shows the sampling/interface unit that provides twenty-four 4-level FPGA-only MVT channels by employing a single Altera EP4C115F29C7 FPGA. The reference voltages are provided using Texas Instrument (TI) DAC7678. All the MVT channels are synchronized to a built-in clock on the board or the external sync clock when it is provided. The FPGA also implements logics to pack the resulting MVT samples and output them via a gigabit Ethernet communicator. The physical layer interface of the Ethernet interface is implemented using Marvell 88E111 (Marvell Technology Group Ltd.). The size of the board is 76 mm $\times$ 50 mm, matching that of the LYSO/SiPM unit.

Fig. 5 The differential nonlinearity of an FPGA-based TDC of the detector.

Fig. 6 The sampling/interface unit. The board size is 76 mm × 50 mm. It provides twenty-four 4-level FPGA-only MVT channels by employing one Altera EP4C115F29C7 FPGA. These channels are synchronized to a built-in clock or an external sync clock. The reference voltages are set using twelve 12-bit, 8-ch DACs (Texas Instrument DAC7678). The board also implements I/O interfaces for the detector modules, including an Ethernet port.

Fig. 7 An FPGA-based 50-MHz sync-clock generator supporting up to 12 detectors.

2.4 Sync-Clock Board

Figure 7 shows the design of the sync-clock board. A 50-MHz clock is generated using a phase-locked loop inside an Altera EP4CE10E22C8N FPGA from a 25-MHz oscillator. The 50-MHz clock is connected to an Analog Device ADCLK954, which is an ultrafast clock fanout buffer that provides 12 full-swing emitter coupled logic (ECL) outputs, to produce 50-MHz synchronization clocks for up to 12 detectors. In addition, the FPGA also generates 12 synchronized signals for

resetting the detectors to start a new DAQ session; the detectors are reset at the falling edges of these signals.

3 Performance Characterization

3.1 Experiment Setup: A Stationary Test System

We have developed two detectors as described above and constructed a small test system, as shown in Fig. 8, by connecting them to a computer via a network switch and a sync-clock board. The detectors are placed opposite each other at a distance of 50 mm and remain stationary during the experiment. The computer can directly communicate with and receive outputs from both detectors via the network switch. The MVT samples generated by the detectors are stored on the computer where they are processed postacquisition to derive event information. Energy qualification and coincidence filtering are also done on the computer by software. Subject to the count-rate capability, this system can be easily expanded by connecting more modularized detectors to the network switch and sync-clock board.

The pixel positioning accuracy and energy resolution of the modularized detectors and the coincidence resolving time (CRT) of the test system are measured using a point-like FDG source of $\sim 35 \mu\text{Ci}$. A custom-made resolution phantom filled with $\sim 36 \mu\text{Ci}$ FDG placed at the center of the test system is also imaged to provide an initial estimate of the image resolution. Image reconstruction is achieved using a maximum-likelihood expectation-maximization (MLEM) algorithm⁴⁰ that incorporates a solid-angle-based geometric system response matrix. Presently, no corrections for nonuniform detection efficiency, attenuation, scatter, and randoms are performed.

3.2 Processing of the Multivoltage Threshold Samples

The voltage and time values of the MVT samples are first calibrated using channel-based calibration factors as previously described by Xi et al.³⁵ Refer to Fig. 2(b) and consider signals at terminals *A* and *B* of the SL that receive the column-sums of an FM30035 array. As Fig. 9 illustrates, the two pulses arrived at *A* and *B* are almost identical in shape and amplitude. Based on this observation, we calculate the SL differential time using the mean of the time differences obtained at the specified reference voltages. That is, we have

Fig. 8 (a) A stationary test system employing two developed detectors, with a custom-made resolution phantom placed in-between. The detectors are separated by 50 mm. (b) A schematic drawing of the test system. It consists of a computer, a network switch, a sync-clock board, and two detectors. The system can be readily expanded by connecting more detectors to the network switch and sync-clock board.

Fig. 9 The SL differential time is computed as the mean of the time differences between the four MVT samples taken at the rising edge of two pulses arriving at the two ends of the SL.

$$\Delta T_{AB} = \frac{1}{4} \sum_{i=1}^4 (t_{iA} - t_{iB}), \quad (1)$$

where t_{iA} and t_{iB} are the time values when the rising edges of the pulses reach the i 'th reference voltage. Since the SiPMs and LYSO crystals are 1:1 coupled, only one of the six column-sums will have signal. The time difference ΔT_{AB} , therefore, encodes the column position of the signal-generating LYSO/SiPM pixel. Likewise, ΔT_{CD} , similarly calculated as ΔT_{AB} for the SL receiving row-sums, encodes the row position of the signal-generating LYSO/SiPM pixel. Consequently, the two-dimensional (2-D) histogram of ΔT_{AB} and ΔT_{CD} obtained for one FM30035 array shall display 6×6 clusters, each of which corresponds to one LYSO/SiPM pixel.

The event energy and time are derived from the MVT samples obtained at one end of the SL, say A, using the method previously reported in Xi et al.³⁵ That is, we fit the samples to the following expression to estimate a , t_0 , b , and d , where a and t_0 are the event amplitude and time and b and d are related to the pulse decay time and rise time.

$$y(t) = a \times \exp\left(-\frac{t-t_0}{b}\right) \times \left[1 - \exp\left(-\frac{t-t_0}{d}\right)\right]. \quad (2)$$

After the position, energy, and time are obtained for each event, a user-defined energy window and coincidence time window are applied for energy qualification and coincidence filtering to generate coincidence list-mode data.

3.3 Position Accuracy, Energy Resolution, and Time Resolution

Figure 10(a) shows the six $\Delta T_{AB} - \Delta T_{CD}$ 2-D histograms obtained for one detector, arranged in a 3×2 array according to the physical positions of the corresponding 6×6 LYSO/SiPM blocks in the detector. The straight lines superimposed on the histograms are manually drawn for creating the lookup table for pixel identification. As shown, 18×12 clusters, each associated with one LYSO/SiPM pixel, are well discriminated. Figure 10(b) shows an intensity profile of the 2-D histogram at the position that is marked by the yellow box in Fig. 10(a). There are small cross talks between peaks and the peak-to-valley ratios are superior, ranging from 6.2 to 13.7. By applying the manually defined lookup table, each event can be accurately assigned to the signal-generating pixel.

Figure 11(a) shows the pulse-height spectra (PHS) obtained for each pixel of one 6×6 LYSO/SiPM block. The photopeaks of these spectra are clearly observed, and they are fitted by a Gaussian function to estimate their energy resolutions, obtaining a value ranging from 14.4% to 19.4%. Figure 11(b) shows the PHS derived from all events measured by the block, showing an overall energy resolution of 16.8%.

Figure 12(a) shows the coincidence time histogram obtained using all detected coincidence events by all channels for the point-like source after applying a 450- to 650-keV energy window. By fitting the histogram with a Gaussian function, we obtain a 1.67-ns FWHM CRT for the test system.

3.4 Phantom Imaging

Figure 12(b) shows a photo of the custom-made resolution phantom and the preliminary image obtained for the phantom. The phantom contains six groups of hollow rods of various diameters and is placed approximately half-way between the two detectors with the rods normal to the face of the detectors [see Fig. 8(a)]. The rod diameters in the six groups are 0.7, 1.0, 1.2, 1.6, 2.0, and 2.4 mm. In the same group, the distance between rods is twice the rod diameter. Since the phantom and detectors remain stationary during imaging, the acquired data

Fig. 10 (a) The $3 \times 2 \Delta T_{AB} - \Delta T_{CD}$ 2-D histograms for one of the developed detectors. The straight lines are manually drawn to segment the histograms to create lookup tables for crystal identification. (b) An intensity profile of the 2-D histogram at the position shown in the yellow box in (a).

Fig. 11 (a) PHS obtained for the 6×6 pixels of an LYSO/SiPM block (blue curves). By fitting the photo-peaks with a Gaussian function (red curves), we obtain an energy resolution ranging from 14.4% to 19.4%. (b) The pulse-height spectrum for all events of the block and its Gaussian fit, yielding an energy resolution of 16.8%.

Fig. 12 (a) The coincidence time spectrum after applying a 450- to 650-keV energy window (blue curve). By fitting with a Gaussian function (red curve), we obtain an overall CRT of 1.67 ns FWHM for the test system. (b) A photo of the custom-made resolution phantom consisting of six groups of hollow rods having diameters of 2.4, 2.0, 1.6, 1.2, 1.0, and 0.7 mm (left) and the resulting image, reconstructed using an MLEM algorithm (right). The red circle identifies the 1.6-mm-diameter rods. In the image, rods having diameters larger than 1.6 mm are resolved.

are incomplete for reconstruction (the detector spacing is 50 mm). A coincidence time window of 4 ns and an energy window of 450 to 650 keV are used, and 0.5-mm cubic voxels are used in the MLEM algorithm. Although no corrections for nonuniform detection efficiency, attenuation, scatter, and randoms are applied and the data are incomplete, in this preliminary image, rods having diameters larger than 1.6 mm can be resolved.

4 Conclusions and Discussion

We report a modularized compact PET detector based on 1:1 coupled LYSO/SiPM pixels, cross-wire and SL readouts, and an FPGA-only MVT digitizer. The detector outputs serial streams of digital samples of PET event pulses via an Ethernet port. As a result, a PET system can be readily configured by connecting multiple such detectors to a computer via a network switch. The performance properties of the developed

detectors are measured. We observe that all pixels of the detector are well discriminated; the energy resolution for individual LYSO/SiPM pixel ranges from 14.4% to 19.4%, with an overall energy resolution of $\sim 16.8\%$; CRT estimated from all events collected by two detectors for a point-like source is 1.67 ns. We also perform a preliminary imaging study by placing a custom-made resolution phantom between two opposing detectors. Despite that the acquired data are incomplete and there are no corrections for nonuniform detector efficiency, attenuation, scatter, and randoms, the resulting image can resolve rods having diameters larger than 1.6 mm. The design of the proposed detector can be extended for developing larger flat- or curved-panel PET detectors to enable rapid development of application- or organ-specific PET imagers.

For the developed test system, pulse fitting of the MVT samples, processing of the singles (including calibrations of the event energy and time, identification of the event position,

and application of the energy window), coincidence filtering, and image reconstruction are all performed on a PC postacquisition. In the preliminary imaging study, we acquired 81-million single events and it took ~ 2 h to generate the reconstruction image from the MVT samples. As the focus of this work is detector development, we have not optimized the software programs. We believe that after exploiting the computation power of multicore CPUs and GPUs that are common in present-day PCs, we will be able to substantially reduce the overall computation time, possibly down to ~ 30 min for this particularly dataset. Nonetheless, superior computation power is needed for systems based on the proposed detectors.

While we have previously shown that both the SL readout and MVT DAQ can support TOF detection, as it is currently implemented, the detector has a non-TOF CRT of about 1.67 ns. We stipulate four reasons for this result. First, the current implementation applies a single bias voltage to all SiPMs in the detector. Due to nonuniform properties of the SiPMs, this voltage is not optimal for all, and some channels can have deteriorated timing characteristics. Second, we use the cathode output instead of the fast output of the SensL FM30035. It is known that this can result in 1 to 2 ns deterioration in timing when using the FM30035 array.^{41,42} Third, the use of cross-wire readout to produce row- and column-sums considerably lengthens the pulse rise time and therefore deteriorates the timing. This is possibly due to the increased capacitance when more SiPMs are connected. Finally, different channels generally have different time shifts. This variation in the time shift, which is not calibrated in the present work, can degrade the CRT estimated from events measured by all channels. In future work, we will carefully investigate these factors, introduce modifications, and perform the necessary calibration to improve the CRT.

The count-rate performance of the detector is not examined in this work. Since the MVT DAQ board simply takes pulse samples and pushes them through the Ethernet interface, the main rate-limiting factor of the board is the speed of the Ethernet interface, as supported by our initial test results. With the 1G interface and given the 768-bit event word (Each threshold produces two 48-bit time samples and they are packed into a 192-bit record. Four thresholds are used, and hence one event has 768 bits.), the estimated count-rate limit due to the Ethernet interface is ~ 1.3 million counts per second (Mcps). This limit can be increased using the 10G Ethernet interface. On the other hand, the event pulse entering the board can be a pile-up. On the oscilloscope, the event pulse generated by the LYSO/SiPM unit is observed to be shorter than 300 ns [see Fig. 3(a) for an example]. Using the paralyzable dead-time model⁴³ with a 300-ns dead time, we have $<10\%$ dead-time loss at event rates below ~ 152 thousand counts per second (kcps). With the current implementation, each SL sees signals from one 6×6 LYSO/SiPM array, and thus each such array can support ~ 152 kcps with negligible event loss due to pile-up. The detector has six such arrays operating independently. Consequently, this consideration yields a count-rate capability of ~ 900 kcps for the detector. This is a stronger rate limit on the detector than that imposed by the Ethernet speed. To estimate the singles rate in clinical imaging, we consider a 10-mCi point source at 45 cm away from the detector (assuming a 90-cm ring diameter). Based on the attenuation of 20-mm-thick LYSO for 511-keV photons and the solid angle of the detector to the point source, the singles rate at the detector is calculated to be ~ 0.9 Mcps also. The above analysis suggests that the developed detector is suitable

for building clinical PET systems. However, in future work, we need to measure and systematically study the count-rate properties of the developed detector.

Disclosures

We have no conflicts of interest to disclose.

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