Flexible bottom-gate graphene transistors on Parylene C substrate and the effect of current annealing

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Flexible graphene transistors built on a biocompatible Parylene C substrate would enable active circuitry to be integrated into flexible implantable biomedical devices. An annealing method to improve the performance of a flexible transistor without damaging the flexible substrate is also desirable. Here, we present a fabrication method of a flexible graphene transistor with a bottom-gate coplanar structure on a Parylene C substrate. Also, a current annealing method and its effect on the device performance have been studied. The localized heat generated by the current annealing method improves the drain current, which is attributed to the decreased contact resistance between graphene and S/D electrodes. A maximum current annealing power in the Parylene C-based graphene transistor has been extracted to provide a guideline for an appropriate current annealing. The fabricated flexible graphene transistor shows a field-effect mobility, maximum transconductance, and a I_{on}/I_{off} ratio of $533.5 \text{ cm}^2/\text{Vs}$, $58.1 \mu\text{S}$, and 1.76, respectively. The low temperature process and the current annealing method presented here would be useful to fabricate two-dimensional materials-based flexible electronics. *Published by AIP Publishing.*

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Flexible devices and systems are getting more attractive for various applications such as flexible displays,^{1–3} wearable electronics,^{4–6} and biomedical devices.^{7–9} Among various flexible materials, Parylene C has been used as a substrate or a coating material in implantable biomedical devices due to its biostable and biocompatible characteristics.^{10–12} Recently, a graphene neural electrode array fabricated on a Parylene C substrate has been demonstrated as an implantable biomedical device showing its mechanical flexibility and long-term biocompatibility.⁷ Although Parylene C is a promising flexible material, its vulnerability to high temperature (continuous service temperature: 80°C) hinders its utility as a substrate for conventional silicon- or heteromaterial-based transistors and circuits. Especially, high temperature processes such as thermal annealing, dopant diffusion, and thermal oxidation on the Parylene C substrate are almost impossible. Graphene or organic materials could be suitable candidates as an alternative active material of a transistor on Parylene C substrates due to their low-temperature process. Graphene can be transferred to the Parylene C substrate at room temperature, which does not require dopant diffusion. In spite of the advantages, studies on the fully flexible graphene transistors on Parylene C are lacking. Many of the previous studies have been limited to Parylene C evaporated on rigid Si/SiO₂ substrate or Parylene C as a gate dielectric material.^{13–15} The individually patterned graphene transistors on fully flexible and biocompatible Parylene C substrate would be desirable for implantable graphene-based electronics. The flexible graphene transistors on Parylene C could be combined with other

graphene-based electronics such as a graphene electrode array.⁷ Also, the flexible graphene transistors can be utilized as flexible biosensors since graphene transistors have shown their ability to detect chemicals, molecules, and cells.^{16–19}

In this paper, we present flexible graphene transistors on Parylene C substrate fabricated with low temperature processes. The graphene transistors have a bottom-gate coplanar structure in which graphene can be transferred onto the pre-formed gate (G), gate dielectric, source (S), and drain (D). This structure and the fabrication process are compatible with the flexible graphene neural electrode arrays as the graphene is located in the very last layer and exposed in air.^{7,20} In order to improve the performance of the flexible graphene transistors, a current anneal method has been introduced post fabrication. The current annealing resulted in the increased drain current (I_d), which was attributed to the decreased contact resistance between graphene and S/D electrodes. An empirical estimation of maximum allowing power of the current annealing has been provided. The low-temperature fabrication process and the current annealing method provided here would be valuable not only to the flexible graphene electronics but also to other possible electronic systems on Parylene C substrate.

Figure 1 shows the illustration of the fabrication process (Fig. 1(a)) and microscope images (Figs. 1(b)–1(d)) of the flexible graphene transistors. A $15 \mu\text{m}$ -thick Parylene C film was deposited on a silicon substrate with a size of $2 \times 2 \text{ cm}^2$ using a chemical vapor deposition (CVD) system (SCS Labcoater2). The silicon substrate was used as a handling substrate during the fabrication process. The size of the substrate can vary depending on the applications. A bottom-gate metal was formed by a lift-off process using photolithography and

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FIG. 1. Fabrication method and fabricated flexible graphene transistors on Parylene C substrate. (a) Schematic illustration of the fabrication process. (b) Fabricated flexible graphene transistors on Parylene C substrate. (c) Flexible graphene transistors after bending. (d) Microscope image of the flexible graphene transistors. The channel length and width are $3\ \mu\text{m}$ and $10\ \mu\text{m}$, respectively. (Inset) Microscope image of the entire device including gate, source, and drain pads.

e-beam metal evaporation. Oxygen plasma treatment (O_2 50 sccm, 10 mTorr, 10 mW, 30 s) was performed in-between the negative photoresist (PR) 5214 patterning and the e-beam metal evaporation in order to change the wetting property of the Parylene C film from hydrophobic to hydrophilic. The hydrophilic surface can lead stronger metal bonding to Parylene C.^{7,21} Titanium (Ti, 10 nm) and gold (Au, 60 nm) were used for the gate metal. A silicon dioxide (SiO_2) gate dielectric with a thickness of 100 nm was evaporated using an e-beam evaporator, which is a low-temperature process. In order to open the gate metal pad, the SiO_2 gate dielectric was etched using photolithography and dry etching process (inset of Fig. 1(d)). Source and drain electrodes (Ti 10 nm/Au 60 nm) were patterned on the SiO_2 gate dielectric using the same patterning method as the gate metal patterning. In this process, the O_2 plasma treatment was not performed because the S/D metal was deposited on the SiO_2 gate dielectric, which was hydrophilic already. Mono-layer graphene synthesized by chemical vapor deposition (CVD) method was transferred onto the pre-patterned S/D metal using a wet transfer method. In specific, the CVD graphene grown on copper (Cu) foil was spin coated with Poly(methyl methacrylate) (PMMA) to protect the exposed graphene on Cu foil. After etching the Cu foil with 0.25 M ferric chloride (FeCl_3) and rinsing with deionized (DI) water, the graphene/PMMA film floating on DI water was transferred to the pre-patterned sample. The PMMA was removed by acetone after thoroughly drying out the water in nitrogen atmosphere. Only mono-layer graphene remained on the S/D metal and SiO_2 gate dielectric after this process. The detailed graphene transfer process and Raman spectroscopy of our CVD graphene can be found in our previous papers.^{7,20} Prior to patterning the transferred graphene, a SiO_2 protection layer with a thickness of 30 nm was deposited using an e-beam evaporator. This SiO_2 layer protected the graphene during the patterning and other post processes. The graphene/ SiO_2 layer was patterned using photolithography

and dry etching, and the patterned graphene worked as a transistor channel. Finally, the graphene transistors on Parylene C was released from the silicon substrate after cutting the Parylene C on the edge of substrate. The Parylene C cutting or patterning can be performed using a cutter or O_2 dry etching. Information on the Parylene C patterning using PR 4620 photolithography and O_2 dry etching can be found in our previous paper.⁷ Parylene C can be released from the silicon substrate in water. The hydrophobic property of the Parylene C makes the entire device be repelled from the water molecules penetrated in-between Parylene C and silicon.

Figures 1(b) and 1(c) show the fabricated flexible graphene transistors on Parylene C substrate. Figure 1(d) shows a microscope image of the graphene transistors with two finger gate structure. Patterned graphene is shown on the S/D electrodes and the bottom gate. The channel width (W) and length (L) are $10\ \mu\text{m}$ and $3\ \mu\text{m}$, respectively.

The effect of thermal annealing in graphene transistors has been reported in which the applied heat decreases the contact resistance between graphene and S/D electrodes and reduces the surface contamination of graphene, and thus increases the drain current.^{20,22} On Parylene C substrate, however, the thermal annealing around $100\text{--}250^\circ\text{C}$ could deform or melt the substrate due to the low glass transition temperature of Parylene C ranging from 35°C to less than 100°C .^{23–25} As an alternative annealing method, we introduced a current annealing method to apply heat directly to the interface of S/D electrodes and graphene, diminishing the heat applied to the Parylene C substrate. During the current annealing, the electric current flows through the S/D electrodes and the graphene channel, which generates Joule heating (Figure 2(a)). The generated heat is proportional to the square of the current as shown in the Joule's first law (Equation (1))

$$H \propto I^2 \times R \times t, \quad (1)$$

FIG. 2. Current annealing method. (a) The schematic illustration of the current annealing method. The annealing current is flowing through source/drain electrode and graphene channel reducing the direct heat to the Parylene C substrate. (b) Representative drain current change over time during the current annealing with the drain voltage (V_D) of 2.5 V and 1.0 V. The initial current increase (139.0% I_D increase) is attributed to the decrease of contact resistance, and the abrupt current drop is attributed to the damage to the graphene ($V_D = 2.5$ V case). Negligible current increase is seen when the V_D is low (1.0 V) due to the low Joule heating. (Inset) Magnified view of drain current change at $V_D = 1.0$ V (3.6% I_D increase). (c) Scanning electron microscopy (SEM) image of the graphene before current annealing. (d) The SEM image of the damaged graphene after current annealing.

where H is Joule heating, I is the current traveling through element, R is the resistance of element, and t is time.

The current annealing method has advantages in terms of the localized heat generation and the controllable heating with an appropriate current level. The localized heat generation would substantially reduce the heat damage to the Parylene C substrate compared to the thermal annealing that is applying the heat to the entire device.

The representative drain current (I_D) change during the current annealing with the drain voltage (V_D) of 2.5 V is shown in Figure 2(b). The initial drain current of 0.59 mA was increased to 1.41 mA (139.0% increase) during the current annealing, which is attributed to the decreased contact resistance between the S/D electrodes and graphene. The drain current was abruptly decreased to 10^{-10} – 10^{-11} , a range after the peak and slight degradation, which may be attributed to the damage on the graphene. On the other hand, when V_D was 1.0 V, there was negligible current increase from 104 μ A to 107 μ A (3.6% increase) compared to the $V_D = 2.5$ V case (Fig. 2(b) and inset). This indicates that the current annealing effect is negligible when the V_D and I_D are low due to the low Joule heating. In order to investigate the physical damage on graphene, scanning electron microscope (SEM) images of the graphene on the S/D electrodes and the bottom gate were taken before and after the current annealing as shown in Figures 2(c) and 2(d). Figure 2(d) shows the damaged graphene after the current annealing that could support the abruptly decreased drain current. In [supplementary material](#), Figures S1 and S2, we show similar trends of the drain current and the damaged graphene observed in other investigated samples. Figure S1 shows the detailed trend of drain current change depending on the devices. In Figure S2, the SEM images show the different physical damage to the graphene that may be attributed to the different initial contact condition between S/D electrodes and graphene. However, all the samples showed the increase in initial drain current, which verifies the effect of the current annealing on the performance improvement.

In order to investigate the optimal annealing current without destroying the device, a maximum current annealing power before the device breakage has been calculated using

$$P_{\max} = V_D \times I_{D, \text{peak}}, \quad (2)$$

where $P_{\max}$ is the maximum current annealing power, V_D is the drain voltage, and $I_{D, \text{peak}}$ is the peak drain current.

Figure 3 shows the calculated maximum current annealing power for the device on Parylene C substrate and the device on silicon substrate. The fabrication process and the device dimension of the devices on silicon substrate were the same except the substrate. The maximum current annealing power of the Parylene C device and the silicon device were calculated as 3.8 ± 1.4 mW and 41.3 ± 20.9 mW, respectively. The result indicates that the Parylene C substrate can allow around ten times smaller current annealing power compared to the silicon substrate in this device structure, which could be anticipated by the lower thermal

FIG. 3. Maximum current annealing power allowed to the graphene transistors on Parylene C and silicon substrates. The device on Parylene C could allow around ten times smaller power than the device on silicon.

FIG. 4. Transfer curves (I_D - V_G) before and after current annealing. (a) Transfer curves for the device with larger drain current change after current annealing (134.0% increase of the maximum I_D). (b) Transfer curves for the device with smaller drain current change (13.6% increase of the maximum I_D). The different I_D change is attributed to the different initial condition between graphene and source/drain electrodes.

conductivity of Parylene C than that of silicon.^{26,27} In practical research, the maximum current annealing power can be used to estimate the applying annealing voltage in a device. Typical annealing voltage in our Parylene C devices ranged between 2.5 and 3 V, and the voltage in the silicon devices ranged between 5.5 and 7 V. The calculated maximum current annealing power and the comparison between the two substrates would provide informative guidelines to make Parylene C-based flexible electronics.

Figure 4 illustrates the transfer (I_D - V_G) curves before and after the current annealing. The amount of current annealing effect on the drain current and channel resistance was somewhat different depending on the devices. Figure 4(a) shows a large increase in the amount of drain current (134.0%) after current annealing. On the other hand, Figure 4(b) shows a relatively smaller increase in the drain current (13.6%). As described previously, this difference may be attributed to the different initial condition of the device (Figs. S1 and S2). However, all the devices showed the drain current increase (i.e., channel resistance decrease) after current annealing. Also, the increase in field-

effect mobility was shown ranging from 24.0% to 41.1%. This indicates that the current annealing contributes to improve both channel resistance and field-effect mobility. More detailed studies of the current annealing effect on the contact resistance and the carrier mobility would be helpful to assess the method precisely. As the effect of thermal annealing in various types of transistors suggested, the Joule heating generated by current annealing would be one of the main factors that decreases the contact resistance between graphene and S/D electrodes, and thus increase the drain current.^{20,22}

Figures 5(a)–5(c) illustrate the representative transfer curves (I_D - V_G), the transconductance (g_m) curves, and the output curves (I_D - V_D) of a flexible graphene transistor after current annealing, respectively. The transistor was annealed with a drain voltage of 2.5 V based on the study of the current annealing method. The electrical characteristics measurement and the current annealing were performed using a semiconductor parameter analyzer, HP 4155. In the transfer curves and the g_m curves, the gate voltage was swept from -4 V to 4 V while varying the drain voltage from 0.1 V to

FIG. 5. Representative electrical measurement results after current annealing. (a) Transfer curves (I_D - V_G) of a fabricated flexible graphene transistor on Parylene C substrate. (b) Transconductance (g_m) curves. The transistor shows PMOS-like behavior with the Dirac points located at positive gate voltage. (c) Output curves (I_D - V_D) with various gate bias from -4 V to 4 V.

0.9 V in step of 0.2 V. In general, the graphene transistor showed ambipolar characteristics with electron and hole current on either side of the Dirac points around 1 V to 1.5 V. In specific, however, the transistor showed rather PMOS (p-type metal oxide semiconductor) characteristic with the electron-hole asymmetry in which the Dirac points are located at positive gate voltage. It is known that the PMOS-like characteristic is attributed to the adsorbates on graphene such as polymer residues or the oxygen doping during graphene growth and transfer process.^{28,29} The on-current (I_{on}) and the g_m were linearly increased as the drain voltage was increased from 0.1 V to 0.9 V. The maximum $g_{m,\text{max}}$, I_{on} , and $I_{\text{on}}/I_{\text{off}}$ ratio at $V_D = 0.9$ V were 58.1 μS , 0.165 mA, and 1.76, respectively. The field-effect mobility (μ_{FE}) calculated with the following equation was 533.5 cm^2/Vs :

$$\mu_{\text{FE}} = \frac{L_{\text{ch}} \times g_{m,\text{max}}}{W_{\text{ch}} \times C_g \times V_D}, \quad (3)$$

where μ_{FE} is the field-effect mobility, L_{ch} is the channel length, W_{ch} is the channel width, $g_{m,\text{max}}$ is the maximum transconductance, C_g is the gate dielectric capacitance, and V_D is the drain voltage.

For the output curves in Figure 5(c), the drain voltage was swept from 0 V to 1.0 V while varying the gate voltage from -4 V to 4 V in step of 2 V. The drain current was not saturated well as previously reported in other graphene transistors. This is attributed to the zero bandgap nature of graphene, which results in no depletion regions in the channel. In the ambipolar graphene transistors, a different polarity charge is generated at the drain side rather than forming a depletion region. The lack of depletion region means there is no decrease in the carrier density in the channel near the drain side, which leads to the current saturation in field-effect transistors. We expect that the limitation of non-saturated graphene transistors could be overcome by combining various approaches such as adding low-doped silicon underneath the graphene³⁰ or shifting Dirac points by drain bias induction.²⁹

In summary, a flexible graphene transistor on Parylene C substrate that can be used as an active device in implantable biomedical devices has been demonstrated. We expect the flexible graphene transistors could be integrated in the graphene-based implantable neural electrodes in a monolithic manner to integrate active circuitry into the device. The addition of circuitry would enable making amplified and multiplexed sensors.³¹ In addition, the low temperature processes and the current annealing method introduced in this paper would be useful not only for the Parylene C-based graphene transistors but also for other flexible devices such as transition metal dichalcogenide monolayers (TMDC)-based transistors^{32,33} and nanomembrane-based electronics.^{34,35}

See [supplementary material](#) for additional trends of drain current change and SEM images.

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