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Silicon technologies for arrays of Single Photon Avalanche Diodes

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Abstract

In order to fulfill the requirements of many applications, we recently developed a new technology aimed at combining the advantages of traditional thin and thick silicon Single Photon Avalanche Diodes (SPAD). In particular we demonstrated single-pixel detectors with a remarkable improvement in the Photon Detection Efficiency in the red/near-infrared spectrum (e.g. 40% at 800nm) while maintaining a timing jitter better than 100ps.

In this paper we discuss the limitations of such Red-Enhanced (RE) technology from the point of view of the fabrication of small arrays of SPAD and we propose modifications to the structure aimed at overcoming these issues. We also report the first preliminary experimental results attained on devices fabricated adopting the improved structure.

Keywords

Single-Photon Avalanche Diode (SPAD); Photon Detection Efficiency (PDE); Time Correlated Single Photon Counting (TCSPC); Enhanced Photon Detection Efficiency; Red-Enhanced SPAD; RE-SPAD; SPAD arrays; Photon Counting

1. INTRODUCTION

A significant breakthrough in the field of single photon detection is represented by the recent introduction of a silicon SPAD, namely Red Enhanced SPAD (RE-SPAD)^{[1], [2]}, capable of attaining a good Photon Detection Efficiency (PDE) in the near infrared range (e.g. 40% at a wavelength of 800nm) while maintaining a remarkable timing jitter of about 100ps FWHM. Such a detector overcomes the limitations that are typical of classical thin^[3] and thick^[4] SPADs; in particular, the formers attain a limited PDE at longer wavelengths (e.g. 15% at a wavelength of 800nm), while the latter suffer of a poor photon timing jitter of many hundreds of picoseconds FWHM. The use of such devices has already proved to be remarkably advantageous in a few applications^{[5], [6], [7], [8], [9]} and we expect many more

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demonstrations to come in a near future for fields ranging from single molecule analysis to quantum key distribution.

On the other hand, many single-photon techniques either cannot be implemented by using single-pixel detectors, or would greatly benefit from the use of arrays with at least a small number of pixels. Significant examples are parallel Fluorescence Correlation Spectroscopy (parallel FCS)^{[10], [11]}, high-throughput Single Molecule Analysis^{[12], [13]}, or spectrally resolved Fluorescence Lifetime Imaging (sFLIM)^[14]. Although many of such techniques would take advantage of an improved PDE, especially in the near-infrared range, no arrays exist that provide such a feature. In particular, thick SPAD technology is non-planar and therefore not suitable for the monolithic integration of more than one device on a single chip^[15]; as opposite, high-voltage CMOS technology allows the fabrication of arrays of SPADs with a large number of pixels (e.g. 32×32 or 64×32)^{[16], [17], [18]} but at the expense of a strong limitation in the attainable PDE, especially at the longer wavelengths (e.g. 7% at 800nm^{[16], [17]}). More scaled CMOS technologies allow even large arrays^[19] (e.g. 160×128), with more electronics integrated on the same chip of the detector, but with a significant degradation in the performance of the SPAD. A solution somewhere in between thick SPAD and CMOS SPAD is represented by thin SPAD fabricated by using a custom technology; actually, by using this technology it is possible to fabricate small arrays of detectors^{[20]–[23]} (e.g. 60-pixels, 12×4 pixels, 8×8 pixels) with overall good pixel performance. However their PDE at longer wavelengths (about 15% at a wavelength of 800nm) is somehow limiting in many applications. Finally, single photon detection on a small number of pixels can be achieved also by using multi-anode PMTs; however, besides suffering of all the limitations typical of vacuum-tube devices, their near-infrared PDE is even more limited^[24].

In order to overcome the aforementioned limitations, RE-SPAD technology has been conceived from the scratch to be compatible with the fabrication of arrays^[25]. In particular, the device structure has been designed to be manufactured by using a planar technology. Nevertheless, some crucial technological issues are still to be addressed in order to attain a fully operating array of RE-SPAD^[26].

In this paper we will discuss the requirements that a SPAD structure must fulfill to make possible the fabrication of SPAD arrays either for photon counting or photon timing applications. We will then review the modifications we implemented to the RE-SPAD structure to this aim, and we will present first preliminary experimental results attained on devices fabricated adopting the improved structure.

2. THIN SPAD: STRUCTURE AND ARRAYS' IMPLEMENTATIONS

In this section we will briefly review the structure of a thin SPAD and we will analyse the role of different device regions in making possible the fabrication of SPAD arrays, either for photon counting or photon timing. In particular Figure 1 represents the typical structure of a double epitaxial SPAD^[27] developed at Politecnico di Milano. The device is fabricated starting from an n-type substrate on top of which a p-type epitaxial layer has been grown. The latter is composed of two different regions, respectively a p⁺ *buried layer* and p[−] *quasi-*

intrinsic layer. During following fabrication steps, mainly four regions are manufactured: the *isolation*, the *sinker*, the *shallow n* and the *enrichment*. As suggested by its name, *shallow n* is an n-type, thin diffusion that constitutes the cathode of the device. The *enrichment* is a medium thickness, p-type region that has a two-fold purpose: on one hand, the enrichment region is needed in order to reduce the breakdown value in the central region of the device, thus avoiding premature edge breakdown; on the other hand, its doping profile is designed in order to suitably shape the electric field in the multiplication region, with the aim of optimizing device performance^[28]. Although not belonging to the active region, the *isolation* and the *sinker* have, nevertheless, an important role in assuring the proper operation of the device, either as a single pixel or as an element of an array. In fact, the *sinker*, in conjunction with the *buried layer*, provides a low resistivity path for the current flowing from the SPAD active area to the anode contact. Similarly, the *isolation*, in conjunction with the *n-type substrate*, forms a sort of well that entirely surrounds the device anode; therefore by reverse biasing the isolation-anode junction it is possible to electrically isolate the SPAD from adjacent devices.

The role of the aforementioned regions can be fully understood by analysing a few kinds of arrays fabricated by using a double epitaxial SPAD. Arrays for photon counting applications, i.e. for applications in which a picosecond temporal resolution is not needed, can be fabricated simply by placing multiple devices on the same silicon chip^{[20], [21], [22], [23]}. Although useful, attaining an electrical isolation between anodes is not mandatory in this particular case. In fact, it is possible to operate the devices in a common anode configuration, in which every cathode is connected to a different Active Quenching Circuit (AQC). The isolation region is nevertheless of the utmost importance in order to reduce the direct component of the optical crosstalk between adjacent pixels^{[29], [30]}.

On the contrary, attaining a full isolation between SPADs is essential for timing arrays. In fact, with large active area devices^[31], a temporal resolution of a few tens of picosecond can be attained only if the avalanche current is sensed by means of a suitable circuit^[32] as the one depicted in Figure 2.a. The avalanche current is injected into a low impedance network that converts it into a voltage signal that is in turn sensed by a low voltage comparator^[33]. However, such a scheme requires that both the anode and the cathode are electrically isolated from adjacent devices.

Actually, while the circuit of Figure 2.a provides excellent results for a single SPAD, it cannot be properly used for arrays. In fact the disturbances induced by the commutations of adjacent devices prevents the operation of the comparator at low threshold. Such an issue has been overcome by integrating, on the same chip of the detector, a frontend for reading the avalanche current^{[34], [35]}. The capacitance reduction that results from monolithic integration makes possible to attain the same timing performance while reading the voltage signal at a much higher threshold. The adopted scheme is reported in Figure 2.b; its implementation requires the integration, on the same chip of the detector, of a few n-channel MOSFETs. The isolation region provides therefore not only the electrical isolation from the anodes of adjacent devices, but also from the body region of n-MOS transistors.

Recently, we demonstrated that timing performance can be attained on SPAD arrays also by using a solution in which the avalanche current is read by an external circuit (i.e. not integrated on the same chip of the detector). This solution is based on a front-end circuit considerably different from the one represented in Figure 2.a and based on a transimpedance amplifier^{[36], [37]}. However, also this solution requires a full isolation of the pixels as the AQC and the avalanche readout circuit are connected at the opposite terminals of the active junction.

3. RE-SPAD: STRUCTURE

The RE-SPAD has been designed starting from the double epitaxial structure of Figure 1. The structure has been modified in order to improve the PDE in the red / near-infrared range. To this aim, the thickness of the p^- layer has been considerably increased (from about 3 to about 10 μm) in order to improve the photon absorption probability, especially for the longer wavelengths^[38]. Actually, other modifications to the device structure are needed in order to optimize device performance. In particular a Boron peak inside the quasi-intrinsic layer provides the degrees of freedom needed in order to optimize the shape of the electric field in the multiplication region while limiting the breakdown voltage^[1]. However, for the sake of this paper, we can safely neglect such modifications and focus on the simplified RE-SPAD cross-section reported in Figure 3. The increased thickness of the quasi-intrinsic layer p^- has two main consequences: the sinker does not reach the buried layer anymore and similarly the isolation is not connected anymore with the n^+ substrate. In the following sections we will thoroughly analyse the impact that these facts have on the operation of the RE-SPAD both as a single detector and as an element of an array.

4. RE-SPAD: ISOLATION ISSUES AND SOLUTIONS

4.1 Limitations arising from the lack of electrical isolation

The fact that the isolation does not reach anymore the n^+ substrate prevents the fabrication, on the same silicon chip, of multiple p-type wells electrically isolated one from the others. The most evident and obvious consequence is the impossibility of fabricating SPADs with anodes isolated one from the others and the impossibility of integrating some basic front-end electronics on the same silicon chip. Therefore, without modifications aimed at recovering full isolation between pixels, the RE-technology does not allow the fabrication of arrays for photon-timing applications.

On the contrary, the design of arrays for photon-counting applications is still possible with unmodified RE-technology, provided that the detectors are operated with a common anode voltage and that an AQC is connected to each cathode. Nevertheless this solution presents some remarkable limitations that deserve a more in-depth discussion.

It has already been demonstrated, both theoretically^[25] and experimentally^[1], that RE-SPADs attain the best performance when operated at an overvoltage significantly large than the 5V that are typically used for thin SPADs. For example the curves reported in [1] have been attained at an overvoltage $V_{ov}=20\text{V}$ that guarantees a good PDE while maintaining the DCR very low. However, for some applications in which the PDE is especially important or

in which DCR is dominated by the background, a further increase of the overvoltage might be really advantageous.

The higher applicable overvoltage is limited by the edge breakdown of the junction $V_{BD,EDGE}$. In fact, in order to avoid the operation of the detector in edge-breakdown conditions, the voltage $V_{BD}+V_{OV}$ applied to the diode cannot exceed $V_{BD,EDGE}$:

$$V_{BD}+V_{OV}<V_{BD,EDGE} \quad (1)$$

For a given value of $V_{BD,EDGE}$, the relation (1) poses a limitation to V_{OV} that depends on the value of V_{BD} . For instance, for $V_{BD,EDGE}=60V$, the maximum overvoltage is $V_{OV|MAX}=20V$ if $V_{BD}=40V$, but it is only $V_{OV|MAX}=10V$ if $V_{BD}=50V$. This poses a limitation in the degrees of freedom the designer has in the choice of V_{BD} , hence in choice of the doping profile to optimize the device performance.

The limitation of relation (1) can be overcome by surrounding the cathode with one or more guard rings (see Figure 4). In this case the outer guard ring (GR2 in Figure 4) still need to be biased at voltage lower than $V_{BD,EDGE}$. However, the inner guard rings and the cathode can be biased at higher voltages thanks to the shaping of the electric field provided by the guard rings structure. In this case the limitation to the voltage $V_{BD}+V_{OV}$ becomes:

$$V_{BD}+V_{OV}<V_{BD,EDGE}+n_{GR} \cdot \Delta V_{GR} \quad (2)$$

where n_{GR} is the number of guard rings and V_{GR} is the voltage applied between two adjacent guard rings or between the inner guard ring and the cathode (see Figure 4). Of course a large number of guard rings provides a higher flexibility in the choice of V_{BD} and V_{OV} , but it comes at the expenses of an increased complexity in the biasing of the device and in a reduction of the attainable fill factor. On the other hand, the maximum value of

V_{GR} is limited by the punch-through effect: as the voltage V_{GR} is increased, the electron potential-barrier between two guard rings is decreased until a large current starts flowing between them. The punch-through voltage can be raised by increasing the distance between the rings, but only up to a certain point. In fact, if the rings are placed too far apart, they lose their effectiveness in shaping the electric field and therefore in preventing edge breakdown.

While the introduction of guard rings allows us to have a larger value of V_{OV} and/or V_{BD} , it makes challenging to operate the detector with an AQC connected to the cathode. Therefore, also in this case, it would be really useful to recover a full isolation of the detector, to operate the SPAD array with an AQC connected to each anode of the array.

4.2 Technological solutions for recovering full electrical isolation

From the previous subsection it is evident that the lack of electrical isolation is the main obstacle to the development of an array of RE-SPADs. In the past we have already shown that a convenient approach to recover the full electrical isolation is to resort to Dielectric Isolation(DI)^[26].

In this case, the current flow between adjacent devices is prevented by surrounding each detector with a deep trench filled with isolating material (see Figure 5). Such a structure can be manufactured by using technological steps that are almost standard in today's silicon fabs. In particular, after defining the regions for DI by means of standard lithography, deep trenches are etched into the substrate by using plasma-assisted processes; their walls are then covered with silicon dioxide, with a thickness suitable for attaining the desired isolation; trenches are then refilled with polysilicon and capped with an additional protective silicon dioxide layer; finally the structure is planarized to ease the execution of the following processing steps.

Electrical isolation with deep trenches presents remarkable advantages when compared with junction isolation. First of all, dopant diffusion induced by trench manufacturing is fairly limited; in fact, both trenches etch and material deposition are carried out at low temperature while a limited thermal budget is needed only to densify silicon dioxide at the end of the process. Overall thermal budget is indeed reduced if diffused isolation regions are fully replaced by deep trenches. Another remarkable advantage of DI is its compactness. Actually, junction isolation requires a considerable amount of space essentially because dopant diffusion happens both vertically and horizontally. So when a dopant is vertically driven-in for a certain length L , it simultaneously diffuses laterally for a distance equal to about $0.7 L$. This process limits the minimum geometrical dimension attainable for the isolation region; moreover, to this dimension, one has to add the space needed for the extension of the depleted regions. On the contrary, for manufacturing trenches, nowadays processes are available that etches the silicon almost in one direction. For example Deep Reactive Ion Etching (DRIE) based on Bosch Process makes possible to attain trenches with an aspect ratio ranging from 10:1 to more than 20:1 (see for example [40]). Therefore trenches can be manufactured with a total occupancy of only a few microns.

The main issue with DI isolation is crystal defectiveness. Actually the stress that develops at the interface between silicon and silicon dioxide at the trenches walls can lead to the formation of crystal defects such as slips and dislocations. If these defects reach the SPAD active area they can act as generation and recombination centres with a dramatic impact on device noise. However, in the last years big advances in processing technology have strongly reduced the concentration of such defects. Moreover it has been demonstrated that the defects originate from the bottom of the trench and propagate diagonally along crystallographic axes; therefore they should not affect DCR provided that the active area of the device is placed at a suitable distance from the trench (e.g. $10\ \mu\text{m}$). However since SPADs are especially sensitive to such kinds of defects, this point deserves a detailed experimental verification.

5. RE-SPAD: SERIES RESISTANCE ISSUES AND SOLUTIONS

From the RE-SPAD cross-section reported in Figure 3 it is clear that the increased thickness of the p^- epi-layer prevents also the sinker from reaching the buried layer. This fact results in a remarkable increase of the SPAD series resistance. This is especially undesirable from the point of view of the temporal resolution; in fact, it has been demonstrated^[39] that an increase of the series resistance reduces the avalanche growth rate leading to a worsening of the

photon timing jitter. A very effective and general solution to this problem, perfectly compatible with the fabrication of arrays, comes once again from the use of deep trenches. Actually, a deep sinker can be attained if trenches walls are implanted right before oxide deposition. The resulting structure, depicted in Figure 6, presents once again significant advantages in terms of compactness. Moreover its fabrication does not require a significant additional thermal budget since the implanted Boron can be diffused during other high-temperature steps needed the fabrication of the device active area.

6. RE-SPAD: ANODE-SUBSTRATE BREAKDOWN ISSUES AND SOLUTIONS

In the device structures represented in Figure 1 and in Figure 6, the breakdown voltage of the junction between the anode and the substrate is usually determined by the doping level of the buried layer, being the doping concentration of the substrate significantly higher. Typical doping concentrations used for the buried layer of these devices result in anode-substrate breakdown voltage $V_{BD, A-SUB}$ ranging from 15 to 25V. In this section we will show that such a low breakdown voltage can severely limits the performance attainable with RE-SPAD arrays and we will analyze the solutions that can be adopted in order to overcome such limitations.

6.1 Limitations arising from anode-substrate breakdown voltage

Figure 7.a represents a typical configuration for operating a SPAD, in which the anode is connected to the AQC, the cathode to the voltage supply $V_{POL} = V_{BD} + V_{OV}$ and the substrate to the voltage supply V_{SUB} . The anode voltage is essentially switched between two different values by the AQC; in particular, the anode is kept to ground when the SPAD is waiting for a photon arrival, while it is raised to V_{QUENCH} after an avalanche has been triggered.

For the avalanche to be effectively turned off by the AQC, during the quenching phase the voltage across the SPAD must be lower than the breakdown voltage. For this reason the applied overvoltage V_{OV} must comply with the following relation:

$$V_{OV} < V_{QUENCH} \quad (3)$$

On the other hand, the anode voltage must always remain below the substrate voltage to prevent the forward biasing of the corresponding junction. For this reason also the following relation must be satisfied:

$$V_{QUENCH} < V_{SUB} \quad (4)$$

Finally, since the voltage applied to the anode-substrate junction when the SPAD is waiting for a photon arrival is exactly V_{SUB} , to prevent the breakdown of the junction itself, one has to comply also with following requirement:

$$V_{SUB} < V_{BD,A-SUB} \quad (5)$$

Combining the relations (3) – (5), it turns out that:

$$V_{OV} < V_{QUENCH} < V_{SUB} < V_{BD,A-SUB} \quad (6)$$

Relation (6) shows that the maximum overvoltage applicable to the detector is upper limited by the breakdown voltage of the anode-substrate junction. Since $V_{BD,A-SUB}$ is typically lower than 20V – 25V and since each of the inequalities in (6) must be satisfied with a certain tolerance (for example to avoid possible issues related to overshoots during fast transients), it is evident that there is a severe limitation to the maximum overvoltage applicable and therefore to the attainable performance especially in terms of PDE.

Such a limitation can be partially overcome in single-pixel RE-SPAD. In this case, the detector can be operated by using a configuration, such the one depicted in Figure 7.b, where the substrate is connected to V_{SUB} through a high value resistor R_{SUB} . By adopting this configuration, the substrate is still biased at the voltage V_{SUB} while waiting for a photon arrival; conversely, during the quench and the hold-off phase, the substrate reaches a higher voltage due to the capacitive coupling with the anode. This way, V_{QUENCH} is not required anymore to be lower than V_{SUB} and the applied overvoltage can therefore be larger than $V_{BD,A-SUB}$. Its maximum value actually depends on the raising of the substrate during the hold-off and therefore on the value of the parasitic capacitances.

Although the aforementioned solution works (with some remarkable limitations) in the case of single-pixel detectors, it cannot be applied to RE-SPAD arrays. In fact, in the latter, it is mandatory to keep the substrate at a very fixed voltage. If not, any fast transient due to the quenching of a SPAD would couple through the substrate both to the anodes and to the front-ends of the nearby detectors. The formers might result in spurious counts while the latters in a distortion of the recorded timing curves.

6.2 Technological solutions to increase the anode-substrate breakdown voltage

The previous discussion showed that increasing the breakdown voltage of the anode-substrate junction is mandatory in order to obtain the best performance with a RE-SPAD array.

The more obvious solution to address this problem is the reduction of the doping concentration in the buried layer. However, this approach is not viable since it would result in an increased value of the series resistance. Moreover, the reduction in doping concentration cannot even be compensated by increasing the thickness of the buried layer since this would result in a severe degradation of the lifetime of diffusion tail.

Figure 8 represents the solution we adopted. A lightly doped n-type layer has been interposed between the substrate and the buried layer. The thicker is the n^- layer, the higher

is the breakdown voltage since the space charge region can extend across it. In particular, a thickness of a few microns is sufficient to guarantee a breakdown voltage of many tens of Volts. The interposed n^- layer can be grown by using an epitaxial process; this solution is therefore perfectly compatible with the Red-Enhanced fabrication process.

7. PRELIMINARY EXPERIMENTAL RESULTS

Devices with the structure represented in Figure 8 have been fabricated at the Cornell Nanoscale Science and Technology Facility (Cornell University, Ithaca – USA) on 100mm silicon wafers. Fabrication has been carried out using conventional planar silicon technology and optical lithography.

In order to investigate the effects of the different modifications to the RE-SPAD structure, multiple wafers have been processed on the same run. Wafers are characterized by the presence or the absence of deep trench isolation or ninterposed layer. Moreover, in each wafer, different Boron doses have been used for the enrichment implantation in order to investigate the effect of the doping profile on device performance. Here we will report on a preliminary experimental characterization of these devices.

7.1 Anode-Substrate breakdown

Figure 9.a reports the reverse Current-Voltage (IV) characteristic of the Anode-Substrate junction. In particular, the red curve has been acquired on a device having the structure represented in Figure 8, while the blue curve on a device having the structure of Figure 1 (i.e. without the n^- interposed layer and without deep trench isolation). From the comparison of the two curves it is evident the beneficial effect of the n^- interposer layer on the junction breakdown voltage that increases from about 28V to about 88V. As pointed out in section 6.1, this result is really important for the optimal operation of RE-SPAD arrays, since it essentially removes the limitation to the maximum overvoltage coming from the breakdown of the anode-substrate junction.

7.2 Cathode-Anode edge breakdown

In each wafer, the enrichment region of a few devices has not been implanted with Boron. In this case the breakdown happens at the edge of the junction where the electric field is increased by the curvature effect. Therefore, these devices can be used for an easy and reliable measurement of the edge-breakdown voltage.

Figure 9.b reports the reverse Current-Voltage characteristic at cathode-anode junction, measured on one of such devices. From this curve it is possible to extract the edge-breakdown voltage $V_{BD,EDGE}=56V$.

7.3 Maximum operating voltage

Most of the devices fabricated have 3 guard rings in order to increase the maximum exploitable value of $V_{BD}+V_{OV}$, as illustrated in section 4.1. Figure 10.a represents the Current-Voltage characteristic measured between two adjacent rings. In particular, the curve of Figure 10.a has been obtained by connecting to ground the cathode and the two inner

guard rings (GR1 and GR2) and by applying a voltage sweep to outer guard ring (GR3) while maintaining the anode at a fixed voltage of -20V . The figure shows that the current flowing in GR3 is completely negligible for a voltage as high as 20V . Characteristics similar to that of Figure 10.a can be obtained by sweeping the voltage applied between GR2 and GR1 or between GR1 and the cathode.

From the relation (2), with $n_{\text{GR}}=3$, $V_{\text{GR}}=20\text{V}$ and $V_{\text{BD,EDGE}}=56\text{V}$ it is possible to calculate the maximum bias voltage that can be applied to the active junction of the detector without reaching the edge-breakdown: $V_{\text{BIAS|MAX}}=116\text{V}$.

As already pointed out before, such a high value provides us with a considerable degree of freedom in the choice of the breakdown voltage (V_{BD}) and/or of the operating conditions (V_{OV}).

7.4 Cathode-Anode breakdown

Figure 10.b reports the reverse Current-Voltage characteristic measured at the cathode-anode junction of three devices whose enrichment regions have been implanted with different Boron doses. The measurements have been carried out biasing the guard rings at suitable voltages in order to avoid the onset of edge-breakdown.

On one hand, curves reported in Figure 10.b confirm that we attained a wide range of breakdown voltages, suitable to study the effect of the electric field on device performance. On the other hand, the fact that we were able to measure breakdown voltages well above $V_{\text{BD,EDGE}}$ confirms the effectiveness of guard rings.

7.5 Photon Detection Efficiency

For some of the device fabricated, the Photon Detection Efficiency (PDE) has been measured resorting to a standard setup based on a monochromator and an integrating sphere.

Figure 11 reports an example of PDE as a function of the wavelength, measured on a dose-B SPAD, biased at an overvoltage $V_{\text{OV}}=15\text{V}$. This data confirms the results previously obtained^[2] with the Red Enhanced SPAD structure of Figure 3 (i.e. without deep trench isolation and without n^- interposed layer).

8. CONCLUSIONS

In this paper we discussed how we modified the Red-Enhanced structure to make it compatible with the fabrication of small arrays of SPADs. A preliminary experimental characterization of some devices recently fabricated, has confirmed the effectiveness of the solutions adopted in removing the issues previously identified. Although promising, such results still need to be complemented with a deeper and more extended investigation of additional device parameters (dark count rate, temporal resolution, afterpulsing probability, optical cross talk probability, etc.) in order to assess the readiness of this technology for the fabrication of SPAD arrays with high Photon Detection Efficiency and excellent temporal resolution.

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Figure 1.
Cross section of a typical double epitaxial thin SPAD.

(a)

(b)

Figure 2. Avalanche current pick-up circuit for single pixel detectors (a) and for SPAD arrays (b).

Figure 3.

Cross section of a RE-SPAD. Note that the isolation and the sinker regions do not reach respectively the substrate and the buried layer.

Figure 4. Cross section of a RE-SPAD with additional Guard Rings (GR) to prevent edge breakdown at high overvoltages.

Figure 5.
Cross section of RE-SPAD with isolation implemented by means of deep trenches.

Figure 6.

Cross section of RE-SPAD with isolation implemented by means of deep trenches. Note Boron implantation on trenches wall in order to reduce series resistance.

Figure 7.
Configuration for operating a SPAD with a fixed voltage at the substrate (a) or with a semi-floating substrate (b).

Figure 8.

Cross section of RE-SPAD with isolation implemented by means of deep trenches and a lightly doped n-type layer interposed between the buried layer and the substrate to increase breakdown voltage at this junction.

(a)

(b)

Figure 9.

(a) Reverse current-voltage characteristic at the anode-substrate junction of a device with the structure of Figure 8 (red) and of Figure 1; the presence of the n- interposed layer increase the breakdown value to about 88V. (b) Reverse current-voltage characteristic at the cathode-anode junction of a device without Boron implantation in the enrichment region; the curve shows that the edge breakdown happens at about 56V.

(a)

(b)

Figure 10.

(a) Current flowing at the outer guard ring (GR3) as a function of the voltage applied between GR3 and GR2. The measurement has been carried out with the inner guard ring (GR1) and the cathode shorted with GR2, while the anode is kept at -20V . The current flowing at GR3 is negligible for a voltage as high as 20V . (b) Reverse current-voltage characteristic at the cathode-anode junction of three SPADs implanted with different enrichment doses; the corresponding breakdown values range from 25V to 65V

Figure 11.

Cross section of RE-SPAD with isolation implemented by means of deep trenches.