Published in final edited form as:

IEEE Trans Nucl Sci. 2015 October 1; 62(5 Pt 2): 2327–2333. doi:10.1109/TNS.2015.2465377.

A 2D 4×4 Channel Readout ASIC for Pixelated CdTe Detectors for Medical Imaging Applications

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Abstract

We present a 16-channel readout integrated circuit (ROIC) with nanosecond-resolution time to digital converter (TDC) for pixelated Cadmium Telluride (CdTe) gamma-ray detectors. The 4×4 pixel array ROIC is the proof of concept of the 10×10 pixel array readout ASIC for positron-emission tomography (PET) scanner, positron-emission mammography (PEM) scanner, and Compton gamma camera. The electronics of each individual pixel integrates an analog front-end with switchable gain, an analog to digital converter (ADC), configuration registers, and a 4-state digital controller. For every detected photon, the pixel electronics provides the energy deposited in the detector with 10-bit resolution, and a fast trigger signal for time stamp. The ASIC contains the 16-pixel matrix electronics, a digital controller, five global voltage references, a TDC, a temperature sensor, and a band-gap based current reference. The ASIC has been fabricated with TSMC 0.25 μm mixed-signal CMOS technology and occupies an area of $5.3 \text{ mm} \times 6.8 \text{ mm}$. The TDC shows a resolution of 95.5 ps, a precision of 600 ps at full width half maximum (FWHM), and a power consumption of 130 μW . In acquisition mode, the total power consumption of every pixel is 200 μW . An equivalent noise charge (ENC) of 160 e^- RMS at maximum gain and negative polarity conditions has been measured at room temperature.

Keywords

Analog-digital conversion; application specific integrated circuits; energy resolution; gamma-ray detectors; low-power electronics; positron emission tomography; semiconductor radiation detectors

I. Introduction

Pixelated Cadmium Telluride detectors are commonly used in X-ray and Gamma-ray detection since they are excellent absorbers for the high energy range X-ray photons and provide a large number of charge carriers for each incident gamma photon due to the fairly low ionization energy of 4.43 eV per electron-hole-pair [1]. Moreover, they can be used at room temperature due to their energy band gap of 1.44 eV and can be produced with thickness up to 15 mm. Despite all the positive properties mentioned above, the energy resolution of CdTe detectors gets smeared due to the poor charge collection efficiency of holes [2]. Nevertheless, the energy and time resolution can be improved dramatically by estimating the depth of interaction (DOI) of the photon inside the detector [3].

A common architecture of high-resolution front-end electronics of readout ASICs for single, strip or pixelated solid-state detectors is shown in Fig. 1 [4]–[7]. Every pixel's output is multiplexed and sent to a common ADC that can be located in the same readout ASIC or can be off-chip. The discriminator generates the trigger signal when the shaped pulse crosses a tunable threshold voltage reference.

The timing of the trigger output of a discriminator for Gaussian-shape input pulses increases inversely with the signal's peak height. This feature is known as time-walk [8]. Although this dependency might be partially corrected with proper calibration techniques, the low slope of the shaped signal at low threshold voltage levels introduces large jitter in the trigger signal, which cannot be corrected. Note that the longer the shaper's peak time and the higher the order of the integrator, the larger the jitter of the trigger independently of the threshold voltage reference. The architecture of Fig. 1 offers limited time resolution when the shaper's peak time is designed of few μs .

Based on the proposed design for PET scanner [9], the photon flux is parallel to the CdTe detector's electrodes as illustrated in Fig. 2. In this particular case, the probability for every photon to interact close to the cathode (case a) is equal to the probability to interact close to the anode (case c) or half way (case b), and it is independent of the energy of the photon. Therefore, the degradation of the collection efficiency due to the limited mobility of holes in cadmium telluride detectors plays a fundamental role in the design of the electronics and the biasing conditions.

If the energy of the 511 keV photons can be measured with a resolution of 1% at FWHM, a large fraction of unwanted photons that have undergone a scattering process, before reaching the detector, can be eliminated. Thus one can obtain a data sample with high signal-to-noise ratio (SNR) for the PET image.

The analysis of the dependency of the charge collection efficiency with the depth of interaction (i.e., the distance to the cathode/anode of the photon interaction in the proposed detector design) in 2-mm thick CdTe detectors concludes that the total charge of electrons and holes must be integrated to achieve the energy of 511 keV with 1% resolution at FWHM [10].

For CdTe detector at room temperature, the ratio of the electrons mobility ($\sim 1100 \text{ cm}^2/\text{V} \cdot \text{s}$) to that of holes mobility ($\sim 100 \text{ cm}^2/\text{V} \cdot \text{s}$) is around 11 [11], [12]. Considering that the mobility ratio increases inversely with temperature, the timings of the pixel front-end electronics have been designed to provide an energy resolution of 0.1% at 511 keV regardless the total charge collection time, i.e., cases a, b, or c of Fig. 2.

II. VIP-PIX ASIC and Pixel Architecture

The front-end electronics of every pixel has been designed and optimized for positron emission tomography scanners based on the multiple stacking of pixelated Cadmium Telluride detectors such as the described in [9]. Fig. 3 shows the block diagram of the pixel front-end electronics. As an alternative to the high energy-resolution front-end architecture shown in Fig. 1, we connected the unfiltered signal coming from the pre-amplifier to the discriminator to provide a fast trigger with small time-walk and less dependent on the depth of interaction. Using the unfiltered fast output of the pre-amplifier reduces the jitter of the trigger at the expenses of lower sensitivity, i.e., minimum detectable energy of the discriminator.

The baseline restore time of the pre-amplifier and the shaper's peak time, are programmable with a tuning range that covers from $10 \mu\text{s}$ to $200 \mu\text{s}$, and from $2 \mu\text{s}$ to $30 \mu\text{s}$ respectively. With such long preamplifier and shaper peak times, the analog front-end is able to provide 0.1% resolution regardless the total charge collection time of the proposed biasing conditions of the detector. For a charge collection time of 200 ns (corresponding to a CdTe detector thickness of 2 mm, -1000 V/mm detector bias, and pure holes charge collection), the minimum peak time of a first order CR-RC shaper to have a collection of 99.9% of the energy is $2 \mu\text{s}$ provided a minimum baseline restore time of $20 \mu\text{s}$.

The original specifications of the pixel front-end electronics are listed in Table I [13]. Note that we specify two figures of merit for the equivalent noise charge (ENC) since the discriminator is applied directly to the unfiltered pre-amplifier signal. Usually the discriminator is applied after the shaper, so the ENC for the trigger is equal to the ENC after the shaper or the sample and hold circuit.

It is worth to mention that the power consumption limitation of the pixel comes from the fact that a complete PET scanner would have in total more than 6 million pixels. With a power consumption of $200 \mu\text{W}$ per pixel, the total power dissipation inside the PET scanner would be in the order of 1.2 kW, which will require already a complex cooling system to keep detectors and ASICs at the proper working temperature.

The architecture of the final VIP-PIX with 100 pixels will consist of a 10×10 matrix of pixel front-end electronics connected and controlled by a digital controller. The ASIC features as well a 32-bit chip ID, a TDC, a temperature sensor with digital output, a temperature-compensated current reference, and five voltage DACs with 6-bit resolution each to provide global voltage references such as the global threshold of the discriminators, the biasing of the pre-amplifiers and shapers, and the top and bottom references that define the dynamic range of the ADCs. The VIP-PIX ASIC will be connected to CdTe detectors of $10.2 \text{ mm} \times 10.2 \text{ mm} \times 2 \text{ mm}$ size with voxel size of $1 \text{ mm} \times 1 \text{ mm} \times 2 \text{ mm}$ [13].

The layout of the implemented pixel with an indication of the building blocks is in Fig. 4. The total active area of the pixel is $700\ \mu\text{m} \times 500\ \mu\text{m}$. The global voltage references and every pixel's current reference are located in the analog bus. The digital bus contains the individual control signals of every pixel, plus the common digital lines such as the digital reset, the pixel configuration register data, and the pixel matrix data readout digital bus.

All blocks of each pixel's analog front-end electronics have adjustable parameters that are set to the values stored in the pixel's configuration register. The local digital controller sends the control signals to the configuration register, to the ADC, and to the analog-reset circuitry according to the status of the pixel. The later is set by the ASIC's digital controller with three individual signals: clock, 2-bits status, and analog reset control.

With 2 status lines, the pixel is selected to work in four different operation modes: standby mode (00), digital to analog conversion mode (01), data readout mode (10), and configuration register programming mode (11). During data acquisition, only when a photon interacts with the detector and deposits sufficient energy to set the trigger high, the clock is sent to the triggered channel and the neighboring ones. The data of the ADC of the selected channels will be available on the bus, and it will be stored, by the ASIC controller, channel by channel.

III. 4×4 Pixel Matrix Measurements Results

A 4×4 pixel ROIC with all the functionalities of the final 10×10 pixel array VIP-PIX ASIC has been fabricated with TSMC $0.25\ \mu\text{m}$ CMOS technology. Fig. 5 shows the microphotography of the fabricated ASIC. It includes a 2D pixel matrix with 16 independent pixels readout electronics, a time to digital converter, a band-gap current reference, five adjustable voltage references, a temperature sensor, and the digital controller implemented with TSMC standard cells library.

A total of five ASICs, i.e., 80 pixels, have been fully characterized. The measured DC current consumption of the pixel matrix electronics is $1.21 \pm 0.01\ \text{mA}$. This corresponds to a pixel power consumption of $190 \pm 4\ \mu\text{W}$. Prior to acquisition mode, the tuning parameters of the pixels such as the feedback resistor, the local discriminator threshold, and the peak time of the shaper are adjusted to equalize the DC offset of the pre-amplifiers and the energy path gain.

The characterization of each pixel in the matrix is achieved by 3 set of measurements: the noise at the output of the preamplifier, the linearity and the energy resolution at the level of ADC, and the jitter time of the trigger versus pulse height.

A. Noise Level

The noise level at the output of every pre-amplifier has been obtained in two steps. First, the DC output voltage of every pre-amplifier was obtained by scanning the global threshold reference in steps of 16 mV and checking when the output of the discriminator flips its value. Second, we fixed the global threshold to the value previously found and we scanned the local threshold with the fine-tuning 7-bit current DAC of the pixel. For every value of

the internal DAC, the number of triggers due to the noise within a window of one second was recorded. With this second scan, a more accurate measurement of the baseline of the preamplifier and the peak-to-peak amplitude of the noise were obtained. Assuming a flat noise spectrum density, the RMS value of the noise was obtained as 1/6 of the peak-to-peak amplitude.

In Fig. 6 the distribution of the minimum threshold for 160 pixels (i.e., positive and negative polarity) at maximum preamplifier gain (1.27 mV/keV) is shown. The minimum threshold corresponds to 5 times the sigma of the noise measured. The mean value of the minimum threshold is 5.3 keV which correspond, approximately, to a sigma of 1.06 keV. Using 4.46 eV, the ionization energy for a pair of e-h in CdTe, the pre-amplifier equivalent noise charge is e^- -RMS.

B. Linearity and Resolution

The linearity and the energy resolution have been characterized with external test pulses injected into the pixels' internal test pulse capacitors. Every preamplifier includes a test pulse capacitor that matches the preamplifier feedback capacitor. A switch is cascaded to the testing capacitor to enable the injected charges to be integrated by the preamplifier. All the channels were characterized with 1000 measurements per test pulse amplitude, and a Gaussian fit was used to obtain the mean and the standard deviation values of the measured energy. The linearity of the energy response of 80 pixels is shown in Fig. 7 for positive and negative polarity. The inset plot shows the error of the measured response from a unity gain linear fit in keV. Every pixel's front-end non-linearity is corrected individually offline in order to achieve 0.1% resolution. Fig. 8 shows the energy resolution for positive and negative polarity. The gain of the front-end electronics was calibrated with radioactive sources with ^{57}Co , and ^{133}Ba , and ^{22}Na . The measured absolute gain was 0.55 keV per ADC count.

When the pixel front-end is programmed for negative polarity, the negative pulse at the output of the shaper is inverted by a polarity inverter amplifier and then connected to the peak and detect circuit which always detects the maximum amplitude of its input signal. In the case of positive polarity, the polarity inverter amplifier is just bypassed. Due to the additional inversion stage, the non-linearity and the noise of the pixel front-end at negative polarity settings increases as one can observe by comparing the two curves from Fig. 7 and Fig. 8 respectively.

By extrapolating with a linear fit from 0 to 50 keV the curves from Fig. 8, the mean values of the pedestal noise of 1.4 keV and 1.67 keV at FWHM were obtained for positive and negative settings respectively. The equivalent noise charge with CdTe detectors would be 133 e^- -RMS and 160 e^- -RMS for positive and negative polarity respectively. Note that the shaping stage effectively reduces the ENC of the pre-amplifier by e^- -RMS.

At 511 keV for the maximum gain of 1024 ADC counts for 550 keV, the resolution at FWHM of the pixels front-end has a mean value of 0.4% and 0.5% for positive polarity and negative polarity respectively.

C. Trigger Jitter

We characterized the trigger time-walk and the jitter of the discriminator of 80 pixels with external test pulses with variable amplitude and an external counter/TDC with 25 picoseconds resolution. The plot of the time-walk of the discriminator, obtained as the mean value of one thousand measurements per amplitude step, is shown in Fig. 9 for positive and negative polarity.

The jitter is defined as the time resolution (FWHM) of the time-walk measurements at every pulse amplitude. The results for positive and negative polarity are shown in Fig. 10. The measured trigger jitter in the energy range from 25 keV to 511 keV is below 10 ns. As expected, it follows a linear decreasing dependency with the energy due to the constant peak time of the preamplifier. The measured trigger jitter does not pose a limitation on the performance of a PET [9], since a coincidence time window of 20 ns is established for normal operation of the PET ring [14].

IV. TDC and Temperature Sensor Measurements

For every self-generated trigger, the ASIC digital controller provides to the external FPGA a data packet with the following twelve 10-bit words: the address of the triggered pixel, the value of the TDC corresponding to the time stamp of the trigger, the temperature, and the value of the ADC of the triggered pixel followed by energy of the eight neighboring channels. In the following sections, the characterization of the TDC and the temperature sensor in terms of sensitivity and resolution is described.

A. Integrated Time to Digital Converter

Fig. 11 shows the block diagram of the TDC. It consists of a switched current source connected to an integrating amplifier with 1.4 pF feedback capacitor and tunable feedback resistor that is digitized with a successive approximation register (SAR) ADC with 10 bit resolution. Note that the integration time is defined by the signal GATE PULSE, which is generated by the ASIC digital controller.

As shown, the pulse is activated when a trigger of the pixel matrix arrives to the TDC, and it ends with the following rising edge of a 10 MHz (100 ns period) clock. The output of the TDC is effectively the remaining time to the following clock of 10 MHz. Note that in such conditions the dynamic range of the integrating amplifier should be designed for 100 ns full range integration time.

The integrated TDC has been characterized with an external counter with 25 ps resolution that was used to measure indirectly the period of the gate pulse signal at every measurement. The measured current consumption of the TDC was 52 μA , from which 20 μA were consumed by the ADC, 30 μA by the operational amplifier, and 2 μA from the current reference and current mirrors. Fig 12 and Fig. 13 show the measured linearity and resolution of the TDC with 100 measurements per point. Note that the slope of the fitting indicates that the sensitivity of the TDC is 95.5 ps per ADC count approximately. The measured resolution at full width half maximum is 600 ps at full range, which is below the initial requirements of 1 ns resolution.

B. Integrated Temperature Sensor

The temperature sensor is based on the temperature dependency of the junction voltage of a P-N diode forward-biased with constant I_S current. The complete cell is based on a current DAC connected to a P-N diode and a 10-bit SAR ADC that digitizes the voltage at the anode.

The response of the sensor has been characterized in a temperature-controlled environment with a resolution of 0.1 degree. The measured current consumption was $24\ \mu\text{A}$ from which $20\ \mu\text{A}$ were consumed by the ADC and $4\ \mu\text{A}$ by the current DAC. A sensitivity of 0.4 degrees per ADC count was obtained. It is important to remark that with 1000 measurements per temperature point, the ADC value kept constant at the same ADC bin which indicates the noise is well below 1 ADC count.

V. First Spectroscopy Results

The 4×4 pixel matrix ROIC has been connected to a dedicated 4×4 pixelated CdTe detector via bump bonding technique as the final detector of 100 pixels will be connected to the 10×10 VIP-PIX ASIC [13]. The Schottky diode detector has a thickness of 2 mm and a pixel pitch of 1 mm that matches the pixel pitch of the ROIC. At -10°C , the detector was biased at $-1000\ \text{V}$, and the complete setup was continuously flushed by nitrogen gas to minimize the humidity level and thus reduce the leakage of the detector. The first spectroscopy of ^{57}Co obtained with the presented ROIC is shown in Fig. 14. The data presented are row without considering the charge sharing correction between adjacent pixels. The Gaussian-peak fit for energy peak at 122 keV shows a resolution of 3.6% at full width half maximum.

VI. Conclusions

We presented the performance of a 4×4 pixel readout ASIC with independent pixel front-end electronics, integrated TDC, temperature sensor, and digital controller. We have shown that this ASIC can achieve 1% FWHM for 511 keV, minimum threshold of 5 keV, fast trigger with time jitter below 10 nsec, and low power consumption in every pixel. Table II summarizes the measured performance of the pixel readout electronics, the time to digital converter, and the temperature sensor.

The successful results of the pixel readout electronics including the high resolution spectroscopy obtained for ^{57}Co , the measured linearity and time resolution of the TDC, and the sensitivity of the temperature sensor allow the integration of the complete matrix of 10×10 pixel VIP-PIX ASIC for medical imaging applications such as positron emission tomography scanners.

Acknowledgment

The authors would like to thank Thomas Moore for realizing most of the layouts of the presented ASIC, and David Fernández Bosman and Gerard Ariño Estrada for the measurements and analysis of the temperature sensor.

The research leading to these results was supported by the European Research Council under the European Union's Seventh Framework Programme (ERC Grant Agreement 250207, "VIP") and the Spanish MINECO under the Severo Ochoa excellence program (Grant SO-2012-0234).

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Fig. 1.

Common architecture of high energy resolution single channel front-end electronics.

Fig. 2.

Description of the biasing of the CdTe detector and the interaction of gamma-ray photons at different distances of the electrodes of the detector.

Fig. 3.
Block diagram of the pixel front-end electronics.

Fig. 4.
Layout and block distribution of the implemented pixel.

Fig. 5.
Microphotography of the fabricated 4×4 pixel readout ASIC.

Fig. 6. Distribution of minimum threshold for 160 pixels at 1.27 mV/keV preamplifier gain and 60 μ s baseline restore time.

Fig. 7.

Measured linearity of 80 pixels front-end at 1.27 mV/keV preamplifier gain, 60 μ s baseline preamplifier restore time, and 10 μ s shaper peak time for positive polarity (filled circle) and negative polarity (empty circle).

Fig. 8. Measured energy resolution of 80 pixels front-end at 1.27 mV/keV preamplifier gain, 60 μ s baseline preamplifier restore time, and 10 μ s shaper peak time for positive polarity (filled circle) and negative polarity (empty circle).

Fig. 9. Measured time-walk of the discriminator of 80 pixels for positive polarity (filled circle) and negative polarity (empty circle) at 1.27 mV/keV preamplifier gain.

Fig. 10. Measured jitter of the trigger of 80 pixels versus input energy for positive polarity (filled circle) and negative polarity (empty circle) at 1.27 mV/keV preamplifier gain.

Fig. 11.
Block diagram of the TDC.

Fig. 12.
Measured linearity of the TDC.

Fig. 13.
Measured resolution at full width half maximum of the TDC.

Fig. 14.
Spectroscopy of ^{57}Co obtained with one pixel of the presented 16-channel ROIC.

TABLE I**Specifications of CdTe Detector and Pixel Electronics**

Specification	Value
CdTe detector size	10×10×2 mm ³
Voxel size	1×1×2 mm ³
Detector DC bias voltage	−2000 V
Detector leakage current per pixel	60 pA (up to few nA)
Electron/Hole drift time	17 ns/190 ns
Pixel capacitance	100 fF
ENC of the Energy resolution	150 e [−] RMS
Minimum trigger / Equivalent Noise	25 keV / 1000 e [−] RMS
Maximum Jitter of time stamp	10 ns
Maximum power consumption	200 μW/pixel

TABLE IIPerformance of the 4×4 Pixel Array, TDC, and Temperature Sensor of the Presented ASIC

Input charge maximum range	$\pm 17 \text{ fC}$ to $\pm 70 \text{ fC}$
Gain for both polarities	10, 16, 20, and 40 mV/fC
Detector leakage compensation	dynamic up to 4 nA /pixel
Minimum threshold (from 80 pixels)	5.3 keV
ENC @ 40 mV/fC (positive polarity)	$133 \text{ e}^- \text{ RMS}$
ENC @ 40 mV/fC (negative polarity)	$160 \text{ e}^- \text{ RMS}$
Discriminator jitter	$< 10 \text{ ns}$ for $E > 25 \text{ keV}$
Supply Voltage	2.5 V
Power consumption	$190 \mu\text{W} / \text{pixel}$
TDC resolution	$95.5 \text{ ps} / \text{ADC count}$
TDC precision FWHM	600 ps
TDC power consumption	$130 \mu\text{W}$
Temperature sensor sensitivity	$0.4 \text{ Celsius degrees}$
Temperature sensor consumption	$60 \mu\text{W}$