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Power Amplifier Linearizer for High Frequency Medical Ultrasound Applications

Hojong Choi^{1,*}, Hayong Jung², and K. Kirk Shung²

¹Department of Medical IT Convergence Engineering, Kumoh National Institute of Technology, Gumi, Gyeongbuk, 730-701, South Korea

²NIH Transducer Resource Center and Department of Biomedical Engineering, University of Southern California, Los Angeles, CA, USA, 90089

Abstract

Power amplifiers (PAs) are used to produce high-voltage excitation signals to drive ultrasonic transducers. A larger dynamic range of linear PAs allows higher contrast resolution, a highly desirable characteristic in ultrasonic imaging. The linearity of PAs can be improved by reducing the nonlinear harmonic distortion components of high-voltage output signals. In this paper, a linearizer circuit is proposed to reduce output signal harmonics when working in conjunction with a PA. The PA performance with and without the linearizer was measured by comparing the output power 1-dB compression point (OP_{1dB}), and the second- and third-order harmonic distortions (HD2 and HD3, respectively). The results show that the PA with the linearizer circuit had higher OP_{1dB} (31.7 dB) and lower HD2 (−61.0 dB) and HD3 (−42.7 dB) compared to those of the PA alone (OP_{1dB} (27.1 dB), HD2 (−38.2 dB), and HD3 (−36.8 dB)) at 140 MHz. A pulse-echo measurement was also performed to further evaluate the capability of the linearizer circuit. The HD2 of the echo signal received by the transducer using a PA with the linearizer (−24.8 dB) was lower than that obtained for the PA alone (−16.6 dB). The linearizer circuit is capable of improving the linearity performance of PA by lowering harmonic distortions.

Keywords

Power amplifier; Linearizer; Ultrasonic transducer

1. Introduction

PAs in an ultrasound system drive the ultrasonic transducers. Therefore, PAs are required to have good linearity and the widest bandwidth possible for optimal transducer performance. Designing linear PAs to operate at high frequencies is very challenging since the parasitic impedances of their electronic components become more dominant at higher frequencies [1,2]. Furthermore, the simulation model of the power MOSFET device, which is the main component of a PA, is inaccurate for high-voltage operation [3-5].

*Corresponding author: Hojong Choi, Address: Department of Medical IT Convergence Engineering, Daehak-ro 61, Gumi-citi, Gyeongbuk, 730-071, South Korea, Tel.: 82-54-478-7789, Fax: 82-54-478-7859, hojongch@kumoh.ac.kr.

As the input power of the PA increases, the output power of the PA should increase linearly up to a certain point, called the saturation point, after which the output power no longer linearly increases along with the input power. This saturation point phenomenon is generally caused by unwanted harmonic distortion signals reaching levels that are comparable to those of the fundamental signal generated by the PA, making further amplification impossible [6]. A linearizer circuit can be used to compensate for the harmonic effects of the PA, increasing the dynamic range (saturation point) of the PA [7]. The PA can amplify signals without further distortion at the higher saturation point, as shown in Fig. 1.

In ultrasound systems, PAs normally produce high-voltage output waveforms with harmonic distortion components when the amplifier gain is saturated, thus generating unwanted side lobes [1]. These side lobes produce image artifacts that deteriorate contrast resolution and reduce the estimation of the accuracy of the ultrasonic beam focal zone in therapeutic ultrasound applications [8]. An approach that uses a look-up table algorithm was developed to reduce the harmonic distortion of the output signals generated by a PA in low-frequency ultrasound applications [9]. However, this approach is complex and may not be feasible for high frequency imaging array systems due to cost, complexity, and size limitations. This method requires the use of high-quality analog-to-digital converters and digital-to-analog converters with high-speed digital signal processing algorithms. In the present study, a simpler, smaller, and less expensive linearizer circuit is proposed to reduce harmonic components for PAs. Similar linearizer techniques have been used extensively in RF wireless communication applications to improve the linearity performance of PAs [10-12]. However, none of these approaches have been used to improve the linearity performance of PAs in applications that use high frequency ultrasound systems. Therefore, we have developed a new linearizer circuit that can minimize certain multiple-order (e.g., second and third) PA harmonic distortions.

2. Methods

2.1. System-level description of linearizer and PA

The linearizer circuit was designed to suppress the unwanted harmonic distortions of a PA. The linearizer is placed prior to the PA to reduce the harmonic distortion of its output signals [13]. A block diagram of the linearizer and PA is shown in Fig. 2(a). The circuit diagrams of the linearizer and PA are shown in Figs. 2(b) and (c), respectively. The linearizer circuit is composed of a passive resistor, inductor, and capacitor (RLC) circuit, a power MOSFET device (TR_0), and a controllable DC voltage port (V_{dc0}). The PA topology is that for a typical one-stage common-source class A type linear PA. For a class A PA, controlling the gate and drain voltages (V_{dc1} and V_{dc2}) ensures that the PA is always ON, resulting in significant power consumption and heat problems, especially for a mismatched load. Therefore, impedance matching is critical for all class A PA designs [7]. To address this, a PA that employs an RLC matching network at the input and output port is selected.

In a two-layer printed circuit board, the linearizer circuit was implemented using passive RLC components with a power MOSFET device (BSS123, Diode Inc., Plano, TX). The PA was implemented using a power MOSFET device (PD57006-E, STMicroelectronics Inc., Geneva, Switzerland) and RLC components. In addition, all the RLC components were

selected to tolerate high-voltage operation (> 100 V). The power rating of the resistor, maximum current of the inductor, and maximum voltage of the capacitor were 15 W, 1 A and 100 V, respectively. The measured gain, center frequency, and -3 dB bandwidth of the PA were 15 dB, 200 MHz, and 240 MHz, respectively.

2.2. Component selection of linearizer

The linearizer equivalent circuit model (Fig. 3(b)) was constructed based on the large-signal power MOSFET equivalent circuit model (Fig. 3(a)) to elucidate the operating mechanism of the linearizer circuit [14]. As shown in Fig. 2(b), the linearizer circuit, consisting of an RLC network (R_0 , C_0 , and L_0) with a power MOSFET, behaves as a type of feedback loop network, which generates specific harmonic signals that cancel the nonlinear harmonic distortion signals of the PA. In the linearizer circuit, the resistor (R_0) works as a bias-feed component through the DC power supply. The value of the resistor was selected to avoid noise figure degradation [7]. The external capacitor (C_0) contributes the most towards the total capacitance. Additionally, the MOSFET parasitic gate-source, drain-source, and gate-drain capacitances (C_{GS} , C_{DS} , and C_{GD} , respectively) generate harmonic signals at each power level. The large inductor (L_0) value serves to further avoid large-signal gain degradation as an RF choke [15,16]. As shown in Fig. 3(b), the drain-source current (I_D) of the transistor is controlled by the gate-source DC bias voltage (V_{dc0}) across the RLC network. Therefore, adjusting the DC bias voltage changes the MOSFET transconductance value (G_m) of the drain-source current.

In order to determine proper bias conditions for the power MOSFET, the voltage variance characteristics of the parasitic resistance and capacitances as well as the transconductances need to be determined since each component in the linearizer should work in a larger linear range [11]. Figure 4 shows the transconductance values obtained using a circuit simulator (Agilent ADS, Agilent Technologies Inc., Santa Clara, CA) and impedance parameter values obtained from a datasheet (BSS123, Diode Inc., Plano, TX) [17]. As the input power increases, the transconductance (G_m) works as a variable resistor in a larger linear range, as shown in Fig. 4. According to the datasheet (BSS123), the drain-source resistance (R_{DS}) also works as a linear resistor in a wider current range when the gate-source voltage (V_{GS}) rises above 3 V DC [17]. The gate-source (C_{GS}), gate-drain (C_{GD}), and drain-source (C_{DS}) capacitances become saturated when the drain-source voltage approaches 5 V DC [17]. Therefore, the DC bias voltage (V_{dc0}) of the linearizer is selected to be higher than 3 V. The effects of the MOSFET parameters and RLC network component values on the linearizer characteristics depend on the bias conditions.

2.3. Design guidelines for linearizer

Figure 5 shows the operational mechanism of the gain deviation vs. input or output power of the linearizer and PA. Since the linearizer circuit must have minimal gain deviation throughout a wide range of the input power levels, the PA with a linearizer could have lower gain deviation within a wider input or output power range, resulting in higher power amplification of the amplifier without further distortion [11]. Therefore, the gain deviation vs. input power of the linearizer must be measured in order to properly select the linearizer components.

Figures 6(a) and (b) show the linearizer schematic and its experimental arrangement. Figures 6(c)-(e) show the measurement results of the gain-deviation vs. input power obtained for various linearizer component values (R_0 , C_0 , and L_0). A power supply (E3630A, Agilent Technologies Inc.) provided the voltage to bias the linearizer. A continuous sine wave from a function generator (AFG2020, Tektronix, Beaverton, OR) was also provided into the linearizer. The gain deviation was calculated based on the measured data displayed on the oscilloscope (TDS5052, Tektronix).

Table 1 summarizes the gain deviation points at an input power level of 18 dB_m for the linearizer components. When a 500- Ω resistor, 2.2- μ H inductor, and 300-pF capacitor were selected as the linearizer components, the smallest gain deviation was achieved throughout a wide range of the input power levels.

The gain deviation vs. input power of the linearizer circuit was plotted for various bias voltage conditions to determine the optimal bias voltage in the linearizer. As shown in Fig. 6(f), a 4-V DC bias from the linearizer circuit gives the lowest gain deviation when the input power is increased. The 6-V DC bias from the linearizer also provides lower gain deviation before 25 dB_m input power level compared to those for 3- and 5-V DC biases. It is clear that the gain deviation of the PA at 4- and 6-V DC bias could be further minimized at higher output power levels.

2.4. Linearizer model analysis

The parasitic capacitances of the MOSFET, resistor ($R_0 = 500 \Omega$), capacitor ($C_0 = 300$ pF), and inductor ($L_0 = 2.2 \mu$ H) affect linearizer performance. It can be safely concluded that the drain-source current (I_D) of the power MOSFET (TR_0) is controlled by different gate-source DC bias voltages (V_{dc0}) across the resistor (R_0) and parasitic capacitances. With a properly selected bias voltage, the linearizer circuit generates appropriate harmonics to compensate for the harmonics of the PA. An analysis was conducted to predict the behavior of the circuit to select the values of the individual circuit components[13]. Taylor series expansion was used to predict the output voltages of the linearizer and PA. The transfer function of the linearizer output voltage (V_i) can be characterized as follows [13]:

$$V_i = V_{in} \cos(\omega t) + b_2 V_{in}^2 \cos^2(\omega t) + b_3 V_{in}^3 \cos^3(\omega t) \quad (1)$$

where V_{in} is the original input of the linearizer, and b_2 and b_3 are the second- and third-order harmonic coefficients of the linearizer output, respectively.

The transfer function of the PA output voltage (V_o) is given by:

$$V_o = a_1 V_i(\omega t) - a_2 V_i^2(\omega t) - a_3 V_i^3(\omega t) \quad (2)$$

where a_1 , a_2 , and a_3 are the fundamental, second-, and third-order coefficients of the PA output.

Therefore, the output voltage of the linearizer followed by the PA can be represented as:

$$V_o = \frac{a_1 b_2 - a_2}{2} + (a_1 - \frac{3}{4}(a_3 - a_1 b_3 + \frac{a_1 b_2}{2})) V_{in} \cos(wt) - \frac{1}{2}(a_2 - a_1 b_2) V_{in} \cos(2wt) - \frac{1}{4}(a_3 - a_1 b_3 - 2a_2 b_2) V_{in} \cos(3wt) + \dots \quad (3)$$

The first and second terms represent DC offset and amplitude modulation of the original gain of the PA with the linearizer, respectively. The third and fourth terms represent the second- and third-order harmonic distortions of the final output of the PA with the linearizer, respectively. In order to minimize the second-order harmonic distortion for the output voltage of the PA with the linearizer, the second-order harmonic term of the linearizer output is equal to the PA's second-order harmonic term divided by the fundamental coefficient term of the PA. The equation that represents this relationship is:

$$b_2 = \frac{a_2}{a_1} \quad (4)$$

Furthermore, the equation of the third-order harmonic distortion cancellation of the linearizer is given by:

$$b_3 = \frac{2a_2 b_2 + a_3}{a_1} \quad (5)$$

This equation also indicates that the third-order harmonic distortion term of the linearizer circuit (b_3) is related to the second-order harmonic distortion term (b_2).

3. Results

3.1. Experimental verification of linearizer model

Figure 7(a) shows the measurement setup with a spectrum analyzer for the linearizer and PA circuits. A power supply (E3630A, Agilent Technologies Inc.) provided the voltage to activate the linearizer and another power supply (382285, Extech Instrument, Nashua, NH) provided the DC bias voltage to the PA. A continuous sine wave from a function generator (AFG2020, Tektronix) fed the linearizer and PA, respectively. The harmonic distortion components of the output signal were displayed on the spectrum analyzer (ESA-E, Agilent Technologies Inc.). Figure 7(b) shows original 140-MHz fundamental and harmonic output signals of the PA. Figures 7(c) and (d) show harmonic output signals of the linearizer with 4- and 6-V DC biases, respectively.

The transfer functions of the linearizer and PA from Eqs. (1) and (2) indicate that the linearizer and PA have fundamental amplitude and several harmonic distortion terms [13]. From the fundamental amplitudes and the second- and third-order harmonic distortion coefficients (HD2 and HD3) generated by the PA and linearizer, respectively from Figs. 7(b)-(d), the harmonic terms (a_1 , a_2 , a_3 , b_2 , and b_3) were extracted. The differences between these terms (b_2 and a_2/a_1 or b_3 and $(2a_2b_2 + a_3)/a_1$) from Eqs. (4) and (5) were calculated to verify that these terms are close to 0 dB. Table 2 shows the extracted harmonic terms and their calculated differences. In order to find the optimal biasing point, the same mathematical procedure was used to calculate these coefficient values for various DC bias voltages applied to the linearizer.

Figures 8(a) and (b) show the calculated differences of harmonic components for various different DC bias voltages in the linearizer. As described in the previous section, there is a point where the second-order harmonic distortion of the PA with the linearizer output is minimized. Thus, b_2 is the closest to the a_2/a_1 term from Eq. (4). In Fig. 8(a), the difference between b_2 and a_2/a_1 was minimized when a 4-V DC bias voltage was applied to the linearizer. As shown in Fig. 8(b), the second-order harmonic distortion was reduced ($HD_2 = -61.0$ dB) when a 4-V DC bias voltage was applied to the linearizer. The third-order harmonic distortion of the PA with the linearizer output was minimized at another point. Figure 8(c) shows how close b_3 is to $(2a_2b_2 + a_3)/a_1$ from Eq. (5). At a 6-V DC bias, the difference between these two terms is relatively low (-2.3 dB at 4 V DC vs. 2.1 dB at 6 V DC). In Fig. 8(d), the third-order harmonic distortion is further reduced ($HD_3 = -47.1$ dB). However, the second-order harmonic distortion ($HD_2 = -39.1$ dB) could not be further reduced when a 6-V DC bias voltage was applied.

3.2. Performance measurement of PA with linearizer

In Fig. 9(a), a DC power supply (E3630A) provides the voltage to activate the linearizer and another power supply (382285) provides the DC bias voltage to the PA. A continuous sine wave from the function generator (SG384, Stanford Research Systems, Sunnyvale, CA) served as the input to the system. The peak-to-peak output voltages of the waveform were displayed on an oscilloscope (TDS5052, Tektronix) and measured to calculate the power gain and gain-deviation of the PA with and without the linearizer. In order to demonstrate the improved linearity performance of the PA, the gain variance vs. output power of the PA with and without the linearizer is shown in Fig. 9(b). The gain deviation of the PA is clearly reduced with the help of the linearizer.

The output power 1-dB compression point (OP_{1dB}) indicates where the gain of the amplifier output power is 1 dB below the ideal linear gain [6]. This point is normally defined as the limitation index of the PA dynamic range. The OP_{1dB} of the PA with and without the linearizer was measured since the linearity can be improved by reducing harmonic distortion components of the output signals of a PA. In order to show the linearity performance of the PA with and without the linearizer, graphs of the gain and output power vs. input power at 140 MHz are plotted in Fig. 9(c). In the figure, the OIP_{1dB} of the PA with the linearizer circuit (31.7 dB) is higher than that of the PA alone (27.1 dB). The linearizer bias voltage was selected to maximize the OP_{1dB} for 140-, 190-, and 210-MHz input signals. In Fig. 9(d), the OP_{1dB} values of the PA with and without the linearizer for fundamental frequencies of 140, 190, and 210 MHz are shown. At 190 MHz, the PA with the linearizer has a higher OP_{1dB} (34.2 dB) than that of the PA alone (32.9 dB).

3.3. Pulse-echo measurement

Pulse-echo measurements (Fig. 10(a)) were made using a 140-MHz transducer to highlight the improved linearity of the PA with the linearizer vs. the PA alone. A 140-MHz single-element LiNbO_3 transducer was fabricated in our laboratory for this test. The aperture size and focal distance of this transducer are 1 and 1.5 mm, respectively. The transducer was placed in a de-ionized water tank with the aperture positioned 1.5 mm from the quartz target surface. A three-cycle sine wave signal from the function generator fed the linearizer and

PA, the output of which was then delivered to the transducer through an expander (DEX-3, Matec Instruments, Northborough, MA). The received echo signals generated by the transducer passed through the limiter (DL-1, Matec Instruments) and a preamplifier (AU-1114, MITEQ, Hauppauge, NY) before being displayed on the oscilloscope (LC534, Lecroy, Chestnut Ridge, NY) and recorded using a LabVIEW program. The minimum detection sensitivity, bit resolution, and maximum sampling frequency of the oscilloscope were 5 mV, 6 bits, and 1 GHz, respectively. The echo data were plotted in the frequency domain using the fast Fourier transform in a MATLAB program. Figure 10(b) shows the comparison of the echo power spectrum data of the 140-MHz ultrasonic transducer using the PA with and without the linearizer circuit. HD2 of the echo signal for the PA with the linearizer (HD2 = -24.8 dB) was lower than that for the PA alone (HD2 = -16.6 dB).

4. Discussion

While computer simulation results can be regarded to be accurate within a 5-dB range, analyzing canceling linearization systems requires sub-decibel accuracy, making these simulations inadequate for linearizer circuit design [6,18]. In addition, the power transistor model library in the computer simulation is not very accurate for high-voltage distortion analysis [6]. Therefore, the linearizer technique that supports the PA working at high frequency and high voltage operation was verified using characterization data.

The measured gain deviation vs. power curve of the linearizer could determine to properly select the certain bias voltage and components in the linearizer. The results demonstrate that the bias voltage and components in the linearizer affect performance. According to the transfer function of the PA with the linearizer, the linearizer circuit needs to be properly biased in order to generate harmonic canceling points for the PA harmonic signals. The second- and third-order harmonic distortions of the PA with the linearizer are minimized at different points. To determine which harmonic distortion components are suppressed, a characteristic output transfer function of the PA with the linearizer was derived to determine the conditions for effective harmonic cancellation.

In a linear system, as the input power increases, the output power should increase up to a point, called the saturation point (OP_{1dB}). The measured saturation points demonstrate that the gain deviation of the PA with proper component values and biasing conditions is further minimized with the help of the linearizer at higher output power levels.

For small apertures, higher frequency (> 15 MHz) transducers usually have lower sensitivity than that of lower-frequency transducers [19]. Since high-frequency transducer performance is highly dependent on the PA dynamic range, a linear PA is desirable for ultrasound electronics. Therefore, pulse-echo measurements using a high frequency transducer were performed in order to show the improved performance of the PA with the linearizer. PAs must be capable of generating higher-voltage signals in order to obtain echo signals with sufficient amplitude. The results demonstrate that the addition of the linearizer circuit improves PA performance for high frequency medical ultrasound transducer applications.

5. Conclusion

A linearizer circuit for PAs was proposed for ultrasound transducer applications. The measurement results show that adding the linearizer circuit produces a higher $OP1_{dB}$ (31.7 dB) than that of the PA alone (27.1 dB) at 140 MHz. The linearizer circuit also enhances the linearity of the PA by lowering the second- and third-order harmonic distortion components ($HD2 = -38.2$ to -61.0 dB and $HD3 = -36.8$ to -42.7 dB at 140 MHz) when a 4-V DC bias voltage is applied to the linearizer. The second-order harmonic distortion component of the echo signal received by the 140-MHz single-element transducer using the PA with the linearizer (-24.8 dB) was lower than that for the PA alone (-16.6 dB). This simple and inexpensive linearizer circuit design is suitable for use in high-frequency medical ultrasound array applications such as small animal or cell imaging systems that require a large PA dynamic range.

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Figure 1.
Description of operational mechanism of linearizer and PA.

Figure 2.
 (a) Block diagram of linearizer and PA, (b) linearizer circuit diagram, and (c) PA circuit diagram.

Figure 3. Large-signal equivalent circuits model of (a) power MOSFET and (b) linearizer.

Figure 4.

Simulated transconductance value (G_m) vs. drain-source current (I_{DS}) at gate-source voltage (V_{GS}) variance of MOSFET.

Figure 5. Operating mechanism of gain deviation vs. input or output power graph of linearizer and PA.

Figure 6.

(a) Linearizer schematic and (b) its experimental arrangement. Gain deviation vs. input power with various (c) capacitor values, (d) inductor values, (e) resistor values, and (f) DC bias voltages (3, 4, 5, and 6 V DC).

Figure 7.

(a) Measurement setup with spectrum analyzer for linearizer and PA, (b) fundamental and harmonic output signals of PA when 140-MHz sine waveform was applied, and harmonic output signals of linearizer when 140-MHz sine waveform with (c) 4- and (d) 6-V DC bias voltage was applied to linearizer.

Figure 8. Calculated differences of (a) second- and (b) third-order harmonic distortion component vs. DC bias voltage. Harmonic distortion graphs of PA with linearizer with (c) 4- and (d) 6-V DC bias voltage.

Figure 9.

(a) Measurement arrangement of linearizer and PA and (b) measured gain deviation plot for PA only (black dashed line) and PA + linearizer with 4-V (red solid line) and 6-V (blue dash-dot line) DC bias at 140 MHz fundamental frequency, (c) measured output power vs. input power of PA with (black dash-dot lines) and (red solid lines) without linearizer, and (d) OP_{1dB} vs. frequency of PA with (red solid lines) and without (black dash-dot lines) linearizer circuit.

Figure 10.

(a) Schematic diagram of pulse-echo measurement setup and (b) echo spectrum data comparison of 140-MHz single-element transducer using PA with (red solid line) and without linearizer (black short dash-dot line).

Table 1

Gain deviation data of linearizer at 18-dBm input power level and 4-V DC bias voltage.

Resistor (Ω)	300	500	1000
Gain deviation	0.28 dB	-0.06 dB	-0.32 dB
Inductor (μ H)	1.1	1.5	2.2
Gain deviation	0.84 dB	-0.98 dB	-0.06 dB
Capacitor (pF)	100	300	470
Gain deviation	-0.28 dB	-0.06 dB	-1.29 dB

Table 2

Calculated differences of harmonic terms of PA and linearizer.

V_{DC}	a_1	a_2	a_3	b_2	b_3	Calculated terms		
						a_2/a_1 (dB)	b_2 (dB)	$ b_2 $ (dB) - $ a_2/a_1 $ (dB)
4 V	2.14	0.00327	0.004037	0.00295	0.000145	-56.306	-50.603	-5.703
						$(2a_2b_2+a_3)/a_1$ (dB)	b_3 (dB)	$ b_3 $ (dB) - $ (2a_2b_2+a_3)/a_1 $ (dB)
						-54.445	-56.772	-2.327
6 V	2.14	0.00327	0.004037	0.00719	0.00104	a_2/a_1 (dB)	b_2 (dB)	$ b_2 $ (dB) - $ a_2/a_1 $ (dB)
						-56.306	-42.4006	-13.906
						$(2a_2b_2+a_3)/a_1$ (dB)	b_3 (dB)	$ b_3 $ (dB) - $ (2a_2b_2+a_3)/a_1 $ (dB)
						-54.3809	-52.236	2.144