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Prototype AEGIS: A Pixel-Array Readout Circuit for Gamma-Ray Imaging

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Abstract

Semiconductor detector arrays made of CdTe/CdZnTe are expected to be the main components of future high-performance, clinical nuclear medicine imaging systems. Such systems will require small pixel-pitch and much larger numbers of pixels than are available in current semiconductor-detector cameras. We describe the motivation for developing a new readout integrated circuit, AEGIS, for use in hybrid semiconductor detector arrays, that may help spur the development of future cameras. A basic design for AEGIS is presented together with results of an HSPICETM simulation of the performance of its unit cell. AEGIS will have a shaper-amplifier unit cell and neighbor pixel readout. Other features include the use of a single input power line with other biases generated on-board, a control register that allows digital control of all thresholds and chip configurations and an output approach that is compatible with list-mode data acquisition. An 8×8 prototype version of AEGIS is currently under development; the full AEGIS will be a 64×64 array with 300 μm pitch.

Keywords

CdZnTe; CdTe; CZT; semiconductor detector; hybrid detector; semiconductor camera; nuclear medicine; readout integrated circuit; medical imaging

1. INTRODUCTION

This report describes a collaborative effort by Augustine Engineering and researchers at the University of Arizona Center for Gamma-Ray Imaging to develop a new readout ASIC (Application Specific Integrated Circuit) for gamma-ray imaging in nuclear medicine and biomedical imaging. The readout ASIC will have a shaper-amplifier unit cell, will feature neighboring pixel readout and will incorporate advanced design features such as on-board generation of bias voltages and digital control of configuration and thresholds. An 8×8 prototype of the AEGIS (Augustine Engineering Gamma-ray Imaging and Spectroscopy) readout is currently under design; the full AEGIS will be a 64×64 array with 300 μm pixel pitch. Here we present the motivation for developing a new readout circuit and our reasons for believing that availability of a better readout ASIC could become the critical factor driving the development of a new generation of CdTe/CdZnTe semiconductor detector

cameras. We will conclude with a general description of the AEGIS design and present some results from HSPICE™ simulations of performance of the AEGIS unit cell.

2. SEMICONDUCTOR DETECTORS

Semiconductor detectors such as CdZnTe and CdTe have the potential to dramatically improve the performance of nuclear medicine imaging systems, particularly for SPECT. Slabs of such semiconductor material can be partitioned into arrays having large numbers of pixels and small pixel size, which allows high spatial resolution. We will show that the critical determinant that leads to improved performance is that the detector have *both* small pixel size and a large number of pixels. Semiconductor detectors such as CdZnTe/CdTe also operate at room temperature and potentially can have superb energy resolution. However, despite a decade of development, CdZnTe has not yet had a major impact on nuclear medicine imaging. There are a number of reasons for this: the poor quality of early CdZnTe with numerous dead regions due to grain boundaries and inclusions, the high cost of CdZnTe/CdTe and the limited performance of available readout electronics which is not capable of handling very large numbers of pixels. More recently, progress has been made in all of these areas. Producers of CdZnTe have incrementally improved performance, and large detector wafers ($\sim 10 \text{ cm}^2$) are now available, albeit with the use of careful mapping and selection techniques.^{1,2} More recently, Yinnel Tech³ (CdZnTe) and Acrorad⁴ (CdTe) have developed seeded growth techniques that produce ingots that are mostly one single crystal with potentially high detector uniformity and improved yield of large detector substrates. The cost of CdZnTe/CdTe has slowly come down, but these materials are still very expensive compared to scintillators. A significant number of small prototype semiconductor cameras have now been developed or are under development⁵⁻¹⁷ (see Table 1); a few of these are even commercially available. Unfortunately, as we shall see in the next section, none of these cameras has sufficient performance improvement over existing scintillation cameras to fully demonstrate the advantages of semiconductor detectors; most have moderate spatial resolution and none have very high SpBW.

3. SPACE BANDWIDTH PRODUCT

Barrett¹⁸ has pointed out the importance of high space bandwidth product (SpBW) for nuclear medicine imaging, specifically for SPECT imaging. Space bandwidth product is defined simply as the number of resolvable imaging elements in the detector system (i.e. the total detector area divided by area of the spatial resolution element, if the resolution is spatially constant). In a pixelated system, without sub-pixel resolution, this is just the number of pixels. As an example of the importance of SpBW, consider the case of multiple-pinhole SPECT, where it is possible to gain sensitivity without sacrificing final image resolution, provided that we can improve detector performance. If we develop a detector with improved spatial resolution, we can use it with a smaller pinhole or finer collimator to improve the final image resolution at the expense of sensitivity, but we can also use it to improve sensitivity. To do so, we move the detector closer to the pinhole, thereby reducing the magnification and leaving room for more pinholes (see Figure 1). Even though smaller pinholes are then needed for the same final resolution, the number of pinholes increases faster than the opening area of each decreases, so the overall sensitivity is actually increased.

Rogulski, *et al.*¹⁹ demonstrated this effect in simulations of brain imaging using multiple pinholes and high-resolution, high SpBW detector configurations. Similar conclusions should result for the case of other types of collimators.

Most modern gamma cameras for use in planar imaging and SPECT make use of a slab of NaI (Tl) scintillator, viewed by an array of photomultiplier tubes, and a position estimation technique developed by Anger.²⁰ Anger camera development appears to be approaching a limit of spatial resolution in the range 2.5–3.0 mm. Large format gamma cameras typically have even poorer spatial resolution, 3.5–4.0 mm. At fixed spatial resolution, space bandwidth product can still be increased by increasing the total detector area, but modern multi-headed SPECT cameras may be approaching the practical limits of this strategy. Typical space bandwidth product for a large format gamma camera is 16,000; multiheaded cameras typically have SpBW ~ 32,000. The best chance of improving the performance of SPECT cameras must thus come in improving spatial resolution while continuing the coverage of a large area.

An alternative to conventional scintillation cameras is a reticulated scintillator array (discrete pixels) read out by either an array of silicon photodiodes or a position sensitive photomultiplier tube (PSPMT). The Digirad 2020tc²¹ (it has the same name as their discontinued CdZnTe camera) has pixel pitch of 3.25 mm and SpBW = 4096. Gamma Medica's PSPMT-LUMAGEM²² has pixel pitch of 2.2 mm and SpBW = 3364. Although these cameras have better spatial resolution than conventional gamma cameras, their SpBW's are still quite limited.

A number of research groups and companies are investigating semiconductor detector arrays for use in clinical imaging cameras. Table 1 gives a list of such systems and their properties; most are developmental prototypes, but a few are available commercially. The sheer number of such systems indicates an active interest in developing semiconductor devices as alternatives to scintillation cameras; all use CdZnTe or CdTe. These cameras all have small detector areas (10–400 cm²) as compared to a large format scintillation camera which typically has ~ 2000 cm² of detector area. With the exception of the Arizona and AJAT devices, all the semiconductor cameras in Table 1 have spatial resolution (here pixel pitch) similar to, or only slightly better than scintillation cameras. All have modest SpBW; none has SpBW larger than a conventional large-format scintillation camera. It is clear that existing semiconductor-detector cameras do not yet have sufficiently improved spatial resolution or high enough SpBW that we should expect substantially improved imaging performance over conventional systems.

However, the cameras of Table 1 represent very important milestones, nevertheless. First, camera developers have gained valuable experience adapting CdTe/CdZnTe detectors to real clinical imaging systems, and this was undoubtedly a major motivation for building such systems. Second, many of these cameras are designed for niche applications that take advantage of some of the strengths of semiconductor detectors. For instance, high spatial resolution is important for small-animal imaging applications,^{14,15} compactness is important for imaging probes^{10,12,17} and semiconductor detector arrays have good response near the edges which is useful for mammoscintigraphy.^{8,13,16} A niche is a good place to grow.

However, the importance of scaling up the size of semiconductor detector arrays for use in larger clinical systems appears to be recognized by those developing semiconductor detector cameras.

Unfortunately, the electronics approaches used for most of the cameras of Table 1 is not conducive to scaling up. Discrete circuit components, printed circuit boards and small ICs with ~ 100 channels are common in these systems. A better approach is that of the hybrid semiconductor detector array as is used at the University of Arizona¹⁴ and by Oy Ajat¹² (see Table 1). The detector is typically a single slab of CdTe or CdZnTe with a two-dimensional array of pixel electrodes on one surface. It is relatively easy to make large numbers of pixels (high SpBW) and small pixel sizes using photolithography. Small pixel sizes together with larger detector thicknesses favor a strong “small-pixel effect”²³ which results in a good photopeak fraction and a better energy resolution. The pixels of the detector array are electrically connected to matching pixel circuitry on a readout integrated circuit via an interconnection technique such as indium bump bonding or flip-chip solder bump bonding. It is also possible to use a fanout board or interposer board²⁴ between the detector array and readout ASIC when these have different pixel pitch. The detector array and readout together are called a hybrid semiconductor detector array, and hybrids can be used as the basic building blocks of larger imaging systems. The University of Arizona 64×64 CdZnTe hybrid detector array is shown in Figure 2; it has been used for a number of small-animal SPECT imaging systems developed at the Center for Gamma-Ray Imaging.^{25,15}

It is our belief that an improved readout ASIC and resulting hybrid semiconductor detector arrays could be an important impetus to constructing the next generation of CdTe/CdZnTe cameras; the resulting scalability would favor the development of high-resolution, high SpBW clinical nuclear medicine cameras.

Other groups are investigating hybrid detector arrays for nuclear medicine imaging applications. Oy AJAT in Finland makes readouts and hybrid detector arrays of both the reset-gated-integrator type and shaper-amplifier arrays.¹² The European Medipix consortium is an association of research groups that have pooled resources to develop readout ASICs for medical imaging such as Medipix-2.²⁶

4. READOUT APPROACH

There are many types of circuits that could be used to read out arrays of x-ray/gamma-ray detectors.²⁷ In practice, two approaches are commonly used and both are viable: the reset-gated integrator (Figure 3) and the shaper amplifier (Figure 4).

In the case of the reset gated integrator (Figure 3), the pixel circuitry integrates the leakage current in each pixel for a fixed period of time and then is reset. The interaction of an x-ray or gamma ray in the pixel results in additional charge transport and a higher signal for that integration (frame). The clocking is usually controlled by external circuitry and large pixel arrays of the reset-gated integrator type are usually read out in a raster pattern. For large arrays of thousands of pixels, frame times of milliseconds are typical. Reset gated integrators are the circuit of choice for semiconductor-detector fluoroscopy systems because the signal response after subtraction of the integrated leakage is directly proportional to the

energy fluence in that pixel. This circuit also works well for photon-counting applications as well, as long as the counting rates are kept low enough that pileup is negligible.²⁸ The University of Arizona 64×64 hybrid detector arrays (Figure 2) use a reset-grated integrator.

Advantages of the reset grated integrator include the fact that it is a simple circuit with a small footprint, and it is reliable enough to be used in large pixel arrays. The reset gated integrator has relatively good noise performance allowing acceptable energy resolution in photon-counting applications. When used with raster readout, the reset gated integrator provides access to signals in neighbor pixels since all pixels are read out for every frame. Neighbor-pixel readout is important when pixel size is small (i.e. good spatial resolution); because in this case the finite volume of charge deposition often results in signal spreading to neighboring pixels. Failure to recover the signal that has spread to neighboring pixels can result in serious degradation of the energy resolution.

Disadvantages of using reset gated integrators are mainly due to the consequences of integrating the leakage current. The leakage current in semiconductor detectors typically has the form $I_L \propto e^{-E/kT}$ where the activation energy, E , may be related to the bulk semiconductor properties or to the behavior of the contacts. A consequence of the relatively long integration time (~ 1 ms) is that pixel size must be kept small so that leakage current is low. Alternatively, only the highest-resistivity CdZnTe can be used and/or the detector must be cooled. For high-resistivity CdZnTe, bulk leakage decreases about an order of magnitude for a temperature reduction of 203 C. Even then, much of the useful dynamic range can be taken up by pixel-to-pixel leakage variation due to defects in the detector crystal and differences in the pixel contacts. The strong dependence of leakage current on temperature means that a high degree of temperature control is required for pixel arrays using reset-gated integrator readout. This problem is exacerbated by the fact that the readout circuit is an active component with heat dissipation.

Another disadvantage of the reset-gated integrative is kTC noise associated with the reset switch;²⁷ fortunately, this noise can be suppressed by correlated double sampling which can be implemented by relatively simple circuit changes. Finally, the raster readout of every pixel, every frame means that the down-stream electronics must be capable of handling high data rates. At the counting rates expected for nuclear medicine applications, most of the data will consist of zeros, and the hits in this data stream due to gamma interactions will be sparse.

A shaper-amplifier circuit is shown in Figure 4. Individual semiconductor detectors used for gamma-ray spectroscopy typically use fast-pulse electronics incorporating a shaper amplifier. Most of the prototype cameras in Table I use individual shaper amplifier circuits or ASICs incorporating about 100 channels of shaper circuits such as the IDEAS XA-1.²⁹

An advantage of the shaper amplifier is its excellent noise performance, 2–5 times better than the reset gate integrator. Another major advantage is that the shaper-amplifier is relatively immune to leakage current due to its short shaping time. In general, the shaping time must be long enough to allow the signal generation due to charge transport to reach completion. However, for electron transport in a CdZnTe pixel detector, the shaping time

can be a fraction of a microsecond, corresponding to an integration time thousands of times smaller than that typical of a reset gated integrator. Shaper amplifiers can also make use of leakage compensation in the preamplifier, and we can use capacitive coupling between the preamplifier and shaper-amplifier stages. Insensitivity to leakage current confers numerous advantages. A hybrid semiconductor-detector array using a shaper-amplifier readout should not require cooling, even if lower-resistivity CdTe/CdZnTe and larger pixel sizes are used. The high degree of temperature control needed with the reset gated integrator will not be required. Some of the leakage-caused inter-pixel non-uniformity seen with detector arrays using the gated integrator will be suppressed with the shaper amplifier. Another advantage of the shaper amplifier is that the readout can be event driven, i.e. the hit pixel triggers its own readout. This has the advantage of reducing the signal processing demand on downstream electronics. Fast timing is also possible with shaper amplifiers.

Disadvantages of shaper amplifiers include the complexity of the shaper circuitry which entails an element of design risk, as well as the difficulty of reading out neighbor pixels. As mentioned before, the recovery of signal shared to neighbor pixels is critical for getting good energy resolution, and signal sharing is exacerbated for the small pixels required for high-resolution, high SpBW systems. The problem arises from the difficulty of triggering on the small signals in neighboring pixels, or alternatively the complexity of the logic needed to have pixels trigger sample-and-hold circuits in neighboring pixels. AEGIS has a simple approach to resolving this problem that will be discussed later. Finally, the use of fast-pulse circuitry raises concerns about intra-pixel and inter-pixel coupling effects.

5 AEGIS DESIGN FEATURES

We have concluded that the advantages of shaper-amplifier circuits for use in AEGIS far outweigh the disadvantages, and that the disadvantages discussed above can be resolved by design innovations. AEGIS will be a two-dimensional pixel array having a shaper-amplifier unit cell. It will also have active leakage compensation and provide for neighbor-pixel readout. Aegis will use modern CMOS design techniques (0.35–0.5 μm) and have a single input power line and a ground line; the additional required currents and biases will be generated on board. It will have a control register that allows digital control of circuit configurations and thresholds. AEGIS will encode signals by current transitions, where possible, in order to suppress intra-pixel and inter-pixel coupling, and a grounded metal shield will be used over the circuitry. The pixel pitch will be 300 μm . This will allow a 64×64 array without exceeding the maximum size for the stepper exposure systems used in most foundrys. We will also provide 100 μm × 100 μm pixel bonding pads which may allow for use of alternative interconnect technologies to indium bump bonding.

6. AEGIS READOUT UNIT CELL

Figure 5 shows a schematic of the proposed unit cell for the AEGIS readout. It has some similarity to commercial discrete electronics used with semiconductor detectors. The preamplifier has an active leakage compensation circuit in the feedback loop. Conventional charge sensitive preamplifiers use a resistor and capacitor in parallel in the feedback loop with the time constant chosen to be longer than the risetime of the signal pulse. An active

leakage compensator is preferable in CMOS designs where large value resistors and capacitors are difficult to implement. The preamplifier is capacitively coupled to a shaper amplifier. The shaping time-constant is set by the resistance and capacitance in the feedback loop. A shaping time constant near $0.5\ \mu\text{s}$ is reasonable; this is slightly larger than the transit time for electrons in a 4 mm thick CdZnTe detector at 400 V bias. The unit cell also contains a variable threshold comparator that is used to determine if a gamma ray has interacted in this pixel; the comparator enables a peak detecting trigger which notifies a circuit elsewhere on the AEGIS readout, (the peripheral circuit) of an event. The peripheral circuit then triggers the sample- and-hold for all pixels in the array so that signals are saved to be later read out.

A transistor-level simulation of the unit cell circuit of Figure 5 was carried out in order to estimate its noise performance and power dissipation. The simulation included the preamplifier, shaper amplifier and leakage compensation circuit. Figures 6a and 6b show the predicted preamplifier output signal and shaper amplifier output signal for a $60\ \text{ke}^-$ signal ($\sim 270\ \text{keV}$ in CdZnTe). Figure 6b allows the conversion gain to be estimated as $8.3\ \mu\text{V}/\text{e}^-$. Figure 6c shows the predicted output noise spectrum at 25°C for a range of leakage currents, $0 - 3\ \text{nA}$. The input-referred, rms noise in electrons can be obtained by integrating the square of the noise for each curve in Figure 6c, taking the square root and dividing by the conversion gain; the resulting plot of rms noise versus leakage current is shown in Figure 6d. The predicted noise is $50\text{--}75\ \text{e}^-$ over a range of leakage current of $0\text{--}3\ \text{nA}$.

The unit cell of the AEGIS readout will be similar to that of Figure 5, but it will have some additional features. A disconnect will be included to turn off any noisy pixels that might threaten to produce cascade behavior in the rest of the array. A test input will be included at the pixel node to allow test and calibration of each pixel. The comparator threshold in each pixel will be set independently; there will be a global threshold and a trim in each unit cell that can be set by an addressable DAC in that cell. The AEGIS unit cell is expected to generically resemble the circuit of Figure 5, but the details of the leakage compensator and the peak detector/trigger portions of or the circuit may differ from that of Figure 5.

Onboard control of the readout process of AEGIS is vested in the peripheral circuit (Figure 7) which is at the edge of the ASIC, outside of the pixel array. When a gamma ray interacts in a pixel and the signal exceeds the comparator threshold, a peak detector is enabled and a trigger signal is sent to the peripheral circuit which then identifies the hit pixel. The peripheral circuit then triggers the sample-and-hold in the hit pixel and its neighbors and disables data acquisition for any further triggers. The peripheral circuit then notifies an external circuit called the event processor that it has data. When the event processor confirms ready, the peripheral circuit sends out data on two analog lines. One output line carries the stored signal from the hit pixel; the other carries a reference signal from a dummy unit cell without a detector connection. The peripheral circuit also sends the address of the hit pixel to the event processor along digital I/O lines. The event processor digitizes the analog signal and reference values; comparison of these values allows suppression of common-mode noise. An FPGA in the event processor decides which neighbor pixels to read out and sends the address of each to the peripheral circuit sequentially over the digital I/O lines. The peripheral circuit then responds by sending the signal for that pixel and the

reference signal over the analog output lines. For a hit pixel and eight nearest neighbors, the readout process should take about 5 μ s. When the readout is completed, the event processor signals completion and the peripheral circuit re-enables data acquisition.

The event processor (Figure 7) is an external circuit that acquires the data and controls the acquisition process. One event processor can control multiple AEGIS chips, the exact number will depend on pileup considerations, which in turn depends on the expected counting rates. We already use event processors with similar design and capabilities on two existing small animal imaging systems FAST SPECT II and Semi SPECT¹⁵ at CGRI. These event processors are specifically designed to facilitate list-mode readout which will be the approach used with AEGIS. In list-mode readout, all the pertinent information about a given gamma-ray interaction, including digitized signals from the hit pixel and its neighbors is passed to the data acquisition computer as a single word. Events are processed later, off line and are accepted or rejected and compiled to form images at that time.

7. AEGIS DEVELOPMENT AND FUTURE WORK

An 8×8 prototype AEGIS readout is currently being designed at Augustine Engineering and will be fabricated via a MOSIS run in the Fall of 2005. The prototype AEGIS will demonstrate all the features of a full 64×64 AEGIS including the unit cell, triggering, the peripheral circuit, the control register and the I/O protocol with an event processor. We expect to test the prototype by making 8×8 hybrid CdZnTe detector arrays and testing their performances for imaging and spectroscopy. A full 64×64 AEGIS will then be designed fabricated and tested. AEGIS will be made available as a product of Augustine Engineering to researchers and developers of commercial imaging systems in nuclear medicine, biomedical imaging and other fields. For instance, AEGIS 64×64 hybrid semiconductor arrays would be ideal components for small-animal SPECT imaging systems that would follow CGRI's SemiSPECT.¹⁵ AEGIS hybrids could drive the development of small-format cameras similar to those of Table 1, but with much better spatial resolution. But the goal that motivates AEGIS development is to push on to future clinical nuclear medicine cameras with high spatial resolution and very large SpBW. Hundreds of AEGIS hybrid semiconductor detector arrays would be needed for such a camera. One possible approach is the development of semiconductor detector modules of intermediate size (say 128×128 arrays of 7.68 cm × 7.68 cm with pixel pitch of 0.6 mm) that make use of four AEGIS readouts and a fanout board that connects the readout ASICs to a tiled array of CdZnTe detector with twice the pitch. A few tens of such modules would suffice to build a clinical semiconductor detector camera with superb spatial resolution and SpBW an order of magnitude better than any scintillation camera currently available.

Acknowledgments

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Fig. 1a.

Fig. 1b.

Figure 1.

Fig. 1a. Illustration of a multi-pinhole imager used with low-resolution detectors.

Fig. 1b. Illustration of a multi-pinhole used with high-resolution detectors. With the same final resolution and field of view as in Fig. 1a, this system can have much higher sensitivity.

Figure 2.

University of Arizona 64×64 CdZnTe hybrid semiconductor detector Array.¹⁴ The 64×64 readout ASIC is mounted underneath the detector array, which is the square at lower left. The hybrid detector array is mounted on a ceramic board with some surface-mount components used for noise filtering. Augustine Engineering designed this ASIC.

Figure 3.
Reset gated integrator

Figure 4.
Shaper amplifier

Figure 5.
Schematic diagram of the proposed AEGIS readout unit cell.

Figure 6.

a. Predicted preamplifier output signal; b. Predicted shaper output signal; c. Predicted output noise spectrum; d. RMS noise versus leakage current.

Figure 7.
Schematic of AEGIS readout communications configuration.

Table 1**CdZnTe/CdTe Clinical Imaging System**

Camera/MFG	Type	Area	Pixel Size	SpBW [*]	Remarks	Reference
NUCAM 3 [Soreq]	CdZnTe	18.5×20.1 cm ²	2.1 mm	8448	528, 4×4 arrays	5
SOLSTICE	CdZnTe	182 cm ²	1.8×3.6 mm	2816 [†]	Rotating-Slat Coded Aperture	6
BIOMED II	CdTe	15×15 cm ²	3.1 mm	2304	Individual Crystals	7
EI GEMS	CdZnTe	20×20 cm ²	2.5 mm	6400	25 Imarad Modules ⁺	8
[Siemens]	CdZnTe	12×20 cm ²	2.5 mm	3840	15 Imarad Modules ⁺	9
SSGC	CdTe	4.5×4.5 cm ²	1.4 mm	1024	Sentinel Node Biopsy	10
PEGASE	CdZnTe	18×21.5 cm ²	4.5 mm	1920	Larger System Planned [@]	11
MGC 700 [AIAT]	CdTe	4.4×4.4 cm ²	0.5 mm	7744	Under Development [@]	12
2020 tc [Digirad]	CdZnTe	20×20 cm ²	~3 mm	4096	Discontinued [@]	13
Arizona Hybrid	CdZnTe	2.4×2.4 cm ²	0.38 mm	4096	Probe	14
SemiSPECT [UA]	CdZnTe	8×2.4×2.4 cm ²		32768	Small Animal Imaging	15
Luma Gem [™] 3200 [Gamma Medical]	CdZnTe	16×20 cm ²	2.5 mm	5120	20 Imarad-like Models [@]	16
[eV Products]	CdZnTe	3.4×3.4 cm ²	2.0 mm	256	Probe	17

[@] Commercial Product;⁺ Imarad/Orbotech Module, 4 cm×4cm×0.4cm, 16×16 array + readout;^{*} SpBW = number of pixels;[†] Interconnected Linear Arrays, SPBW given as # of detectors