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A 180-V_{pp} Integrated Linear Amplifier for Ultrasonic Imaging Applications in a High-Voltage CMOS SOI Technology

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Abstract

This brief presents a monolithically integrated fully differential linear HV amplifier as the driver of an ultrasonic transducer. The linear amplifier is capable of transmitting HV arbitrary signals with a very low harmonic distortion, which is suitable for tissue harmonic imaging and other ultrasonic modes for enhanced imaging quality. The amplifier is designed and implemented using the 0.7- μm CMOS silicon-on-insulator process with 120-V devices. The amplifier, when driving a

load of 300 pF in parallel with 100 Ω , is capable of transmitting a sine-wave signal with a frequency of up to 4.4 MHz, a maximum signal swing of 180 V_{pp}, and a second-order harmonic distortion (HD2) of -56 dBc but only dissipating an average power of 62 mW with a 0.1% duty cycle.

Index Terms

High voltage (HV); linear amplifier; second-order harmonic distortion (HD2); tissue harmonic imaging (THI); total harmonic distortion (THD); ultrasonic imaging; voltage swing

I. Introduction

In an ultrasound system, the transmitter that generates HV signals to excite a transducer is one of the most critical components in the entire ultrasonic diagnostic system. First of all, the transmitter needs to be capable of generating HV signals to ensure the penetration depth of ultrasonic signals. The target of this brief is to support the high end of the signal swing required in B-mode up to 180 V_{pp}. This HV signal swing is beyond the breakdown voltage of the devices in most existing HV CMOS processes. Moreover, to enhance the imaging quality, new imaging techniques, such as tissue harmonic imaging (THI), have been developed to provide images of better quality and contrast as compared with conventional ultrasound techniques [1]. In THI, the ultrasonic energy is transmitted in a fundamental frequency, and an image is formed based on the second-order harmonic distortion (HD2) of the received signal, which is generated by the inherent nonlinearity of the body tissue. To obtain good imaging quality using THI, it is thus crucial to minimize the harmonics generated from the ultrasonic systems including both the transmitter and the receiver. In particular, the desired HD2 for THI is lower than -40 dBc for a sinusoidal signal of a few megahertz [2], with a load of 300 pF//100 Ω to emulate the transducer [3].

Most of today's commercial medical ultrasound machines use HV digital square-wave pulsers (unipolar or bipolar) as the transmitters. Although simple and power efficient, the digital pulsers reported in [4] contain an HD2 of -28 dBc, which is not suitable for THI. Harmonic suppression techniques can be applied in both the transmitter and the receiver. Techniques on harmonic suppression in the receivers are widely discussed in literature [5]. On the transmitter side, it is more challenging to apply harmonic suppression due to the HV operation and the difficulty of integrating the low voltage (LV) and HV devices on a single chip. The work in [6] introduced methods to generate multilevel ultrasound pulses using digital pulsers. The work in [7] presented a push-pull linear amplifier designed using discrete MOSFETs and transformers. The work in [8] used a second harmonic inversion technique that employs *I* and *Q* pulses on an interleaved checker board aperture to cancel the HD2 synthetically.

There is a demand to design an integrated HV linear power amplifier capable of generating HV signals with a low HD2 for THI. With the availability of such a linear amplifier in CMOS, it is possible to integrate digital circuitry on the same chip to provide shaping and timing to the waveform. This solution can support various imaging schemes for enhanced image quality by exciting the transducers with any number of complex voltage waveforms to

control the frequency spectrum and the pulse duration. The works in [9] and [10] presented an integrated ultrasound linear amplifier for ultrasound applications, but the maximum voltage swing is only $90 V_{pp}$.

In this brief, we present an integrated HV linear amplifier employing a fully differential topology to achieve a high signal swing beyond the device breakdown voltage limited by the process and to simultaneously obtain a low HD2. Given the technology transit frequency and a load of $300 \text{ pF}/100 \Omega$, we target the amplifier at achieving a 5-MHz bandwidth for the B-mode THI with a medium resolution but a deep body penetration depth [11]. To the best of our knowledge, this amplifier presents the lowest HD2 compared with the published ultrasonic transmitter works while delivering a $180\text{-}V_{pp}$ signal swing. Section II details the design considerations, including the architecture selection and design of the gain and buffer stages of an HV linear amplifier. Section III presents the measurement setup and results. Section IV provides the conclusion.

II. Design of Fully Differential Linear Amplifier

A. Architecture Selection

The technology used for this linear amplifier contains HV devices that have a drain–source junction breakdown voltage $V_{ds,max}$ of 120 V and a gate-oxide breakdown voltage $V_{gs,max}$ of 18 V, and it contains medium-voltage devices with a $V_{ds,max}$ of 50 V and a $V_{gs,max}$ of 5 V. The maximum achievable output voltage swing using a conventional class-AB amplifier is less than $120 V_{pp}$ without operating the devices beyond their break-down voltage. Extra HV protection techniques are required in order to boost the output voltage swing to be above $120 V_{pp}$.

One of the widely used HV protection techniques is based on the totem-pole topology, which employs additional source followers in the biasing of the stacking output transistors to divide the voltage across several devices connected in series [12]. Such structure may allow for output voltages higher than the breakdown voltage of the individual devices, but that approach needs an extra higher supply-voltage headroom, which would increase the power consumption, and the HD2 in this architecture remains high.

To achieve a low HD2 and a voltage swing beyond the transistor voltage limitation, we propose a fully differential structure. The output of the fully differential structure is twice that achievable through a single-ended design, which is capable of generating output swings close to twice that of the device limitations (minus the voltage headroom of transistors). Additionally, the differential structure inherently cancels out the HD2, enabling a more linear output compared with a single-ended design. As shown in Fig. 1, the proposed amplifier takes in a $\pm 1\text{-V}$ differential sinusoidal signal, amplifies it by a gain of 45 through two gain stages followed by a class-AB output buffer stage, and produces a sinusoidal output of $90 V_{pp}$ on each single-ended side. The two differential outputs are connected to an off-chip HV transformer, which converts the differential output signal to a single-ended $180\text{-}V_{pp}$ signal as the final output across the ultrasonic transducer. Fig. 2 depicts the circuit schematics, where $VDDL/VSSL$ are $\pm 25 \text{ V}$, and $VDDH/VSSH$ are $\pm 60 \text{ V}$. Detailed design considerations, the tradeoff, and the optimization are described in the following sections.

B. Design of Output Buffer Stage

Due to the HV and bandwidth requirements on the transmitter, the output stage of the linear amplifier is one of the most critical building blocks in the design, which determines the signal swing and the frequency bandwidth. Most of the ultrasound transducers have a low impedance between 50 and 100 Ω , which is much lower than the output resistance of the transistors. To avoid gain degradation and to isolate the low impedances from the gain stage, an HV push-pull class-AB stage is used as an output buffer.

The HV buffer design involves tradeoffs among the output signal swing, the maximum current needed to be delivered to the load, the reliability of the devices, and the frequency response of the circuit. To keep HV transistors M8, M9, M1, and M2 in saturation, as shown in Fig. 2, the maximum signal swing is $120 \text{ V} - (V_{\text{od},\text{M8}} + V_{\text{th},\text{M1}} + V_{\text{od},\text{M1}} + V_{\text{od},\text{M9}} + V_{\text{th},\text{M2}} + V_{\text{od},\text{M2}})$, where V_{od} is the overdrive voltage, V_{th} is the threshold voltage, and $(V_{\text{od}} + V_{\text{th}})$ for each device needs to be lower than $V_{\text{gs,max}} = 18 \text{ V}$. With a peak voltage V_{peak} , the peak current delivered to the load is $I_{\text{peak}} = V_{\text{peak}}/|Z_L(2\pi f)|$, where f is the signal frequency, and Z_L is the load of 300 pF/100 Ω . For example, for a V_{peak} of 100 V and $f = 5 \text{ MHz}$, the resulting I_{peak} is 1.37 A. Based on I_{peak} and $V_{\text{gs,max}}$, the transistor size can be determined

according to $V_{\text{od}} = \sqrt{2I_{\text{peak}}/[k(W/L)]}$. This leads to very large transistor dimensions, on the order of tens of millimeters for the transistor width in the output stage, which would result in large parasitic capacitance and limit the frequency response. A higher V_{peak} would result in higher I_{peak} , which in turn gives rise to higher V_{od} for the same W/L or a larger W/L to keep the same V_{od} . In our design, we optimize the design by choosing the transistor size to ensure a 5-MHz bandwidth while achieving the maximum possible signal swing and keeping $V_{\text{od}} + V_{\text{th}}$ to be below $V_{\text{gs,max}}$ with some margin. This yields a size of 15 mm/6 μm for the nMOS device, 28 mm/10 μm for the pMOS device in the output buffer stage, and a signal swing of 90 V_{pp}, which leaves enough voltage headroom to keep all transistors in saturation. A small biasing current generated by the diode-connected transistors (M3A, M3B, M4A, and M4B) are used to set the V_{gs} of the devices to be slightly above the device V_{th} for good linearity. The static current is small, which is on the order of milliamperes.

The transformer turn ratio is chosen to be 1: 1 to obtain an output swing of 180 V_{pp} and to maximize the bandwidth. This is because a larger turn ratio ($N: 1$, where $N > 1$) would require an output voltage of $N \times 90 \text{ V}$ from the buffer stage, which is nearly impossible to obtain using the 120-V technology. On the other hand, a smaller N ($N < 1$) would reduce the load impedance and increase the capacitance seen by the buffer by a factor of N^2 , which would greatly reduce the amplifier bandwidth.

C. Design of Gain Stage

The gain stage is another critical building block of the ultrasound transmitter. In most HV processes, because the transistor gate length is large and an additional low-doped HV drift region is employed in series with the channel, the HV transistors tend to have a low intrinsic gain bandwidth (GBW) product (typically in the range of hundreds of megahertz or lower gigahertz). To achieve an overall gain of 45 for a bandwidth of 5 MHz while driving a load of 300 pF/100 Ω , we choose to cascade an LV closed-loop amplifier followed by an HV

closed-loop amplifier to boost the overall GBW [13], as shown in both Figs. 1 and 2. The LV stage uses devices with $V_{ds,max}$ of 50 V and a supply voltage of ± 25 V, whereas the HV stage uses ± 60 V. Both the LV and HV stages employ their own local feedback to ensure well-controlled gain, stability, device reliability, and bandwidth.

Due to their low transit frequency, the HV devices become the bottleneck of the overall frequency response of the linear amplifier. The highest bandwidth of the overall cascaded amplifier is achieved when both the HV and LV stages have equal bandwidth [13]. Thus, we allocate a gain of 16.87 for the closed-loop LV amplifier and a gain of 2.67 for the closed-loop HV stage, achieving an overall gain of 45 that is needed while obtaining the same bandwidth for the LV and HV amplifiers and the maximum overall bandwidth.

For both the LV and HV amplifiers, a two-stage Miller operational amplifier (op-amp) topology is employed. Due to the large transistor gate length and an additional low-doped HV drift region, the transconductance of the HV laterally diffused MOS transistor is so small that its $1/g_m$ becomes even larger than its output resistance r_o . Consequently, when we compare a two-stage op-amp with a single-stage op-amp with the same input transistor size and loading capacitance C_L , the nondominant pole frequency of the two-stage op-amp $1/(r_o \cdot C_1)$, where C_1 is the output capacitance of the first gain stage, would be higher than that of the single-stage op-amp g_m/C_L . This results in a larger GBW product for a two-stage op-amp than for a single-stage topology for HV operation. For these reasons, a two-stage Miller-compensated op-amp is used for both the LV and HV gain stages.

D. HV Design Considerations

For reliable device operations under an HV, it is crucial to ensure that all devices in the design are operated under safe voltages. Both the LV and HV amplifiers use a differential amplifier structure for their input stage with a tail current source, and each of the LV and HV stages employs its own negative feedback. The negative feedback ensures a very small ac signal between the positive and negative inputs of the LV and HV amplifiers. The tail current source allows the source node of the input transistors to follow both inputs; thus, there would be no gate-oxide breakdown. The second stage of both the LV and HV amplifiers is carefully designed to have enough gain so that the device V_{gs} is always less than $V_{gs,max}$. Since both the LV and HV devices are operated on the same chip with two different power rails, proper power sequencing is needed to ensure circuit reliability. For a ± 1 -V input signal, the LV amplifier delivers ± 16.87 V to the HV amplifier. It is important to turn on ± 60 V before tuning on ± 25 V to prevent a large signal from the LV amplifier to cause damage to the HV input stage.

III. Measurement Setup and Results

The fully differential linear amplifier was designed, implemented, and fabricated using a 0.7- μ m 120-V silicon-on-insulator HV process. The chips were assembled in a 56-pin quad-flat no-leads (QFN) plastic package. The packaging size was 8 mm $\times$ 8 mm. Fig. 3 illustrates the layout view and the photo of the test chip. The linear amplifier layout occupies an area of 6 mm $\times$ 2.3 mm. On the test board, we used 300 pF//100 Ω to emulate the transducer. The input arbitrary signal was generated by a Tektronix AFG3012 function generator. The output

of the linear amplifier was directly measured by an oscilloscope with a 1-M Ω input impedance and an HV option.

In the first set of experiments, an input signal frequency of 2 MHz with a pulse repetition frequency of 2 kHz is set for both a continuous wave (CW) sinusoidal signal and a six-cycle Morlet wavelet (often, six cycles of a Morlet wavelet are recommended, but fewer cycles can be also used to the benefit of the temporal resolution but at the expense of the frequency resolution). Figs. 4 and 5 show the measured output waveforms and the frequency spectrum. Due to the limitation of the equipment at the time of the measurement, the wave-form magnitude was only measured up to 140 V_{pp}. The fully differential amplifier achieves a measured HD2 of -56 dBc, which is a 20-dB improvement from that of a single-ended channel that was measured to be -36 dBc. To achieve such a low HD2 using the differential structure, good matching in the layout between the two single-ended channels is required. This is done in our layout by careful floor planning and having the layout of one single-ended channel be the exact mirror of the other single-ended channel. The amplifier has a 1-dB gain compression point (P1dB) of 51 dBm and an input-referred third-order interception point (IIP3) of 43 dBm. The effective power consumption of the chip is 62 mW with a 0.1% duty cycle.

Next, we measured the HV amplifier performance interfacing with a real transducer (Panametrics NDT V382). For comparison, we also used a commercial radio-frequency amplifier instrument ENI 325LA (with a size of 7.0"H $\times$ 10.0"W $\times$ 16.5"D and a weight of 35 lb) interfacing with the same transducer. The signal frequency is set at 3.5 MHz in this case. The pulse-echo measurement setup is shown in Fig. 6. We sent pulses and then read the transducer-collected echoes by using a LeCroy oscilloscope. The measured frequency spectrum of a three-cycle burst signal at the amplifier output shown in Fig. 7(a) indicates that our integrated HV linear amplifier and the commercial ENI amplifier achieve the same HD2. Fig. 7(b) shows that the HD2 of the pulse-echo signal of ENI 325LA is less than 2 dB lower than that of our HV integrated linear amplifier.

The measured frequency response in Fig. 8 shows that the -3-dB closed-loop bandwidth of our HV linear amplifier is 4.4 MHz, driving a load of 300 pF//100 Ω at an amplitude of 140 V_{pp}. The bandwidth is independent of the output amplitude. Both the LV and HV amplifiers have multipole closed-loop frequency responses, and when they are connected in series, those poles overlap, sharpening the roll-off of the overall frequency response. The bandwidth can be further improved by using a process with a higher intrinsic frequency or by techniques such as a current feedback amplifier [14].

We also compared the performance of our HV power amplifier IC to an existing commercial product Supertex MD2130 [15] when both are driving a 0.1% duty-cycle signal. For comparison purposes, we use the same output load, i.e., 220 pF//1 k Ω , for our linear amplifier as the Supertex MD2130 does. The reduced capacitance results in a higher bandwidth for our chip compared with that presented in the previous section with a load of 300 pF//100 Ω . The performance comparison between our amplifier, Supertex MD2130, and other states of the art is listed in Table I. Our linear amplifier achieves the lowest HD2 reported among all commercial products and published works. The limitation of this

approach is that it requires an off-chip transformer, which is hard to implement on chip and would limit the number of channels inside the probe head of the transducer. On the other hand, using the presented linear amplifier IC will result in greatly reduced system size and cost for high-end ultrasonic instruments. Multiple channels can be implemented on chip, and the number of channels would be mainly limited by the total power consumption that the chip package can handle. Multiple ICs can be employed to further increase the number of channels for high-end ultrasonic instruments.

IV. Conclusion

This brief has presented an integrated HV linear amplifier for ultrasound transmitters with 180 V_{pp} and an HD2 of –56 dBc. This solution can support various imaging schemes for enhanced image quality with arbitrary waveform excitation. Because of its integration capability with LV devices, very good linearity, and large signal swing, the proposed amplifier is attractive for high-end ultrasonic applications.

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Fig. 1.
Circuit diagram of a fully differential amplifier as the transmitter.

Table of device parameters		
	Instance Name	Size (μm/μm) or value
HV amp and output stage	M1A,M1B	15000/6
	M2A,M2B	28000/10
	M3A,M3B	4899/6
	M4A,M4B	8601/3
	M5A1,M5A2,M5B1,M5B2	30/10
	M6A1,M6A2,M6B1,M6B2	600/6
	M7A,M7B	320/10
	M8A,M8B	2900/10
LV amp	M9A,M9B	1900/6
	CcA,CcB	8 pF
	M1A,M1B	200/6
	M2A,M2B	46/6
	M3A,M3B	50/10
	M4A,M4B	400/10
	M5A1,M5A2,M5B1,M5B2	600/6
	M6A1,M6A2,M6B1,M6B2	90/10
	M7A,M7B	800/10
	CcA,CcB	3 pF

Fig. 2.
Schematic view of the cascaded fully differential amplifier.

Fig. 3.

(a) Layout view of the linear amplifier. (b) Photo of the off-chip transformer, the integrated linear amplifier, and a coin.

Fig. 4.

(a) Measured differential output of the 2-MHz CW sine wave. (b) Spectrums of the single-ended and fully differential outputs. The load is 300 pF//100 Ω .

Fig. 5.

(a) Measured differential output of the six-cycle Morlet wavelet. (b) Spectrums of the single-ended and differential outputs of the Morlet wavelet.

Fig. 6.
Pulse-echo measurement test bench.

Fig. 7.

Our linear amplifier and ENI 325LA output spectrums of the (a) three-cycle pulsed sinusoidal signal and the (b) pulse echo, with the load of the Panametrics NDT V382 transducer.

Fig. 8.
Frequency response with a load of 300 pF//100 Ω .

TABLE I

Performance Comparison Between the Presented Integrated Linear Amplifier and Published Works

	This work		Supertex MD2130 [15]	[10]	[14]
Output load	220 pF//1k Ω	300 pF//100 Ω	220 pF//1k Ω	150 pF//100 Ω	300 pF//100 Ω
HD2	-63 dBc	-56 dBc	-46 dBc	-43 dBc	-50 dBc
THD	-48 dB	NA	-45 dB	-42 dB	-48 dB
Bandwidth	8.7 MHz	4.4 MHz	15 MHz	6.5 MHz	8.6 MHz
Voltage swing	180 Vpp		180 Vpp	90 Vpp	180 Vpp
Power supplies	2		1	2	2
Output transformer	Yes		Yes	No	No
External DAC	Yes		No	Yes	Yes
Power consumption	62 mW	152.5 mW (including digital circuits and DAC)		37 mW	NA