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CMUTs with High-K Atomic Layer Deposition Dielectric Material Insulation Layer

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Abstract

Use of high- κ dielectric, atomic layer deposition (ALD) materials as an insulation layer material for capacitive micromachined ultrasonic transducers (CMUTs) is investigated. The effect of insulation layer material and thickness on CMUT performance is evaluated using a simple parallel plate model. The model shows that both high dielectric constant and the electrical breakdown strength are important for the dielectric material, and significant performance improvement can be achieved, especially as the vacuum gap thickness is reduced. In particular, ALD hafnium oxide (HfO₂) is evaluated and used as an improvement over plasma-enhanced chemical vapor deposition (PECVD) silicon nitride (SixNy) for CMUTs fabricated by a low-temperature, complementary metal oxide semiconductor transistor-compatible, sacrificial release method. Relevant properties of ALD HfO₂ such as dielectric constant and breakdown strength are characterized to further guide CMUT design. Experiments are performed on parallel fabricated test CMUTs with 50-nm gap and 16.5-MHz center frequency to measure and compare pressure output and receive sensitivity for 200-nm PECVD SixNy and 100-nm HfO₂ insulation layers. Results for this particular design show a 6-dB improvement in receiver output with the collapse voltage reduced by one-half; while in transmit mode, half the input voltage is needed to achieve the same maximum output pressure.

I. Introduction

As suggested by the simple linear parallel plate capacitive micromachined ultrasonic transducer (CMUT) equivalent circuit, which is suitable for modeling small signal receive mode operation, the electromechanical transformer ratio of a CMUT is determined as the product of the DC electric field and the device capacitance [1]. In the transmit mode, where large voltage signals are applied to obtain large membrane displacement swings, the electrostatic force applied to the CMUT membrane is a quadratic function of the ratio between the applied voltage to the instantaneous gap [2]. Therefore, one should reduce the gap between the top and bottom electrodes of the CMUT for efficient operation with reduced voltage levels. Limitations to the gap thickness will be the minimum gap thickness required for the desired transmit pressure at the operation frequency and the fabrication process limitations.

Ideally the gap between the electrodes is filled with vacuum and can be completely traversed during the CMUT operation, but most realistic CMUT structures are as shown in Fig. 1. A layer of dielectric material exists between the top and bottom electrodes to ensure that the electrodes do not electrically short during full gap swings in transmit and near collapse operation during receive. This layer of dielectric material must by design be able to withstand the maximum electric fields generated within the material during CMUT operation, especially if the CMUT has already collapsed and the electrodes are separated only by the thin dielectric layer [3]–[6]. If one keeps the movable vacuum gap thickness the same to retain the same membrane displacement range, for a given applied voltage, this dielectric layer reduces the electric field and the device capacitance because it effectively increases the vacuum gap thickness. As further discussed below, the choice of the dielectric layer becomes a significant factor in determining the electromechanical performance of the CMUT, especially when the vacuum gap thickness is small (<100 nm).

Materials such as low-pressure chemical vapor deposition (LPCVD) silicon nitride (SixNy), plasma-enhanced chemical vapor deposition (PECVD) SixNy, thermal silicon oxide (SiO₂), and PECVD SiO₂ are traditional dielectric materials in semiconductor processing and are commonly used as the insulation dielectric material in different CMUT fabrication processes [7]–[10]. Here we focus on a low temperature surface micromachining-based CMUT fabrication process, which allows monolithic integration of complementary metal oxide semiconductor transistor (CMOS) electronics and CMUT imaging arrays [11]–[13]. This approach is particularly suitable for catheter-based ultrasound imaging applications where small size and flexibility is important [6], [14], [15].

In low temperature surface micromachining processes for CMUTs, it is convenient to use the same PECVD SixNy (abbreviated as SiN) as the dielectric insulation material [7], [11], [16], [17] and membrane structure material. However, as demonstrated below, higher performance CMUTs can be realized by choosing a high- κ dielectric material (high dielectric constant κ as compared with silicon dioxide) with minimal adverse effects in terms of achievable device capacitance and electric field.

There are many high- κ materials cited in literature with dielectric constants ranging from 9 to 200 [18], [19]. However, there is a tradeoff between dielectric breakdown strength (EBD) and the dielectric constant κ . This is a non-linear relationship shown both in theory and in experiments [18], [20], meaning that a decrease in dielectric strength corresponds to an increase in κ value. In selection of a suitable high- κ dielectric material to improve capacitance while designing for maximum voltage requirements of CMUTs, we took a balanced approach in material selection of these 2 parameters. According to Robertson [20], dielectric materials with a good balance between κ and EBD are ZrO₂, HfO₂, La₂O₃, Y₂O₃, and SrO. We chose hafnium oxide (HfO₂) for the study of this paper due to its promising material performances in terms of κ and EBD and its wide use in the scale-down of CMOS [21]. Although there are many methods to deposit high- κ dielectric materials such as sputtering and chemical vapor deposition, here the method of ALD is selected. This method is attractive for CMUT application because of its low temperature processing, conformal deposition over large areas, intrinsically stress-free film, and ability to have nanometer precision control over the thickness of the film [22], [23].

In this paper the ALD HfO₂ (abbreviated HfO) film is deposited at 250°C and both κ and EBD are characterized in section III. We note that previous work with ALD materials for CMUTs focused on advantages of aluminum oxide (Al₂O₃) as a thin conformal structural film as a membrane material [24], [25]. Another initial investigation of HfO₂ as a potential high-performing dielectric layer for air coupled CMUTs have been performed in [26]. The advantages of using ALD materials for collapsed-mode CMUT operation due to its high dielectric constant have also been proposed, but no optimization study or experimental data has been provided [27].

In this paper, we explore the performance improvements through the use of high- κ insulation layer in CMUTs fabricated through a low temperature surface micromachining process, which is compatible with CMOS integration. We investigate the effect of the insulation layer on transmit and receive performance by using a simple parallel plate model and consider practical limitations due to electrical breakdown. We compare the modeling results for SiN and HfO. We then present HfO characterization results and details of CMUT fabrication using HfO. Finally, we present comparative experimental results on CMUTs with SiN and HfO insulation layers demonstrating the performance advantages of high- κ dielectrics.

II. Effect of Dielectric Insulation Material on CMUT Performance

In order to evaluate dielectric insulation materials for CMUT applications, we follow a step by step approach. We first focus on the electrostatic force and transformer ratio, limited by the breakdown strength and at the limit of vanishing vacuum gap. We then calculate these parameters specifically for HfO and SiN materials for practical vacuum gap and insulation layer thickness. Finally, we impose the collapse voltage limitations on these curves for a particular CMUT geometry used in experimental comparisons.

A. Criteria for Choosing the Insulation Layer Material

Using a simple parallel plate model as shown in Fig. 1, the electrostatic force applied to the electrodes, F_{el} , can be written as

$$F_{el} = \frac{\epsilon_0 A V^2}{2 \left(g_0 + \frac{t_d}{\kappa} \right)^2} = \frac{\epsilon_0 A V^2}{2 g_{eff}^2} \quad (1)$$

where “ ϵ_0 ” is the permittivity of free space (F·m⁻¹); “ κ ” is the dielectric constant or relative permittivity of the material (unitless); “ g_0 ” is the initial vacuum gap (m); “ $V(t) = V_{DC} + V_{AC}$ ” is the total input voltage (V). The term in the denominator of (1) is also known as the “effective” gap (g_{eff}) of the CMUT which the vacuum and dielectric layer thicknesses can be lumped into a single term and expressed as

$$g_{eff} = g_0 + \frac{t_d}{\kappa} \quad (2)$$

where t_d is the thickness of the dielectric layer. This is simply an equivalent vacuum gap value that represents the same capacitance between the top and bottom electrodes of a

capacitor. To evaluate the effect of the dielectric material on the electrostatic force, one can consider the limiting case that the vacuum gap “g” is close to zero, and the voltage on the dielectric layer is at maximum value, i.e. $V = E_{BD}t_d$. In this case, the electrostatic force approaches the value

$$F_{el} \rightarrow \frac{\epsilon_0 A (E_{BD} t_d)^2}{2 \left(\frac{t_d}{\kappa}\right)^2} = \frac{\epsilon_0 A (E_{BD} \kappa)^2}{2} \quad (3)$$

This result shows that for larger electrostatic force generation in the transmit mode, one should choose the dielectric material with the larger $E_{BD}\kappa$ product. For example, SiN has E_{BD} in 4–9 MV/cm and κ in the 6–7 range [28], which depends on the plasma power, gas ratios, temperature and processing pressure of deposition. The particular nitride layer we use for CMUT-on-CMOS processing has $E_{BD} = 6.5$ MV/cm and $\kappa = 6.3$ [29]. In comparison, HfO has E_{BD} in 4–6.7 MV/cm range [18] depending on the molecular structure it takes during various deposition conditions. Low temperature HfO typically has breakdown strength of 4 MV/cm and κ in 14–16 range as deposited below 300°C. However, higher κ values, in the 20–25 range, can be achieved with either higher deposition temperatures, as high as 370°C [30]–[32] or post deposition high temperature annealing in the 300–500°C range [18], [20]. Leakage current improvements were also previously observed and reported after annealing, reducing the physical defects that may exist inside the thin film after deposition. Since most of the quoted annealing recipes are within the thermal budget of a CMOS compatible process, these methods can be used to enhance HfO properties for CMUT-on-CMOS implementation. As described in Section III, the particular HfO layer we deposited has $E_{BD} = 4$ MV/cm and $\kappa = 16$. Therefore, one can expect up to 2.5 times improvement in electrostatic force generated when SiN is replaced with HfO and each film used close to their breakdown limit.

For the receive mode, one can use the small signal equivalent circuit turns ratio, η [33] as a comparison metric, especially when a low impedance transimpedance amplifier (TIA) is used to convert the current at the output of electromechanical transformer to voltage. A TIA with negligible input impedance will effectively short circuit both the CMUT and parasitic capacitances. As compared to high input impedance voltage amplifiers, this approach significantly reduces the negative effects of parasitic capacitance and ensures constant voltage operation. Consequently, a TIA based receiver has been popular for integrated circuit (IC) design for CMUTs, and in this context provides us with a metric independent of the parasitic capacitance [10], [34]. With low receiver impedance the output current (neglecting the spring softening effect) will be proportional to η , which is given by

$$\eta = \frac{F_{AC}}{V_{AC}} = \frac{\epsilon_0 A V_{DC}}{\left(g_0 - x + \frac{t_d}{\kappa}\right)^2} \quad (4)$$

where, x is the absolute value of the displacement of the membrane from the initial gap with applied bias and $g = g_0 - x$. If again one considers the limit where the vacuum gap vanishes and maximum field sustainable on the dielectric layer is used, i.e. $V_{DC} = E_{BD}t_d$, the transformer ratio takes the form

$$\eta \rightarrow \frac{\varepsilon_0 A E_{BD} t_d}{\left(\frac{t_d}{\kappa}\right)^2} = \frac{\varepsilon_0 A E_{BD} \kappa^2}{t_d} \quad (5)$$

Therefore, for higher receive sensitivity, one should use the dielectric with a high E_{BD} , but especially high κ due to the quadratic dependence. In addition, the dielectric material which can be deposited as a thinner high quality film should be selected to minimize “ t_d ” without compromising the dielectric properties. For example, when used at the limiting field strength, HfO should provide up to 3.8 times larger as compared to SiN of the same thickness. However, as discussed below, reliable deposition of SiN is limited to about 200-nm, whereas thinner layers of HfO can be deposited with good dielectric properties, leading to a more significant advantage.

To analyze the effect of the insulation layer on coupling coefficient of a parallel plate CMUT model, one can modify the expression in A16 from [35] such that:

$$k_T^2 = \frac{1}{1 + \left(\frac{g_{eff} - 3x}{2x}\right) \left(1 + \frac{C_p}{C_a}\right)}. \quad (6)$$

Here, C_p is the parasitic capacitance and $C_a = \frac{\varepsilon_0 A}{(g_{eff} - x)}$ is the active device capacitance under applied bias voltage. Note that if one uses a high- κ dielectric material, then g_{eff} is reduced while keeping the same vacuum gap. This implies that although all CMUTs would

theoretically achieve $k_T^2 = 1$ at collapse ($x = \frac{g_{eff}}{3}$), this limit will be approached with a smaller DC bias with reduced g_{eff} . In addition, for any given stable DC bias and non-zero C_p , k_T^2 will be larger since C_a is larger (i.e. the ratio C_p/C_a is smaller). The relevant graphs for the effect of parasitic capacitance on coupling coefficient can be found in [35]. Given the same mechanical properties for the CMUT (same mechanical Q), the noise figure will also improve with larger coupling coefficient as described in [36].

B. Comparison of HfO₂ and PECVD nitride Insulation Layers in Transmit Mode CMUT Operation

The maximum output pressure of a transmitting CMUT is determined by the ability to reach full gap swing when actuated. It is important to achieve the same full gap swing with a smaller voltage input, i.e. higher transmit sensitivity. This is especially significant in case of CMUT-on-CMOS integration applications when pulse amplitudes generated by IC pulsers are limited by the CMOS fabrication process [11]. For a fair comparison between HfO and SiN insulation materials we compare the electrostatic force, F_{eld} , generated for the same input voltage using (1) for the same vacuum gap. We then normalize F_{eld} with the maximum electrostatic force generated for the same vacuum gap, i.e. *without* the dielectric insulation layer ($t_d = 0$), F_{elnd} , to arrive a force ratio, R_F :

$$R_F = \frac{F_{eld}}{F_{elnd}} = \frac{g_0^2}{(g_0 + \frac{t_d}{\kappa})^2} = \frac{g_0^2}{(g_{eff})^2} \quad (7)$$

Figure 2 plots R_F as a function of the vacuum gap thickness for different practical HfO and SiN insulation layer thicknesses. The thickness of SiN is fixed to 200 nm due to the practical minimal thickness achievable during fabrication, and is further explained in Section IV. The breakdown field is not considered as a limitation in this graph. The thinnest insulation layer shows the closer behavior to the ideal case ($R_F = 1$), as expected. For gap thickness larger than 200 nm, all insulation layers considered achieve $R_F > 0.75$, i.e. the insulation layer material does not make a significant difference for large gaps. However, for small gap thicknesses, 50nm and below, which are important for high frequency applications, the difference is significant. For example, $R_F = 0.64$ and 0.37 for 200 nm thick HfO and SiN, respectively, at a gap of 50 nm, i.e. a 4.75-dB larger electrostatic force is generated by the HfO device than by the SiN device for the same input voltage.

Since a thinner dielectric material corresponds to a larger electrostatic force, one should choose the thinnest possible dielectric layer that can withstand the maximum operating voltage without exceeding the breakdown field of the dielectric. Hence, the thickness of the HfO dielectric (t_d), V_{BD} and $V_{COLLAPSE}$ are considered as optimization parameters in designing CMUTs for maximum electrostatic force for given input voltage during non-collapse transmit mode operation. A specific design example is given in section II-C.

C. Comparison of HfO and SiN Insulation Layers in Receive Mode CMUT Operation

To increase the sensitivity of a CMUT during receive mode operation using a low impedance receiver, the CMUT should be biased close to collapse [37]. Therefore the maximum operating V_{DC} is $V_{COLLAPSE}$ for non-collapsed mode operation, which can be expressed as

$$V_{COLLAPSE} = \sqrt{\frac{8K g_{eff}^3}{27\epsilon_0 A}} \quad (8)$$

where “ K ” is the stiffness of the membrane [38].

The collapse voltage will increase for any fixed vacuum gap if either the thickness of the dielectric increases or the dielectric constant decreases. Thus the advantage of a dielectric with higher κ insulation is a lower collapse voltage for the same insulation thickness as observed from (2) and (8). A lower collapse voltage is advantageous in reducing the maximum DC operating requirements especially in voltage limited situations such as CMUT-on-CMOS integration [39].

Given that η at collapse is

$$\eta_{COLLAPSE} = \sqrt{\frac{3K\epsilon_0 A}{2g_{eff}}}, \quad (9)$$

one can improve the receive sensitivity by reducing g_{eff} using a dielectric layer with a higher κ . However to capture both factors, reduction of collapse voltage and increase in the transformer ratio for a given vacuum gap thickness, one can use the transformer ratio evaluated at collapse and then normalize it to the corresponding collapse voltage itself.

Using a normalization similar to (R_F) in (7), the ratio of the transformer ratio at collapse to the collapse voltage for a given gap and dielectric layer thickness ($\eta_{Norm\_Vcol\_d}$) can be normalized to the case *without* the dielectric layer ($\eta_{Norm\_Vcol\_nd}$). Hence, one can obtain R_η as

$$R_\eta = \frac{\eta_{Norm\_Vcol\_d}}{\eta_{Norm\_Vcol\_nd}} \cdot \quad (10)$$

In Fig. 3, it is observed that the calculated R_η has a similar variation as R_F calculated for the electrostatic force ratio since R_η simplifies to the fractional expression:

$$R_\eta = \frac{(g_0 - x)^2}{(g_0 - x + \frac{t_d}{\kappa})^2} \cdot \quad (11)$$

Similar to Fig. 2, using HfO instead of SiN one can achieve the same maximum receive sensitivity with smaller DC bias, or conversely one can achieve higher maximum receive sensitivity with the same available DC bias. For a typical case of 50-nm gap and 200-nm dielectric layer thickness, the gain will be 4.45dB.

D. Insulation Design for a Practical CMUT

Small gaps, very thin insulation, and high κ values are desirable to obtain better performance. However, practical design limitations such as the breakdown field strength (E_{BD}) of the insulation layer which can withstand at $V_{COLLAPSE}$ needs to be considered. CMUT design constraints such as desired pressure output and center frequency of interest are typically known for the target application. Then design parameters such as the gap, lateral geometry, membrane thicknesses and mechanical properties such as stiffness and mass of the membrane are determined for a particular design. This means that $V_{COLLAPSE}$ is now only a function of t_d of the dielectric in use. Thus, the nature of optimizing t_d becomes an inequality problem since $V_{COLLAPSE}$ is a function of t_d and cannot be greater than $V_{BD} = E_{BD} t_d$ for non-collapse mode CMUT operation, i.e.

$$V_{COLLAPSE}(t_d) < V_{BD}(t_d) \quad (12)$$

To determine the range of acceptable insulation layer thicknesses that are feasible for a particular gap design, the collapse voltage is calculated either with (8) or with the large-signal model used in [2] for higher accuracy to match the breakdown voltage at a particular thickness. As an example, this calculation is performed for HfO layer CMUTs for a $35 \mu\text{m} \times 35 \mu\text{m}$ square membrane. The thickness of SiN above the top electrode varies such that the total membrane material thickness (including HfO) is $2.2 \mu\text{m}$ with Young's modulus of 110

GPa and Poisson's ratio of 0.22. The overall membrane stiffness is estimated using static Finite Element Analysis (FEA) based on average membrane displacement to a uniform pressure on the electrode area of $25 \times 25 \mu\text{m}^2$ and including the effect of the HfO layer. The stiffness (K) is then used in (8) to calculate V_{COLLAPSE} .

By equating the collapse voltages at various gaps to the breakdown voltage of different thicknesses of HfO films, 2 design curves are shown in Fig. 3. Note that an E_{BD} of 4MV/cm for HfO is used to calculate the breakdown voltages of a particular thin film thickness, which is experimentally determined and described in Section III. The difference between the design curves is the method used to calculate V_{COLLAPSE} which is based on: 1) the parallel plate model (curve A in Fig. 3) in (8), and 2) the large-signal model (curve B in Fig. 3) being more accurate in modeling the stiffness of the square membrane which results in higher collapse voltages than the simple parallel-plate equation. Note that the CMUT device should be designed to operate more reliably by accounting for the fabrication inaccuracies which may result in thinner dielectric thickness than expected. This can lead to lower dielectric breakdown voltages than predicted, and can be handled by choosing a design point in the shaded region shown in Fig 3. For example, for a 50-nm gap, choosing a 100-nm-thick HfO satisfies design Curve A with a $R_{\eta} = 0.8$, which already accounts for the underestimated V_{COLLAPSE} based on (8). This is a practical and reliable design point such that the condition (12) is safely kept within bounds even if the fabricated device had a lower quality deposited HfO. The true optimum point for R_{η} performance for $g_0 - x = 50\text{-nm}$ is when HfO $t_d = 42\text{ nm}$ and can be seen when curve B crosses with 50-nm as the x-axis value. The true optimum point gives a marginally better $R_{\eta} = 0.9$ (~10% increase); however, we decided to fabricate at $t_d = 100\text{-nm}$ for a better balance between performance and stability of the HfO layer.

III. Hafnium oxide dielectric Material properties Characterization

For accurate prediction and simulation of the CMUTs using high- κ material such as HfO_2 , κ and E_{BD} should be experimentally characterized. A good prediction of E_{BD} is critical to achieve electrical reliability and the thinnest possible thickness for the dielectric layer.

To calculate κ and measure E_{BD} of the HfO thin film, test capacitors on a copper bottom and aluminum top electrodes were fabricated. Copper was chosen for the bottom electrode due to the material's low resistivity and the process similarity to the growth of HfO on copper sacrificial layer during the CMUT fabrication process [40]. Since the nucleation rate of HfO may differ on various material surfaces, affecting its thickness per cycle of deposition [41], the HfO film on top of a copper bottom electrode was characterized to best replicate the surface conditions used in the CMUT fabrication process. Both top and bottom electrodes are 1300 Å and a 50-nm HfO dielectric layer was deposited using a Cambridge Nanotech Fiji F202 system at 250°C. The thickness of the ALD film was measured with a Woollam M-2000 ellipsometer, with a recipe that was calibrated for the specific copper layer that the HfO was deposited on. A mean squared error (MSE) of 27.5 Å and an average refractive index of 2.06 was measured for the HfO thin film on top of sputtered copper which is close to literature values [42]. A Fluorine based Reactive Ion Etching (RIE) recipe (discussed in

Section IV) was used to etch open the area over the bottom electrode copper bond pads used for external electrical characterization.

The capacitance of the test capacitor, measured using a standard probe station and Agilent B1500 Semiconductor Analyzer (Santa Clara, CA), is shown in Table I, where other capacitor parameters are also summarized. The average capacitance value over 10 capacitor measurements was used to calculate the average dielectric constant of the HfO based on 50-nm thickness and designed capacitor electrode surface area. The variation in capacitance measured can be due to the non-uniformity of the actual HfO thickness deposited. A typical C-V measurement was obtained by sweeping between -15 V to $+15$ V with a 0.3 V step. The AC voltage level applied was at 0.25 V while the frequency of the AC signal was held at 100 kHz. All measurements were carried out at room temperature.

IV. Fabrication of CMUT with Hafnium Oxide Insulation Layer

The fabrication method used in this investigation is similar to that of the low temperature silicon nitride process previously described in Knight, *et al.* [7] and will be summarized in this paper along with the new steps. The novel steps including the HfO insulation layer and using a copper sacrificial layer, will be discussed in greater details, are schematically described in the CMUT fabrication process flow shown in Fig. 5.

Starting with a $4''$ $\langle 100 \rangle$ silicon wafer, a $3 \mu\text{m}$ thermal oxide is grown for passivation from the substrate. A 120 nm layer of Chromium is then sputtered and patterned to form the bottom electrode of the CMUT. After this step, 50 nm of copper is sputtered and patterned for the sacrificial layer (further the vacuum gap layer). Both electrodes are sputtered with the Unifilm DC Sputterer and achieved high thickness uniformity over the entire wafer. The gap thickness and its uniformity are critical since it affects the CMUT device performance, such as collapse voltage and pressure output for the given input voltage. Both layers of patterning were achieved by using Shipley SPR 1813 photoresist (Torrance, CA). The chromium is wet etched via CR-7S Chromium etchant (Hollister, CA) and the copper by Copper APS 100 (Danvers, MA) diluted at 1:60 with deionized (DI) water. Both etchants etched in the range of $4\text{--}8 \text{ \AA/s}$ at room temperature. Chromium was chosen as the bottom electrode because the copper etchant does not etch chromium, and thus is suitable for selectivity when patterning the sacrificial layer without the need to introduce an extra dielectric passivation layer in between. Then, a 100-nm layer of HfO is grown uniformly across the surface of the substrate at 250°C to form the top dielectric insulation. The thickness of this insulation is designed to operate near V_{COLLAPSE} without exceeding the threshold of V_{BD} as discussed in Section III. For the HfO CMUT device, operating at about 15 MHz center frequency, the thickness of the insulation is designed as 100 nm. This is not the optimum thickness for this particular device configuration, however it is also a safe thickness for other devices that work at higher frequencies fabricated on the same wafer. The ALD recipe parameters used in HfO deposition are summarized in Table II. The precursor used in this study is Tetrakis (Dimethylamido) hafnium (IV) (TDMAHf) along with Cambridge Nanotech's Fiji F202 ALD system. For the SiN insulation layer CMUT device, a thickness of 200 nm was deposited instead of HfO. In order to avoid material defects such as pin-hole effects and voids in the SiN thin film, we did not deposit below this thickness for the particular low

stress PECVD recipe. Pin-hole and void like defects can adversely affect both mechanical and electrical properties of the SiN material.

In order to minimize the oxidation of the copper sacrificial layer which can introduce additional surface roughness, the substrate is loaded onto the ALD chuck at 25–35°C in the load lock area and subsequently reduced to a vacuum pressure of 0.5 Torr range before entering the main ALD deposition chamber. Due to the vacuum environment inside the ALD chamber, oxidation rate is very slow at 250 °C. The average growth rate observed is 1.15 Å/cycle and an average of 10–20 cycles is needed before nucleation of the first layer of hydroxyl groups forms to create the first molecular layer of HfO on top of the copper sacrificial layer. To control this slight delay in nucleation is challenging, and thus it is accepted as a small source of error when measuring the deposition rate within the first 100 cycles.

To form the top electrode, a 300 nm layer of AlSi 1% is evaporated and patterned through lift-off. AlSi is chosen due to its good adhesion, relatively high electrical conductivity and linear thermal coefficient similar to that of copper ($22 \times 10^{-6}/^{\circ}\text{C}$ for AlSi versus $16.7 \times 10^{-6}/^{\circ}\text{C}$ for copper). The similarity in coefficient of thermal expansion (CTE) between the aluminum and copper helps with reducing thin film stress and peeling of the top electrode. After depositing 1 μm of SiN for the membrane formation, small release holes are drilled via RIE to the copper sacrificial layer to allow copper etchant APS 100 to come in for a wet release. A separate sulfur hexafluoride (SF₆) chemistry was also used to etch the HfO layer compared to the standard CHF₃ chemistry used to etch SiN. Etching rates of 5 nm/min and 58 nm/min are observed for the release hole etching in HfO and SiN, respectively. After the release, the wafer is placed back into the PECVD for sealing at 900 mTorr and further thickening to a desired 2.2 μm total thickness. A final step of opening the electrical bond pad connections for testing is needed via RIE. The test array geometry parameters are summarized in Table III.

V. CMUT characterization and comparison

To compare the performance of CMUTs with HfO and SiN, insulation layers, CMUT elements with identical geometry and 50-nm vacuum gap were fabricated by the method described in Section IV. The only difference between these wafers is the method followed for the formation of dielectric insulation. The HfO and SiN thicknesses are 100 nm and 200 nm, respectively. The device geometry for the comparing test arrays are summarized in Table III and the fabricated CMUT devices are shown in Fig. 6.

Both devices are diced from the main substrates and secured side by side to the same PCB testing board for wirebonding of the bond pad connections. A 3-μm layer of parylene-C is coated over the devices, exposed wirebonds and PCB traces and the devices are submerged for acoustical characterization in water. With the 2 devices side by side on the same PCB, physical setup variations such as alignment changes to the hydrophone are minimized to achieve a reliable comparison study.

A. Transmit Performance Characterization and Comparison

Both devices were measured in the same setup using the same pulser. A 28-ns unipolar pulse generated by a custom design pulser excited the transducers and the transmitted pressure was measured with a hydrophone (HGL0085, ONDA™, Sunnyvale, CA).

The pulse amplitudes were increased to a point which maximizes the output peak-to-peak pressure observed by the hydrophone, meaning the full gap swing of the membrane. The spectra of the received signals were also monitored to make sure that the devices operated in the non-collapsed mode. No DC bias was applied with this short pulse to achieve maximum output pressure with full-gap swing [2]. Pulse amplitudes of 32 V and 60 V were found to reach maximum output pressure for HfO and SiN insulation devices respectively. Note that the collapse voltages of the devices were 21V and 42V for HfO and SiN insulation devices respectively. Therefore, the devices needed to be driven 50% higher than their collapse voltages for full swing operation with this particular pulse width. The hydrophone outputs from the devices at the maximum pressure points are shown in Fig. 7. The pressure output signals are very similar in shape as well as amplitude, meaning that both devices are fabricated with good uniformity and could be used for a fair performance comparison. The same peak output pressure measured on the hydrophone shows that both devices achieved full gap swing. The frequency responses are similar with a center frequency of 16.5 MHz.

The detailed comparison of the transmit mode performance is depicted in Fig. 8, which plots the hydrophone output voltage as a function of the pulse amplitude. A nonlinear dependence of the output pressure to input pulse amplitude is observed. As expected, both devices reach the same maximum pressure which is limited by the vacuum gap thickness. However, the CMUT with the 100nm HfO layer reaches maximum pressure with a 32V pulse whereas a 60V pulse is required for the CMUT with 200-nm SiN layer. Therefore, there is ~2 times improvement in transmit sensitivity with no DC bias case. This is in reasonable agreement with the simple parallel plate model prediction in Fig. 2.

B. Receive Performance Characterization and Comparison

To compare receive performance of CMUT elements, a 15-MHz piezoelectric transducer was used as a transmitter. The CMUT elements were connected to a Panametrics Pulser/Receive (Model 5072R, Waltham, MA, 500 Ω input impedance) using a coaxial cable with 60 pF capacitance (180 Ω impedance magnitude at 15 MHz). We note that the impedance magnitude of both SiN and HfO CMUTs due to their active capacitance and parasitic capacitances from wirebonding are greater than 5 k Ω . The effective receiver impedance magnitude resulting from the receiver input, and parasitics due to the cable and wirebonding is ~130 Ω . This is a low impedance termination for the CMUT, as considered in the simplistic calculations shown here, compared to an open circuit termination. During the measurements, both CMUT elements were centered with respect to the piezoelectric transducer and absolute transmitter-receiver distances were kept the same. Fig. 9 shows the received signal amplitude while the DC bias voltage is varied from 0 V up to each CMUT's collapse voltage.

Two important conclusions can be made about the receive performance. First, the 100-nm HfO insulation device has half the collapse voltage of the 200-nm SiN device. This is desirable since this will allow operation of the CMUT close to collapse at lower voltages. Second, the maximum receive signal from the HfO device is ~ 2.2 times that of the SiN device at collapse, indicating an absolute gain in receive signal level with low impedance termination. When normalized to the collapse voltage of each CMUT, there is about 4 times improvement in the receiver performance. Although this is not a direct validation of the simplistic analysis results, it is in reasonably good agreement with the trend indicated in Fig. 3, especially considering that the gap is reduced and there is significant membrane curvature very close to membrane collapse.

C. Preliminary Stability Testing of HfO insulation layer

An initial test was performed to observe the stability of the HfO insulation layer under high electric field during operation. The device tested was a 23 MHz center frequency CMUT with 100 nm HfO insulation. The CMUT was biased at 35 V (88% of $V_{collapse}$) while a piezoelectric transducer is used as the transmitter. Due to the particular mask design, the DC bias was applied directly on the HfO film, without a vacuum gap, in many locations resulting in an electric field strength of 3.5 MV/cm. Therefore, during the ~ 4 hour long test the HfO film was under significant electric field, corresponding to 88% of the E_{BD} . Fig 10 shows that the peak-to-peak received signal from the CMUT had a standard deviation of 3.7% from the mean. Since this variation is less than 0.3 dB, this initial measurement shows that the CMUTs with HfO insulation layers are stable at least for short term use.

VI. Conclusion

We investigated the performance improvement of ALD high- κ insulation layers in CMUTs using a simple parallel plate model. As an example, we used HfO as compared to the PECVD Si_xN_y insulation used in low temperature CMUT fabrication. Theoretical and experimental characterization of HfO₂ insulation CMUTs demonstrated significant advantages especially for vacuum gaps below 100 nm. Switching to ALD deposited HfO₂ can also allow low temperature fabrication of insulation layers with thickness below 100 nm without compromising the quality of the film as compared to PECVD Si_xN_y . Experiments on 16.5 MHz CMUTs with 100-nm HfO and 200-nm SiN insulation layers show that maximum transmit voltage requirement is reduced by one half for the same 50-nm vacuum gap device. The receive output is improved by 2 times with low impedance termination while reducing bias voltage requirements by one half. Integration of the low temperature ALD HfO₂ material into the CMUT-on-CMOS fabrication process is currently underway.

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Fig. 1.
A Schematic of a single CMUT membrane modeled as a 1D mass-spring-damper parallel plate.

Fig. 2.

A plot of normalized electrostatic force (R_F) for the same input pulse between HfO vs. SiN insulation device as a function of vacuum gap. $\kappa = 16$ and 6.3 for HfO and SiN respectively used.

Fig. 3.

A plot of the ratio of transformer ratios normalized to the collapse voltage R_η for HfO and SiN insulation CMUTs compared to the ideal case of parallel plate with no insulation. Design Curve A is based on V_{COLLAPSE} calculated from (8) and Design Curve B is based on V_{COLLAPSE} calculated from a large signal model. E_{BD} of HfO used in calculation is 4MV/cm. Shaded area is acceptable design space.

Fig. 4.
I-V curve for test capacitor with 50 nm of HfO as dielectric layer.

Fig. 5. CMUT fabrication process flow with copper sacrificial layer and HfO top insulation layer.

Fig. 6.

(a) A Micrograph of the test CMUT device. Both test cases are identical in lateral geometry size. Only one test device is shown above. There are 4 elements per device (b) Close-up view of 1 element with 4 membranes.

Fig. 7.
 (top) Transient pressure waveforms from test devices, (bottom) Frequency response comparison of test devices showing fabrication uniformity that is suitable for a fair performance comparison.

Fig. 8.

Experimental hydrophone data comparing the Tx between the two types CMUTs. HfO_2 device can achieve the same maximum pressure output with half the input voltage compared to Si_3N_4 .

Fig. 9.

Experimental CMUT receive data comparing the Rx sensitivity of the 2 CMUTs. HfO device can achieve ~2.2 times the receive voltage using half the DC voltage compared to SiN.

Fig. 10.
Stability test with piezoelectric transducer transmitting and CMUT receiving.

TABLE I Test Capacitor Parameters and average κ value

Parameter	Value
Electrode Area	$3.469\text{e-}7 \text{ m}^2$
HfO ₂ film thickness	50 nm
Measured Capacitance	0.86 – 1.1 nF
K	16 (+/-2)

TABLE IIALD HFO₂ Recipe Parameters

Parameter	Value
H ₂ O Pulse Time	0.6s
H ₂ O Pulse Pressure Peaks	700mTorr
Purge Time	10s
TDMAHf Pulse Time	0.25s
TDMAHf Pulse Pressure Peaks	200mTorr
Purge Time	10s
Substrate Temperature	250°C
Pre-cursor Jacket Temperature	75°C

TABLE III

Test Array Geometry Parameters

Parameter	Value
Membrane Size	35×35 μm
Top Electrode Size	25×25 μm
Vacuum Gap	50 nm
Si_3N_4 Membrane Thickness	2.0–2.1 μm
HfO_2 Insulation Thickness	100 nm
Si_3N_4 Insulation Thickness	200 nm
No. of Membranes per element	4
No. of Elements per device	4
Total No. of Membrane per device	16