Design and fabrication of a perpendicular magnetic tunnel junction based nonvolatile programmable switch achieving 40% less area using shared-control transistor structure

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A compact nonvolatile programmable switch (NVPS) using 90 nm CMOS technology together with perpendicular magnetic tunnel junction (p-MTJ) devices is fabricated for zero-standby-power field-programmable gate array. Because routing information does not change once it is programmed into an NVPS, high-speed read and write accesses are not required and a write-control transistor can be shared among all the NVPSs, which greatly simplifies structure of the NVPS. In fact, the effective area of the proposed NVPS is reduced by 40% compared to that of a conventional MTJ-based NVPS. The instant on/off behavior without external nonvolatile memory access is also demonstrated using the fabricated test chip. © 2014 AIP Publishing LLC.

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I. INTRODUCTION

A field-programmable gate array (FPGA) using a nano-scale CMOS process is quite attractive hardware because of its low volume cost as well as fast turn around time.¹ However, standby power dissipation due to leakage current² has been the largest obstacle for the advancement of the FPGA. The implementation of a nonvolatile FPGA, wherein all the stored data remain in the nonvolatile devices even if the power supply is cut off, is one promising way of completely eliminating wasted standby power.³⁻¹² Because a magnetic tunnel junction (MTJ) device has attractive features such as 3D-stacking capability, scalability, and virtually unlimited endurance (over 10^{16} cycles),^{13,14} it is a viable candidate for realizing a Nonvolatile FPGA (NVFPGA), and fundamental logic components of the NVFPGA have been proposed.⁷⁻¹² On the other hand, it is also important to implement a compact nonvolatile programmable switch (NVPS) that is composed of an NMOS pass switch together with a nonvolatile storage element and used for signal routing in the FPGA. However, a conventional MTJ-based NVPS tends to be large because the nonvolatile storage element requires large write-control transistors for supplying sufficient bi-directional write current through MTJ devices.^{8,15}

In this paper, a compact NVPS is fabricated using 90 nm CMOS technology together with perpendicular-MTJ (p-MTJ)

devices.¹³ Because routing information does not change frequently once it is programmed into an NVPS, high-speed read and write access is not required, which greatly simplifies the structure of the NVPS. Moreover, because a large-sized transistor for driving sufficient write current is shared among all the NVPS, the effective size of two write-control transistors in each NVPS can be minimized. In fact, the effective area of the proposed NVPS is reduced by 40% in comparison with a conventional MTJ-based NVPS.

II. NONVOLATILE PROGRAMMABLE SWITCH USING SHARED-CONTROL-TRANSISTOR STRUCTURE

Figure 1(a) shows a cross-sectional view of the fabricated CoFeB/MgO p-MTJ device having an effective junction size and a tunnel-barrier thickness of 75 nm^2 and 1.0 nm , respectively. The resistance value (R_M) is R_P if the p-MTJ device is in a parallel state (P), while it becomes R_{AP} and in an anti-parallel (AP) state. Additionally, the stored data $M = 1$ corresponds to $R_M = R_P$ and $M = 0$ corresponds to $R_M = R_{AP}$, respectively. Figure 1(b) shows a typical measured R - I curve of the fabricated p-MTJ device. We can see that two distinct resistance values $R_P = 6 \text{ k}\Omega$ and $R_{AP} = 12 \text{ k}\Omega$ are obtained by applying write current $I_{AP-P} = 50 \text{ }\mu\text{A}$ or $I_{P-AP} = -80 \text{ }\mu\text{A}$.

Figure 2 shows the overall structure of the routing block for the NVFPGA, in which NVPSs are used for signal routing from/to the logic block. To reduce the effective area of

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FIG. 1. Fabricated p-MTJ device: (a) Cross-sectional view. The effective junction size is 75 nmφ and the thickness of the MgO barrier is 1.0 nm. (b) R-I characteristic of the fabricated p-MTJ device.

FIG. 2. Overall structure of the proposed routing block for the NVFPGA.

the routing block, control transistors are shared among all the NVPSs. Figure 3 shows a schematic diagram of the proposed NVPS. The output of nonvolatile storage element (Q) is used for turning on/off the NMOS pass switch. The nonvolatile storage element consists of a sense amplifier using two inverters and two local write control transistors together with two p-MTJ devices, in which routing information is programmed in a complementary fashion. The sense amplifier is used for reading stored state M and keeping it as Q during the power-on state without creating a steady DC current path. Because they do not change once configuration data are programmed into the NVPS, no additional control transistor is required.

Figure 4 shows the configuration scheme of the proposed NVPS where $M = 1$ and $M' = 0$ are stored into p-MTJ devices. When STR, STRC, and BL are activated high,

FIG. 3. Schematic diagram of the proposed NVPS.

FIG. 4. Configuration scheme of the proposed NVPS.

parallel current paths are created and I_M and I'_M flow through R_M and R'_M , respectively. In this case, I_M is larger than switching current I_{AP-P} and the state of R_M becomes the P state. Then I'_M exceeds switching current I_{P-AP} and the state of R'_M changes to the AP state. After the configuration, the states are loaded by the sense amplifier. The read-control transistor is implemented with a small feature size compared to that of write-control one, which enables the avoidance of read disturbance, wherein data are accidentally written into an MTJ device while reading. Note that the proposed configuration scheme is performed under a standard CMOS supply voltage, and no special transistor is required. By tuning the gate width of the write-control transistors, we can control appropriate write current for the proposed configuration scheme.

III. EVALUATIONS

Figure 5(a) shows a die photo of the fabricated test chip using 90 nm CMOS technology together with p-MTJ devices. The p-MTJ devices are stacked over the 4th metal layer. The shared-control transistors are located at the right side of the NVPS array. Figure 5(b) shows the measured waveform of the fabricated test chip. We can confirm that configuration data “0” (turn off NMOS pass switch) and “1” (turn on

FIG. 5. Fabricated test chip using 90 nm CMOS/75 nm MTJ technologies: (a) Die photo. (b) Measured waveform.

FIG. 6. Area comparison.¹⁶ R_P , R_{AP} , I_{P-AP} , and I_{AP-P} used for the circuit design are based on measurement results as shown in Fig. 1(b).

NMOS pass switch) are stored into the nonvolatile storage element in the NVPS by utilizing the shared-control transistor, and they are recalled after power-on successfully.

Figure 6 summarizes the area comparison.¹⁶ The area of NVPS using Ref. 8 is the largest among the three because a bi-directional write current must be applied simultaneously to the series connected p-MTJ devices. By utilizing a two-step MTJ configuration, the area of the NVPS using Ref. 15 becomes smaller than that of the previous one. However, there are wasted control transistors in terms of the NVPS. Moreover, it is somewhat difficult to explore design space between reading and writing properties because the reading and writing functions are merged into the same circuit. In contrast, the proposed NVPS is implemented in the smallest area by removing all the wasted functions and sharing a portion of the read/write-control transistors. Moreover, we can optimize reading properties and writing one of the proposed circuit independently using pseudo three-terminal structure. Note that the effective voltage applied to a p-MTJ device is lower than 0.63 V, which is much lower than both breakdown voltage and back-hopping one.^{17,18} While I_M (or I'_M) when a p-MTJ device is AP state is decreased as the tunnel magnetoresistance ratio (TMR) is increased, the proposed NVPS can drive sufficient write current even if TMR reaches 200%, which is sufficiently high for reading (the applied voltage to a p-MTJ device is lower than 0.69 V).

IV. CONCLUSIONS

A compact NVPS is presented for an MTJ-based NVFPGA. By removing all the wasted control circuits and

utilizing a shared-control transistor structure, the effective area of the NVPS can be minimized. For the next objective, it is very important to discuss how to determine the granularity of shared-control transistor for both an area and time efficient configuration scheme.

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