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A Low-power CMOS BFSK Transceiver for Health Monitoring Systems

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Abstract

A CMOS low-power transceiver for implantable and external health monitoring devices operating in the MICS band is presented. The LNA core has an integrated mixer in a folded configuration to reuse the bias current, allowing high linearity with a low power supply levels. The baseband strip consists of a pseudo differential MOS-C band-pass filter achieving demodulation of 150kHz-offset BFSK signals. An all digital frequency-locked loop is used for LO generation in the RX mode and for driving a class AB power amplifier in the TX mode. The MICS transceiver is designed and fabricated in a 0.18 μ m 1-poly, 6-metal CMOS process. The sensitivities of –70dBm and –98dBm were achieved with NF of 40dB and 11dB at the data rate of 100kb/s while consuming only 600 μ W and 1.5mW at 1.2V and 1.8V, respectively. The BERs are less than 10^{-3} at the input powers of –70dBm at 1.2V and –98dBm at 1.8V at the data rate of 100kb/s. Finally, the output power of the transmitter is 0dBm for a power consumption of 1.8mW.

I. Introduction

Several implantable devices enabling medical telemetry have recently been appearing in both commercial product lines [1] and research archives [2–6]. Implantable wireless health care systems, however, have faced a technical challenge associated with battery life. They last over several years (~5 years) inside the human body without the possibility of recharging or replacing, which in turn requires the architectures of medical implants to be simplified as much as possible while being optimized to dissipate as little power as possible with reasonable performance. Various techniques have been proposed to deal with reducing power associated with telemetry circuits of medical implants. A digitally controlled oscillator (DCO) using a sub-ranged, pre-distorted capacitor array is incorporated into the loop antenna as its inductive element [3]. This approach achieves a wide tuning range, linear digital-to-frequency conversion, and high frequency resolution. The unified transceiver concurrently operating in both MICS and BCC bands is introduced in [4], in which the on-body controller positions on a patient's skin allowing for the minimum detectable power of about –70dBm with sub-mW power dissipation. In [5], reconfigurable Radio Frequency (RF) front end contributes to the simplification of the transceiver architecture with an all-digital frequency-locked loop (ADPLL). A transceiver based on injection locking and frequency multiplication was presented in [6].

In this paper, an energy efficient receiver chain operating in MICS band (402 ~ 405MHz) with a binary frequency shift keying (BFSK) modulation is proposed. The folded LNA-Mixer is used as the RF front-end of the receiver to detect BFSK signals while achieving low power consumption. The MOS-C band-pass filter (BPF) filters out down-converted BFSK signals, followed by a continuous comparator generating a demodulated digital

waveform. The rest of the paper is organized as follows: Section 2 provides the transceiver architecture. Details on building blocks are provided in section 3. Section 4 presents main experimental results. Finally, conclusions are drawn in section 5.

II. Transceiver architecture

Fig. 1 shows the receiver architecture which consists of a folded low-noise amplifier (LNA) and mixer, band-pass filter (BPF) and comparator. A MICS transceiver usually adopts either on-off keying (OOK) [2] or binary frequency shift keying (BFSK) modulation [3–5] for an energy efficient design. The proposed RX chain adopts direct conversion BFSK modulation with the 150kHz offset because it offers better performance against interference than OOK [5]. The transmitter consists of an ADPLL and class AB power amplifier. The ADPLL operates as a MICS direct modulator in the RX mode and drives a class AB power amplifier for a nonlinear output amplifier in the TX mode.

An LNA is merged with the mixer in a folded configuration reusing the bias current. A typical MICS transceiver employs a passive mixer requiring a buffer stage to drive a transimpedance amplifier at the expense of extra current consumption [5]. The proposed LNA-Mixer configuration doesn't require a buffer stage reducing overall front-end power. The amplified, down-converted BFSK signals are filtered out by a MOS-C based G_m -C BPF with the center frequency of 150kHz [7]. A BPF is used here to relax the requirements of the DC offset and flicker noise instead of a low-pass filter (LPF) usually adopted in MICS RX chains. OTA-based G_m -C filters are widely used in conventional MICS RX chains at the expense of extra current consumption due to the common-mode feedback network (CMFB) to handle the effect of common-mode perturbations. A MOS-C based G_m -C BPF is pseudo differential, therefore a separate CMFB network is not necessary and it finally leads additional reduction in power consumption. Following the pseudo differential BPFs at I and Q channels, the continuous comparators convert filtered BFSK signals into digital waveforms with phase delay or lag by 90° to recognize a symbol type of detected signals.

III. Low-power Strategies

A. Folded LNA-Mixer

Fig 2 shows the detailed schematic of the proposed fully differential folded LNA and mixer. The mixer is merged into common-gate (CG) LNA to reuse the bias current and the amplified input signals through the CG-LNA are converted into voltage quantities through the down conversion by the folded quadrature mixers. The folded configuration of the proposed LNA-Mixer allows for high linearity in a wide range of power supply. The cross-coupled capacitors (C_C) are inserted between gates and sources of devices M_1 and M_2 to increase the effective transconductance (G_{eff}) of GC-LNA with low DC bias currents [8].

The small signal resistance looking into M_1 – M_3 and M_2 – M_4 is much larger than that of a load of the LNA so that contribution of the load resistance to the input matching can be ignored. The small-signal half circuit model is drawn in Fig. 3 and the input matching is analyzed as the following.

$$Z_{IN} = sL_{IN} + \frac{1}{sC_{IN}} + \frac{sL_S}{sL_S(sC_S + G_{eff}) + 1} \quad (1)$$

At the resonant frequency, the imaginary part of the input impedance is cancelled and Eq. 2 becomes

$$R_{IN} \approx \frac{1}{G_{eff}} \quad (2)$$

$$G_{eff} = (1 + C_C / (C_C + C_{gs1,2})) g_{m1,2} \quad (3)$$

In equations above, L_{IN} is the inductor and C_{IN} the capacitor of the external matching network. L_S is the source degenerated inductor and $g_{m1,2}$ is the transconductance of the input pair. Lastly, C_C is the cross-coupled capacitors for enhancement in the effective transconductance of the LNA and $C_{gs1,2}$ is the gate-source capacitance of the input transistors, M_1 and M_2 .

B. Pseudo-differential BPF

In this design, pseudo differential all MOS-C based G_m -C BPFs are used to take both power efficiency and simple realization of ICs into account at the expense of mismatches in I and Q channels due to the absence of the CMFB network. The G_m -C integrator is realized by a transconductor M_1 , capacitor C_1 , and a bias device M_4 as shown in Fig. 4. Source degenerated devices, $M_4 - M_6$, are placed to enhance immunity to non-linearity [9].

C. All Digital Frequency-Locked Loop

A conventional PLL is not suitable for implantable devices operated by a single battery. Reduction in power consumption in a TX is achieved by employing an ADFLL consisting of a type-I phase-locked loop (PLL) scheme as shown in Fig. 1 [10]. The features of the ADFLL are (i) all-digital implementation, (ii) programmable loop bandwidth, and (iii) fast locking. The ADFLL operates as a MICS direct modulator in the RX mode and drives a class AB power amplifier for a nonlinear output amplifier in the TX mode. An LC-VCO is fully implemented for the better phase noise. The output power is about 0dBm.

IV. Measurement Results

The MICS transceiver was fabricated in a $0.18\mu\text{m}$ 1-poly, 6-metal CMOS process and the active chip area is 9mm^2 . The microphoto of the chip is shown in Fig 5. The LNA+MIX consumes $480\mu\text{W}$ from 1.2V power supply while the RX chain dissipates $600\mu\text{W}$ from a 1.2V power supply. The NF is less than 40dB at 1.2V achieving the minimum detectable signal level of -70dBm [4,5]. This sensitivity is acceptable power level when the implanted devices communicate with an on-body controller within the limited communication range ($\sim 1\text{m}$) [4]. The return loss of the folded LNA-Mixer at various power consumptions is measured as shown in Fig 6. The NF and voltage gain at various power consumptions are displayed in Fig 7. The achieved voltage gain of the folded LNA-Mixer and RX chain are 35dB and 51dB at the power supplies of 1.2V and 1.8V, respectively, while 11dB and 14.6dB for the folded LNA-Mixer at the same power supplies. The average NF is about 40dB and 11dB at 1.2V and 1.8V, respectively which means, in other words, the minimum detectable signal powers are -70dBm and -98dBm at 1.2V and 1.8V, respectively. Fig 8 shows measured digital waveforms at I and Q with 150kHz-offset BFSK RF signals with the carrier frequency of 400MHz at the input power of -85dBm . I channel leads Q channel by 90° when +150kHz-offset RF signal is detected at the front-end of the receiver chain and I lags Q by 90° in -150kHz -offset. Fig 9 shows the phase noise performance at various control voltages. Finally, the performance of the receiver chain is summarized in Table I.

V. Conclusions

A low-power CMOS transceiver for the MICS band has been fabricated and measured. The folded LNA-Mixer configuration and MOS-C based G_m -C BPF allow for a low-voltage and low-power operation under the limited power capacity. The RX chain shows -98dBm sensitivity with a 100kb/s and consumes only 1.5mW from a 1.8V power supply while shows -70dBm sensitivity and $600\mu\text{W}$ from a 1.2V power supply. This work demonstrates that implantable wireless devices such as Pacemakers consuming a sub-mA with reasonable performance can be designed.

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Figure 1.
MICS Transceiver Architecture

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Figure 3.
Small-signal half circuit model of the proposed LNA for input matching

Figure 4.
Schematic of the MOS-C BPF

Figure 5.
Microphoto of MICS chip Experimental results

Figure 6.
Measured S_{11}

Figure 7.
Measured Noise Figure & Voltage Gain

Figure 8.
Measured RX digital waveforms at I and Q channels at -85 dBm with 150kHz offset BPSK
(i) +150kHz offset (ii) -150 kHz offset at 400MHz carrier frequency

Figure 9.

The phase noise of ADFLL at various control voltages of 0.6, 1.2, and 1.8V.

TABLE I**SUMMARY OF THE TRANSCEIVER**

Technology	0.18 μ m 1-poly, 6-metal CMOS
Operating Frequency	402MHz – 405MHz
Modulation	BFSK
Data Rate	100 kb/s
Sensitivity @ 10 ⁻³ BER	-70 dBm @ 1.2V (NF = 40 dB) -89 dBm @ 1.5V (NF = 20 dB) -98 dBm @ 1.8V (NF = 11 dB)
Supply Current	500 μ A @ 1.2V 630 μ A @ 1.5V 840 μ A @ 1.8V
Voltage Gain, RF+BB	35 dB @ 1.2V 44 dB @ 1.5V 51 dB @ 1.8V
Voltage Gain, LNA+Mixer	11 dB @ 1.2V 14.3 dB @ 1.5V 14.6 dB @ 1.8V