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New silicon technologies enable high-performance arrays of Single Photon Avalanche Diodes

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Abstract

In order to fulfill the requirements of many applications, we recently developed a new technology aimed at combining the advantages of traditional thin and thick silicon Single Photon Avalanche Diodes (SPAD). In particular we demonstrated single-pixel detectors with a remarkable improvement in the Photon Detection Efficiency at the longer wavelengths (e.g. 40% at 800nm) while maintaining a timing jitter better than 100ps.

In this paper we will analyze the factors that currently prevent the fabrication of arrays of SPADs by adopting such a Red-Enhanced (RE) technology and we will propose further modifications to the device structure that will enable the fabrication of high performance RE-SPAD arrays for photon timing applications.

Keywords

Single-Photon Avalanche Diode (SPAD); Photon Detection Efficiency (PDE); Time Correlated Single Photon Counting (TCSPC); Enhanced Photon Detection Efficiency; Red-Enhanced SPAD; RE-SPAD; SPAD arrays; Photon Counting

1. INTRODUCTION

A significant breakthrough in the field of single photon detection is represented by the recent introduction of a silicon SPAD, namely Red Enhanced SPAD (RE-SPAD)^{[1], [2]}, capable of attaining a good Photon Detection Efficiency (PDE) in the near infrared range (e.g. 40% at a wavelength of 800nm) while maintaining a remarkable timing resolution of about 100ps FWHM. Such a detector overcomes the limitations that are typical of classical thin^[3] and thick^[4] SPADs; in particular, the formers attain a limited PDE at longer wavelengths (e.g. 15% at a wavelength of 800nm), while the latter suffer of a poor photon timing jitter of many hundreds of picoseconds FWHM. The use of such devices has already proved to be remarkably advantageous in a few applications^{[5], [6], [7], [8]} and we expect many more demonstrations to come in a near future for fields ranging from single molecule analysis to quantum key distribution.

On the other hand, many single-photon techniques either cannot be implemented by using single pixel detectors, or would greatly benefit from the use of arrays with at least a small number of pixels. Significant examples are, for instance, parallel Fluorescence Correlation Spectroscopy (parallel FCS)^{[9], [10]}, high-throughput Single Molecule Analysis^[11], or spectrally resolved Fluorescence Lifetime Imaging (sFLIM)^[12]. Although many of such techniques would take advantage of an improved PDE, especially in the near-infrared range, no arrays exist that provides such a feature. In particular, thick SPAD technology is non-planar and therefore not suitable for the monolithic integration of more than one device on a single chip^[13]; as opposite, high-voltage CMOS technology allows the fabrication of arrays of SPADs with a large number of pixels (e.g. 32×32)^{[14], [15]} but at the expense of a strong limitation in the attainable PDE, especially at the longer wavelengths (e.g. 7% at 800nm^[14]). More scaled CMOS technologies allow even large arrays^[16] (e.g. 160×128), with more electronics integrated on the same chip of the detector, but with a significant degradation in the performance of the SPAD. A solution somewhere in between thick SPAD and CMOS SPAD is represented by thin SPAD fabricated by using a custom technology; actually, by using this technology is possible to fabricate small arrays of detectors^{[17], [18]} (e.g. 60-elements, or 8×1-elements) with overall good pixel performance. However their PDE at longer wavelengths (about 15% at a wavelength of 800nm) is somehow limiting in many applications. Finally, single photon detection on a small number of pixels can be achieved also by using multi-anode PMTs; however, besides suffering of all the limitations typical of vacuum-tube devices, their near-infrared PDE is even more limited^[19].

In order to overcome the aforementioned limitations, RE-SPAD technology has been conceived from the scratch to be compatible with the fabrication of arrays^[20]. In particular, the device structure has been designed to be manufactured by using a planar technology. Nevertheless, some crucial technological issues are still to be addressed in order to attain a fully operating array of RE-SPAD.

In this paper we will therefore examine which are the requirements that a SPAD structure must fulfil to enable arrays fabrication, either for photon counting and photon timing applications; then we will discuss the limitation of RE-SPAD structure and we will analyse technological solutions to overcome them.

2. THIN SPAD: STRUCTURE AND ARRAYS' IMPLEMENTATIONS

In this section we will briefly review the structure of a thin SPAD and we will analyse the role of different device regions in making possible the fabrication of SPAD arrays, either for photon counting or photon timing. In particular Figure 1 represent the typical structure of a double epitaxial SPAD^[21] developed at Politecnico di Milano and manufactured in collaboration with CNR-IMM in Bologna. The device is fabricated starting from an n-type substrate on top of which a p-type epitaxial layer has been grown. The latter is composed of two different regions, respectively a p⁺ *buried layer* and p⁻ *quasi-intrinsic* layer. During following fabrication steps, mainly four regions are manufactured: the *isolation*, the *sinker*, the *shallow n* and the *enrichment*. As suggested by its name, *shallow n* is an n-type, thin diffusion that constitutes the cathode of the device. The *enrichment* is a medium thickness, p-type region that has a two-fold purpose: on one hand, the enrichment region is needed in

order to reduce the breakdown value in the central region of the device, thus avoiding premature edge breakdown; on the other hand, its doping profile is designed in order to suitably shape the electric field in the multiplication region, with the aim of optimizing device performance^[22]. Although not belonging to the active region, the *isolation* and the *sinker* have, nevertheless, an important role in assuring the proper operation of the device, either as a single pixel or as an element of an array. In fact, the *sinker*, in conjunction with the *buried layer*, provides a low resistivity path for the current flowing from the SPAD active area to the anode contact. Similarly, the *isolation*, in conjunction with the *n-type substrate*, forms a sort of well that entirely surrounds the device anode; therefore by reverse biasing the isolation-anode junction it is possible to electrically isolate the SPAD from adjacent devices.

The role of the aforementioned regions can be fully understood by analysing a few kinds of arrays fabricated by using a double epitaxial SPAD. Arrays for photon counting applications, i.e. for applications in which a picosecond temporal resolution is not needed, can be fabricated simply by placing multiple devices on the same silicon chip^{[17], [18]}. Although useful, attaining an electrical isolation between anodes is not mandatory in this particular case. In fact, it is possible to operate the devices in a common anode configuration, in which every cathode is connected to a different Active Quenching Circuit (AQC). The isolation region is nevertheless of the utmost importance in order to reduce the direct component of the optical crosstalk between adjacent pixels^{[23], [24]}.

On the contrary, attaining a full isolation between SPADs is essential for timing arrays. In fact, with large active area devices^[25], a temporal resolution of a few tens of picosecond can be attained only if the avalanche current is sense by means of a suitable circuit^[26] as the one depicted in Figure 2.a. The avalanche current is injected into a low impedance network that converts it into a voltage signal that is in turn sensed by a low voltage comparator^[27]. However such a scheme requires that both the anode and the cathode are electrically isolated from adjacent devices.

Actually, while the circuit of Figure 2.a provides excellent results for a single SPAD, it cannot be properly used for arrays. In fact the disturbances induced by the commutations of adjacent devices prevents the operation of the comparator at low threshold. Such an issue has been overcome by integrating, on the same chip of the detector, a front-end for reading the avalanche current^{[28], [29]}. The capacitance reduction that results from monolithic integration makes possible to attain the same timing performance while reading the voltage signal at a much higher threshold. The adopted scheme is reported in Figure 2.b; its implementation requires the integration, on the same chip of the detector, of a few n-channel MOSFETs. The isolation region provides therefore not only the electrical isolation from the anodes of adjacent devices, but also from the body region of n-MOS transistors.

3. RE-SPAD: STRUCTURE

The RE-SPAD has been designed starting from the double epitaxial structure of Figure 1. The structure has been modified in order to improve the PDE in the red/near-infrared range. To this aim, the thickness of the p^- layer has been considerably increased (from about 3 to

about 10 μm) in order to improve the photon absorption probability, especially for the longer wavelengths^[30]. Actually, other modifications to the device structure are needed in order to optimize device performance. In particular a Boron peak inside the quasi-intrinsic layer provides the degrees of freedom needed in order to optimize the shape of the electric field in the multiplication region while limiting the breakdown voltage^[1]. However, for the sake of this paper, we can safely neglect such modifications and focus on the simplified RE-SPAD cross-section reported in Figure 3. The increased thickness of the quasi-intrinsic layer p^- has two main consequences: the sinker does not reach anymore the buried layer and similarly the isolation is not connected anymore with the n^+ substrate. In the following sections we will thoroughly analyse the impact that these facts have on the operation of the RE-SPAD both as a single detector and as an element of an array.

4. RE-SPAD: ISOLATION ISSUES AND SOLUTIONS

4.1 Limitations arising from the lack of electrical isolation

The fact that isolation does not reach anymore the n^+ substrate prevents the fabrication, on the same silicon chip, of multiple p-type wells electrically isolated one from the others. The most evident and obvious consequence is the impossibility of fabricating SPADs with anodes isolated one from the others and the impossibility to integrate some basic front-end electronics on the same silicon chip. Therefore, without modifications aimed at recovering full isolation between pixels, the RE-technology does not allow the fabrication of arrays for photon-timing applications.

On the contrary, the design of arrays for photon-counting applications is still possible with unmodified RE-technology, provided that the detectors are operated with a common anode voltage and that an AQC is connected to each cathode. Nevertheless this solution presents some remarkable limitations that deserve a more in-depth discussion.

It has already been demonstrated, both theoretically^[20] and experimentally^[1], that RE-SPADs attain the best performance when operated at an overvoltage significantly large than the 5V that are typically used for thin SPADs. For example the curves reported in [1] have been attained at an overvoltage $V_{ov}=20\text{V}$ that guarantees a good PDE while maintaining the DCR very low. However, for some applications in which the PDE is especially important or in which DCR is dominated by the background, a further increase of the overvoltage might be really advantageous.

The higher applicable overvoltage is limited in practice by the edge breakdown of the junction. For example, for the devices reported in [1] the breakdown of the active junction was of about 50V, while the edge breakdown was of about 75V, thus limiting the maximum overvoltage to slight less than 25V. In order to overcome this limitation it is possible to surround the cathode with one or more guard rings (see Figure 4). The latter make it possible to suitably shape the electric field at the edge thus increasing correspondingly the edge breakdown. However, the use of guard rings makes challenging connecting the AQC to the cathode and the solution in which the AQC is connected to the anode would be really preferable. So, summarizing, the fabrication of arrays for counting applications with RE-

technology is possible but with either some limitations or with a significantly increased complexity.

The lack of isolation has some disadvantages also for the operation of the single-pixel RE-SPAD. One of the most relevant is the fact that the junction between the anode and the substrate is not limited to a region slightly larger than the active area, but extends across the entire silicon chip with a huge capacitance between those terminals. The consequences are remarkable for single RE-SPAD used for photon timing. In fact, the large value of capacitance prevents an effective pick-up of the avalanche current from the anode; this can be faced by reading the avalanche current at the cathode and by connecting a suitable AQC to the anode. However, such a large capacitance has an impact also on the operation of the AQC and might result in a degradation of performance like maximum counting rate, power dissipation and afterpulsing probability. Actually, the effect of the large capacitance can be partially mitigated by avoiding the connection of the substrate directly to a fixed voltage. It can rather be connected to a suitable voltage through a large value resistor (e.g. 100k Ω) that leaves the substrate almost floating on fast transients.

4.2 Technological solutions for recovering full electrical isolation

From the previous subsection it is apparent that the lack of electrical isolation is the main obstacle to the development of an array of RE-SPADs. Therefore, in this subsection, we will analyse the solutions that can be adopted in order to overcome this limitation.

The most straightforward approach is to work on the drive-in phase of the isolation region; by increasing either the temperature or the duration of the diffusion step is indeed possible to drive the isolation region deeper into the epitaxial layer. Such an approach is feasible thanks to the large value of the diffusion coefficient of Phosphorous ions used as a dopant. However, the overall increase of the thermal budget has some remarkable drawbacks. First of all, the Boron dopant into the buried layer would experience a significant diffusion leading to an increased thickness of the neutral zone beneath the active region. Since the lifetime of the slow component of the temporal response of the device is quadratically related to that thickness^[30], this solution is incompatible with the requirements of many time-resolved applications. Similarly, also the Boron peak introduced into the quasi-intrinsic layer would experience a broadening, with a strong impact on the electric field profile in the multiplication region. Finally, during the high-thermal budget annealing, the Phosphorous into the isolation would diffuse also laterally therefore increasing the minimum width of the isolation region, with a negative impact on fill-factor of the array.

In order to reduce the overall thermal budget while attaining electrical isolation, it is possible to make the Phosphorous diffuse from both the top and the bottom of the epitaxial layer. This approach, widely used in power devices fabrication, requires that Phosphorus ions be implanted into the regions where the isolation has to be performed both before and after the growth of the epitaxial layer. The main drawback of this solution is in the increased complexity of the fabrication process, especially if the epitaxial growth is not performed on same site of the other processing steps. Moreover, although probably viable for the current structure, this approach is somehow limited in terms of further device development prospective since it is unsuitable for thicker structures.

The limitations set by aforementioned solutions can be completely overcome by resorting to Dielectric Isolation (DI). In this case, the current's flow between adjacent devices is prevented by surrounding each detector with a deep trench filled with isolating material (see Figure 5). Such a structure can be manufactured by using technological steps that are almost standard in today's silicon fabs. In particular, after defining the regions for DI by means of standard lithography, deep trenches are etched into the substrate by using plasma-assisted processes; their walls are then covered with silicon dioxide, with a thickness suitable for attaining the desired isolation; trenches are then refilled with polysilicon and capped with an additional protective silicon dioxide layer; finally the structure is planarized to ease the execution of the following processing steps.

Electrical isolation with deep trenches presents remarkable advantages when compared with junction isolation. First of all, dopant diffusion induced by trench manufacturing is fairly limited; in fact, both trenches' etch and material deposition are carried out at low temperature while a limited thermal budget is needed only to densify silicon dioxide at the end of the process. Overall thermal budget is indeed reduced if diffused isolation regions are fully replaced by deep trenches. Another remarkable advantage of DI is its compactness. Actually, junction isolation requires a considerable amount of space essentially because dopant diffusion happens both vertically and horizontally. So when a dopant is vertically driven-in for a certain length L , it simultaneously diffuses laterally for a distance equal to about $0.7 \cdot L$. This process limits the minimum geometrical dimension attainable for the isolation region; moreover, to this dimension, one has to add the space needed for the extension of the depleted regions. On the contrary, for manufacturing trenches, nowadays processes are available that etches the silicon almost in one direction. For example Deep Reactive Ion Etching (DRIE) based on Bosch Process makes possible to attain trenches with an aspect ratio ranging from 10:1 to more than 20:1 (see for example [32]). Therefore trenches can be manufactured with a total occupancy of only a few microns.

The main issue with DI isolation is crystal defectiveness. Actually the stress that develops at the interface between silicon and silicon dioxide at the trenches' walls can lead to the formation of crystal defects such as slips and dislocations. If these defects reach the SPAD active area they can act as generation and recombination centres with a dramatic impact on device noise. However, in the last years big advances in processing technology have strongly reduced the concentration of such defects. Moreover it has been demonstrated that the defects originate from the bottom of the trench and propagate diagonally along crystallographic axes; therefore they should not affect DCR provided that the active area of the device is placed at a suitable distance from the trench (e.g. $10 \mu\text{m}$). However since SPADs are especially sensitive to such kinds of defects, this point deserves a detailed experimental verification.

5. RE-SPAD: SERIES RESISTANCE ISSUES AND SOLUTIONS

From the RE-SPAD cross-section reported in Figure 3 it is apparent that the increased thickness of the p^- epi-layer prevents also the sinker from reaching the buried layer. This fact results in a remarkable increase of the SPAD series resistance. This is especially undesirable from the point of view of the temporal resolution; in fact, it has been

demonstrated^[31] that an increase of the series resistance reduces the avalanche growth rate leading to a worsening of the photon timing jitter. In single-pixel detectors, the problem can be easily addressed by widening the sinker region. On the contrary, this solution is not fully viable for the arrays since a larger sinker increases the ratio between pixels' pitch and active area diameter, leading to a significant reduction in the fill-factor.

A very effective and general solution to this problem, perfectly compatible with the fabrication of arrays, comes once again from the use of deep trenches. Actually, a deep sinker can be attained if trenches' walls are implanted right before oxide deposition. The resulting structure, depicted in Figure 6, presents once again significant advantages in terms of compactness. Moreover its fabrication does not require a significant additional thermal budget since the implanted Boron can be diffused during other high-temperature steps needed the fabrication of the device active area.

6. RE-SPAD: ANODE-SUBSTRATE BREAKDOWN ISSUES AND SOLUTIONS

In the device structures represented in Figure 1 and in Figure 6, the breakdown voltage of the junction between the anode and the substrate is usually determined by the doping level of the buried layer, being the doping concentration of the substrate significantly higher. Typical doping concentrations used for the buried layer of these devices result in anode-substrate breakdown voltage $V_{BD, A-SUB}$ ranging from 15 to 25V. In this section we will show that such a low breakdown voltage can severely limits the performance attainable with RE-SPAD arrays and we will analyze the solutions that can be adopted in order to overcome such limitations.

6.1 Limitations arising from anode-substrate breakdown voltage

Figure 7.a represents a typical configuration for operating a SPAD, in which the anode is connected to the AQC, the cathode to the voltage supply $V_{POL} = V_{BD} + V_{OV}$ and the substrate to the voltage supply V_{SUB} . The anode voltage is essentially switched between two different values by the AQC; in particular, the anode is kept to ground when the SPAD is waiting for a photon arrival, while it is raised to V_{QUENCH} after an avalanche has been triggered.

For the avalanche to be effectively turned off by the AQC, during the quench phase the voltage across the SPAD must be lower than the breakdown voltage. For this reason the applied overvoltage V_{OV} must comply with the following relation:

$$V_{OV} < V_{QUENCH} \quad (1)$$

On the other hand, the anode voltage must always remain below the substrate voltage to prevent the forward biasing of the corresponding junction. For this reason also the following relation must be satisfied:

$$V_{QUENCH} < V_{SUB} \quad (2)$$

Finally, since the voltage applied to the anode-substrate junction when the SPAD is waiting for a photon arrival is exactly V_{SUB} , to prevent the breakdown of the junction itself, one has to comply also with following requirement:

$$V_{SUB} < V_{BD,A-SUB} \quad (3)$$

Combining the relations (1) – (3), it turns out that:

$$V_{OV} < V_{QUENCH} < V_{SUB} < V_{BD,A-SUB} \quad (4)$$

Relation (4) shows that the maximum overvoltage applicable to the detector is upper limited by the breakdown voltage of the anode-substrate junction. Since $V_{BD,A-SUB}$ is typically lower than 20V – 25V and since each of the inequalities in (4) must be satisfied with a certain tolerance (for example to avoid possible issues related to overshoots during fast transients), it is evident that there is a severe limitation to the maximum overvoltage applicable and therefore to the attainable performance especially in terms of PDE.

Such a limitation can be partially overcome in single-pixel RE-SPAD. In this case, the detector can be operated by using a configuration, such the one depicted in Figure 7.b, where the substrate is connected to V_{SUB} through a high value resistor R_{SUB} . By adopting this configuration, the substrate is still biased at the voltage V_{SUB} while waiting for a photon arrival; conversely, during the quench and the hold-off phase, the substrate reaches a higher voltage due to the capacitive coupling with the anode. This way, V_{QUENCH} is not required anymore to be lower than V_{SUB} and the applied overvoltage can therefore be larger than $V_{BD,A-SUB}$. Its maximum value actually depends on the raising of the substrate during the hold-off and therefore on the value of the parasitic capacitances.

Although the aforementioned solution works (with some remarkable limitations) in the case of single-pixel detectors, it cannot be applied to RE-SPAD arrays. In fact, in the latter, it is mandatory to keep the substrate at a very fixed voltage. If not, any fast transient due to the quenching of a SPAD would couple through the substrate both to the anodes and to the front-ends of the nearby detectors. The formers might result in spurious counts while the latters in a distortion of the recorded timing curves.

6.2 Technological solutions to increase the anode-substrate breakdown voltage

The previous discussion showed that increasing the breakdown voltage of the anode-substrate junction is mandatory in order to obtain the best performance with a RE-SPAD array.

The more obvious solution to address this problem is the reduction of the doping concentration in the buried layer. However, this approach is not viable since it would result in an increased value of the series resistance. Moreover, the reduction in doping concentration cannot even be compensated by increasing the thickness of the buried layer since this would result in a severe degradation of the lifetime of diffusion tail.

Figure 8 represents the solution we adopted. A lightly doped n-type layer has been interposed between the substrate and the buried layer. The thicker is the n⁻ layer, the higher is the breakdown voltage since the space charge region can extend across it. In particular, a thickness of a few microns is sufficient to guarantee a breakdown voltage of many tens of Volts. The interposed n⁻ layer can be grown by using an epitaxial process; this solution is therefore perfectly compatible with the Red-Enhanced fabrication process.

7. CONCLUSIONS

In this manuscript we showed that, although essentially compatible with the fabrication of arrays, RE-SPAD structure still requires a few critical modifications to make a proper operation of the array itself possible. We showed also that simple modifications to current process parameters are not sufficient to attain the full electrical isolation between devices and to reduce the series resistance that are crucial for the implementation of time resolved arrays. Dielectric insulation obtained by means of deep trenches appears to be the most promising technology to address these issues; however a more detailed investigation is still needed. To this aim, a new generation of RE-SPAD devices implementing DI is currently under development in our laboratory.

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Figure 1.
Cross section of a typical double epitaxial thin SPAD.

Figure 2. Avalanche current pick-up circuit for single pixel detectors (a) and for SPAD arrays (b).

Figure 3.

Cross section of a RE-SPAD. Note that the isolation and the sinker regions do not reach respectively the substrate and the buried layer.

Figure 4.

Cross section of a RE-SPAD with additional Guard Rings (GR) to prevent edge breakdown at high overvoltages.

Figure 5.
Cross section of RE-SPAD with isolation implemented by means of deep trenches.

Figure 6.

Cross section of RE-SPAD with isolation implemented by means of deep trenches. Note Boron implantation on trenches wall in order to reduce series resistance.

Figure 7.

Configuration for operating a SPAD with a fixed voltage at the substrate (a) or with a semi-floating substrate (b).

Figure 8.

Cross section of RE-SPAD with isolation implemented by means of deep trenches and a lightly doped n-type layer interposed between the buried layer and the substrate to increase breakdown voltage at this junction.