A Building Block for Nuclear Medicine Imaging Systems Data Acquisition

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I. Introduction

Developing new detector designs for PET and SPECT imaging systems often leads to problems in adapting existing data acquisition electronics to the requirements for the new devices. As we developed our dMiCE and cMiCE detector concepts [1,2], we found that our existing electronics was inadequate to the task and launched a design effort we have termed our Phase II electronics [3]. Here we report on the implementation and evolution of the Phase II system as a basic building block for a wide variety of data acquisition tasks.

II. Phase II System Design and Testing

A. System Design

The basic approach was to minimize analog processing and move as much pulse processing as feasible into an FPGA. To allow easy adaptation to different detectors, we designed the system around a digital processing board (the Phase II board) that is then connected to the detectors with a separate analog adapter board. The analog board provides power and any local control needed to the detector and sends differential signals to the Phase II board.

Given the costs of board design and layout, we also decided to put our resources into designing a single board that can take on many different roles in a data acquisition system depending on which components are installed and the version of FPGA code utilized. This approach makes for a complex board but made best use of the resources available to us for this project. During the design phase, one engineer did both the schematic design and board layout in parallel. In that way, we were able to optimize the design to maintain needed bandwidth of signal traces, minimize any skewing issues for parallel data paths, and keep the number of layers down to twelve. The board also provides significant heat dissipation by using large ground planes to "pipe" heat out to the board mounting points. Another design decision was to use a family of Altera FPGAs that share the same footprint so that different cost/performance targets can be meant by simply choosing which FPGA to mount on the board.

Figure 1 is a block diagram of the Phase II board. It is designed to accept either 64 channels of differential analog signals (which are then digitized with 65 MHz ADCs) or 64 channels of serial signals from a detector adaptor board. The board also has one high speed (> 300 MHz) ADC channel for those detectors that provide a fast timing pickoff signal. The Phase II board is designed around a family of high performance FPGAs from Altera, and we have developed a wide range of pulse integration, timing, and processing algorithms for the device [4-7].

Figure 2 is a diagram of the basic FPGA logic structure that supports our cMiCE detectors – and represents the most demanding use of the Phase II board resources we have implemented to date. The FPGA code provides baseline restoration and pulse pile-up correction for all 65 ADC channels. The 64 “slow” channels are then used as inputs to the event estimator that locates the event in three dimensions using the estimation algorithms developed in our laboratory. In parallel, the high-speed pickoff-timing signal is processed and the time stamp determined. The data are then combined and sent to the host using the NIOS II soft processor and the host bus transceiver integrated circuit (e.g., the USB interface).

Other features of the board include several SPI bus and temperature monitoring connectors, as well as expansion connectors for daughter boards for future requirements. Switches allow setting ID numbers for the boards. Due to the requirements for the statistical estimator for the cMiCE detector [6], the board also includes 380 Mbytes of static random access memory. As described in [3, 8] the cards can be setup to serve several functions in a scanner system including serving as a master coincidence controller, an acquisition node taking data directly from detectors, or as a acquisition node that is taking data from other Phase II cards that are in turn connected to detectors (a modified star topology). This connectivity flexibility allows supporting different acquisition topologies. Some of the possibilities are diagramed in Figure 3.

The initial design used FireWire for the host to board data transfer and commands. We are currently implementing USB 2.0/3.0 support and will incorporate that circuitry on the main board in the next revision (expected by August 2012). As part of that revision, we are investigating the feasibility of dedicated daughter board architecture to allow converting the board between the different host bus options (USB, FireWire, Ethernet, PCIe, etc). The restrictions of such an adapter board are dictated by the current transceiver to FPGA data path (based on an 8 bit parallel bus with several control lines) and preserving the bandwidth of the different bus standards. Thus far, all of the transceivers we have considered can easily be adapted to the current restrictions.

For the short term, we are focusing on the USB implementation that is based around a Cypress CYUSB3014 transceiver. In operation, the board will default to USB 2.0 on power up. However, the host computer can send a command to the board to instruct it to use USB 3.

The FPGA also is configured with the NIOS II software based embedded processor for general control, processing of commands from the host, and communications between the cards. A megabyte of FLASH ROM is included for NIOS software and other data needed to be loaded into the static RAM supporting the FPGA. The FPGA is loaded at power up from an Altera load device and additional FLASH ROM. JTAG connectors are provided for programming and testing. More details are included in [3,8]. Figure 4 depicts the top side and an “X-ray” view of the traces of the Phase II board.

B. Initial Testing

Figure 5 shows the configuration for testing with a cMiCE detector. The overall performance met expectations and the time to debug the card was less than we had anticipated. Once all of the components were confirmed to be operating properly, simple Verilog code was written and combined with C code in the NIOS II soft embedded processor to begin testing the card with real data. For these first tests, a prototype detector adapter board was fabricated to provide amplification and conversion of signals to differential pairs from a cMiCE detector utilizing a 64 channel Hamamatsu H8500 PMT. This setup allowed testing of the revision 1.0 Phase II board by recording event by event data digitized from all 64 analog inputs.

Figure 6 depicts one of the first tests done with signals from a cMiCE PMT based detector. A single event is shown with the digitized outputs from each of the 64 anodes (the grid of small plots) and a zoomed plot of the anode with the largest signal.

Figure 7 depicts the result of summing all of the 64 channel “slow” ADCs and comparing it to the high speed ADC that is connected to the timing pickoff signal from the cMiCE detector. The data both show the fidelity of the two different input channels in terms of pulse shape, but also confirms that possible time skewing issues for the entire chain are all properly compensated for in the basic board design.

Figure 8 depicts a simple coincidence test configuration with two cMiCE detectors. One has the full set of analog boards, the other is only connected to the detector fast timing pickoff. Similarly, one of the Phase II boards is processing all 64 channels and the fast timing signal from one detector. The second Phase II board is only using its fast ADC to process the timing signal from the second cMiCE detector. One of the results is shown in Figure 9 where we depict the 64 slow channels processed by the first Phase II board and overlay the fast timing ADC results from both boards. Again, we see that the time skews for the entire processing chain are minimal.

III. Discussion and Conclusion

This project was undertaken initially to support the cMiCE and dMiCE detector designs in our laboratory. At the time the project started, we were unable to find commercial products that would support the estimation tasks at the detector level required by our cMiCE approach. Similarly, the OpenPet initiative (<http://openpet.lbl.gov/>) was in the early stages of development and did not provide the capabilities we wished for the data reduction for the cMiCE detector. The board is meeting its design specifications and is now being used to develop a pre-clinical scanner and also a human breast scanner based on the cMiCE detector concept. Additional projects include licensing the card to a company for use in their gamma ray imaging systems as well as implementing an easily configurable I/O system to support a variety of bus types – with the first major revision being the support of USB 2.0/3.0 will be completed later this year. Along with the card, we have a reconfigurable software tool for list mode acquisition that will support the bus types the Phase II card is configured for (currently FireWire or USB). Standard command and control code has also been written for the embedded processor on the Phase II board to allow easy adaptation to many different acquisition topologies – a few examples of which are shown in Figure 3.

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Fig. 1.
Block diagram of the Phase II digital board.

Fig. 2.
Diagram of the FPGA logic used for the cMiCE detector module.

Fig. 3.
Diagram of the FPGA logic used for the cMiCE detector module.

Fig. 4. Phase II card top view and the X-ray image (generated by the Eagle layout software) showing the 12 layers of traces.

Fig. 5.
Phase II board connected to a cMiCE detector with new adapter cMiCE adapter boards.

Fig. 6.
Example of a single event in the cMiCE detector (grid of 64 channels on the left) and the timing pulse (plot on the right) as recorded by the Phase II digital card.

Fig. 7. Comparison of the summed slow ADC channels and its high-speed timing ADC for a single event from the cMiCE detector recorded by the Phase II digital card.

Fig. 8. Test bench with two Phase II digital boards and two cMiCE detectors (left detector with full 64 channel readout, right detector setup for timing only).

Fig. 9.

Data from a single event for the test configuration of Figure 8. The 64 channels of the left PMT are shown on the left and both timing pickoff channels are shown on the right. In this case, the FPGA logic utilized the SPI busses to notify the paired boards that a coincidence event occur red.