Published in final edited form as:

J Phys Condens Matter. 2013 January 9; 25(1): 014011. doi:10.1088/0953-8984/25/1/014011.

Structure and Growth of Quasi One-Dimensional YSi₂ Nanophases on Si(100)

V. Iancu,

Department of Physics and Astronomy, The University of Tennessee, Knoxville, TN 37996, USA

P.R.C. Kent,

Center for Nanophase Materials Sciences and Computer Science and Mathematics Division, Oak Ridge National Laboratory, Oak Ridge, TN 37831

S. Hus,

Department of Physics and Astronomy, The University of Tennessee, Knoxville, TN 37996, USA

H. Hu,

Department of Physics and Astronomy, The University of Tennessee, Knoxville, TN 37996, USA

C.G. Zeng, and

Hefei National Laboratory for Physical Sciences at Microscale and Department of Physics, University of Science and Technology of China, Hefei, Anhui 230026, China

H.H. Weitering

Department of Physics and Astronomy, The University of Tennessee, Knoxville, TN 37996, USA
Materials Science Technology Division, Oak Ridge National Laboratory, Oak Ridge, TN 37831
hanno@utk.edu

Abstract

Quasi one-dimensional YSi₂ nanostructures are formed via self-assembly on the Si(100) surface. These epitaxial nanowires are metastable and their formation strongly depends on the growth parameters. Here, we explore the various stages of yttrium silicide formation over a range of metal coverages and growth temperatures, and establish a rudimentary phase diagram for these novel and often coexisting nanophases. In addition to previously identified stoichiometric wires, we identify several new nanowire systems. These nanowires exhibit a variety of surface reconstructions, which sometimes coexist on a single wire. From a comparison of scanning tunneling microscopy images, tunneling spectra, and first-principles density functional theory calculations, we determine that these surface reconstructions arise from local orderings of yttrium vacancies. Nanowires often agglomerate into nanowire bundles, the thinnest of which are formed by single wire pairs. The calculations show that such bundles are energetically favored compared to well-separated single wires. Thicker bundles are formed at slightly higher temperature. They extend over several microns, forming a robust network of conducting wires that could possibly be employed in nanodevice applications.

1. Introduction

Rare-earth silicide nanowires have sparked great interest in recent years. These nanowires self-assemble on a heated silicon substrate in the presence of a small metal flux and are typically several nanometers wide and up to 1000 nanometers long [1, 2, 3, 4, 5, 6]. Their unidirectional growth typically requires a highly anisotropic lattice match between the substrate and silicide compound so that the crystalline wire grows almost exclusively along the lattice-matched direction [4, 7, 8]. These epitaxial structures are superior to nanowires fabricated by *e.g.* lithography because they are smaller and because they are highly

crystalline, having atomically abrupt interfaces. These wires are also very stable and robust at room temperature, and thus they are ideal candidates for low-resistance electrodes or interconnects in nanoelectronic circuits [9, 10, 11]. From the physics perspective, they are particularly interesting for studying the complexity of electronic interactions in one-dimension (1D). Possible ground states include charge- [6] or spin density wave condensates [12], a Luttinger liquid state [13], or perhaps even superconductivity [14].

Of all the silicide nanowires studied so far, YSi_2 appears to be the best candidate for producing nanowires with extreme aspect ratios [6, 15, 16]. This particular silicide compound exhibits the hexagonal AlB_2 -type structure, which perfectly matches the lattice

constant of the Si(100) substrate along its $\left[1\bar{1}0\right]$ direction [6]. Consequently, their aspect ratios can be enormous, up to one thousand for even the thinnest ones, and exceed those of other rare-earth silicide nanowires. However, the YSi_2 nanowires are thermodynamically metastable and their formation sensitively depends on the growth conditions.

Nanowire formation is preceded by the formation of a 2D yttrium-induced Si(100)(2×7)-Y surface reconstruction or 'wetting layer'. This wetting layer reconstruction can be viewed as a quasi 1D template for the growth of YSi_2 nanowires. Similar reconstructions have been observed for Gd and Dy on Si(100) [1, 3, 17] whereas Er induces (2×3) and (2×4) reconstructions [18]. The structure and precise composition of the wetting layers remains unclear although a study by Liu *et al.* indicated a wetting layer coverage of about 1/3 monolayer (ML) for the Gd case [17]. The presence of this wetting layer complicates our understanding of the mechanism of wire formation. For instance, the wetting layer obscures the exact registry and orientation of the nanowires relative to the Si dimer rows of the clean Si(100)(2×1) substrate. In addition, the structure, electronic properties, and stability range of the individual YSi_2 nanowires and nanowire bundles remain to be determined. The thinnest nanowires, which are only 1.1 nm wide, are a notable exception. They have been well studied and were shown to represent a very close realization of a 1D electronic system, which undergoes a charge ordering transition at low temperature [6].

In this paper, we will investigate the various stages of silicide formation, starting with the 'wetting layer' and the formation of ultrathin nanowires, nanowire bundles, and flat-top 3D islands. We first present a bird's eye view of the growth features and establish a rudimentary 'phase diagram' for this complex submonolayer silicide system. Next, we will investigate the structures of the nanowires and nanowire bundles. Specifically, we will focus on the intermediate-width nanowires (1.9 nm wide) which, unlike the thinner wires, exhibit surface superstructures that are unrelated to charge ordering. Similar superstructures are observed on broader wires. The 1.9 nm-wide wires can thus be regarded as the key building blocks of the bigger nanowire bundles and solving their structures will be essential for understanding the properties of the larger nanowire bundles. The wire structures are determined by comparing scanning tunneling microscopy (STM) images and scanning tunneling spectroscopy (STS) data to simulated images and spectra obtained from first-principles Density Functional Theory (DFT) calculations. In these calculations, we considered a large number of structure models with varying stoichiometry. Several new structures are found that closely reproduce the topographic STM images and measured density of states. A common feature is a reduced yttrium concentration, the resultant pattern of vacancies strongly influencing the simulated STM data. Finally, we will show how wire-wire interactions lead to the formation of wire bundles and ultimately 3D islands.

2. Experimental and Computational Methods

The growth of YSi_2 nanowires was performed in ultrahigh vacuum. Nominally undoped $\text{Si}(100)$ wafers were outgassed at 500°C for several hours and the native SiO_x layer was subsequently removed by flash-heating to 1200°C , producing atomically clean $\text{Si}(100)(2\times 1)$ surfaces. YSi_2 nanowires were grown via e-beam evaporation of 99.99% pure yttrium metal onto a heated $\text{Si}(100)$ substrate. The substrate temperature was varied between 600°C and 650°C during growth and between 600°C and 700°C during post annealing. Temperatures were measured with an infrared pyrometer with a precision of $\pm 25^\circ\text{C}$. The yttrium deposition rate was 0.2 ML/min , which was determined from the deposition time needed to complete the $\text{Si}(100)(2\times 7)$ -Y wetting layer reconstruction (0.35 ML [17]). Scanning tunneling spectroscopy (STS) was performed by recording the tunneling current (I) while ramping the tunneling bias (V) at specific locations on the nanowires. The differential conductance (dI/dV) was obtained via numerical differentiation of the I/V curves [19]. STM and STS data have all been recorded at room temperature (RT), unless stated otherwise. Tunneling voltages in this paper always refer to the sample bias. STM images were analyzed using WSxM software [20].

To assess the possible YSi_2 nanowire structures and electronic properties, we employed DFT calculations, implemented in the plane-wave projector augment wave method [21, 22, 23, 24] and the local density approximation (LDA) functional [25]. We used supercells containing a slab with nine layers of Si atoms. Hydrogen atoms passivated the rear surface. The bottom two layers of atoms were held fixed at the theoretical bulk lattice positions. All other atoms were allowed to fully relax. To study the reconstructed wires we used larger supercells than our previous studies [6, 15], doubled along the wire axis to allow for up to 4 repeat units. The $5a_0$ -width wire supercells contained 596 atoms. Geometries were obtained using only the Gamma-point for Brillouin zone sampling. STM simulations used a finer $6\times 2\times 1$ k-point grid and the Tersoff-Hamann scheme [26]. We utilized a 250 eV plane wave cutoff.

3. Results and Discussion

3.1. Self-assembly of YSi_2 Nanostructures: from quasi 1D wires to 3D islands

Figure 1 presents a STM image of the YSi_2 wetting layer. At low yttrium coverage ($\theta = 0.25\text{ ML}$), figure 1(a), both the clean Si surface and the wetting layer can be resolved. The wetting layer rows clearly grow perpendicular to the surrounding silicon dimer rows. The two types of terraces on a flat clean $\text{Si}(001)$ surface, the Type-A terrace (T_A) where the Si dimer rows are running parallel to the down-step edge, and the Type-B terraces (T_B) where the dimer rows are perpendicular to the down-step edge, are indicated in the figure together with the respective steps edges (S_A) and (S_B). Due to the intrinsic 4-fold symmetry of the $\text{Si}(100)$ surface, one always finds two orthogonal domains. However at this low coverage, the wetting layer is predominantly formed on the Type-B terraces, suggesting that the terrace edges play an important role in wetting layer nucleation. Yttrium atoms on Type-A terraces can travel over very long distances parallel to the terrace edges. However, on the Type-B terraces they travel much shorter distances before reaching a terrace edge, where they nucleate or merge with existing (2×7) patches. Interestingly, unlike the yttrium rows of the (2×7) reconstruction, the YSi_2 (discussed below) do not show any preference for the terrace type, nor is there a clear preference for nucleation at the terrace edges.

A small increase of coverage ($\theta = 0.4\text{ ML}$) completes the wetting layer on both types of terraces. Figure 1(b) and (c) show the wetting layer, which apparently consists of dimer rows that are separated by areas of lower apparent height, depending on tunneling bias and polarity. At this stage, YSi_2 nanowires have not yet been formed on the surface. The only

features that are somewhat out of the ordinary are the extra rows highlighted by arrows in figure 1(b) and (c). They appear to grow on top of the 2×7 rows and protrude about 0.1 nm above the (2×7) reconstruction at -1 V bias. Their density is coverage dependent and they likely act as the 'building foundation' of a future YSi_2 wire. These extra rows have also been observed for Dy on Si(100) [27], where they have been referred to as "dark wires". For Y, these "dark wires" are found to be 1.1 nm and 1.5 nm wide and their formation seems to be associated with occasional 'phase shifts' in the interwire spacing of the (2×7) phase. At higher coverage these extra rows become more numerous. Similar to the Dy (2×7) wetting layer [11], the yttrium-induced (2×7) wetting layer is not metallic, a fact that is confirmed by STS and 4-probe transport measurements [28].

The thinnest wires nucleate after an almost complete (2×7) wetting layer has formed. They grow parallel to the atom rows of the wetting layer, suggesting that the adatom diffusion barriers are lowest along the atom rows. Deposition flux, substrate temperature and the yttrium content of the wetting layer are all expected to influence the growth and morphology of the nanowires. We find that a small change in one parameter alone can strongly influence the growth process and tilt the balance between formation of isolated wires versus bundles of wires. This is well captured by the DFT calculations as described in the next sections. For the present study we kept the deposition flux constant at 0.2 ML/min and varied the yttrium coverage and substrate temperature.

Extremely thin nanowires are formed at very low coverages ($0.4 < \theta < 0.5$), low deposition rates and *no postgrowth annealing* (figure 2(a)). The most favored structures in this regime are isolated YSi_2 nanowires with widths ranging from 1 nm to 4 nm. Their in-plane widths are quantized in integer multiples of silicon lattice constant ($a_0 = a_{\text{Si}} = 0.384$ nm). They can grow as long as 1000 nm, depending of the local availability of yttrium and the step density.

At slightly higher coverage, ($\Delta\theta = 0.1$ ML), the wires tend to assemble in bundles with an interwire distance of $1a_0$. Figure 2(b) shows wire-bundles obtained by yttrium deposition at 630°C and no post-growth annealing. The bundles are uniformly distributed over the entire surface in two orthogonal domains. Inside the bundles, the wires are found to have widths similar to those of the isolated nanowires in the low coverage regime. Occasionally, one finds wider wires inside the bundles with widths ranging from $8a_0$ to $11a_0$. The latter ones are formed on vacancy-rich wetting layers. A detailed STM description of the bundles and their formation energies is presented in the next section.

Besides the yttrium coverage, the growth temperature also influences the wire growth. Figure 2(c) displays a STM image of a surface with the same yttrium content as in figure 2(b) but grown at slightly higher temperature ($\Delta T = 30^\circ\text{C}$). Here, the bundles can span across the surface for micrometers. A surface step that is running perpendicular to the wire is easily eroded by the wire-bundle as it consumes the local silicon reservoir to increase its length. The growth of bundles can only be stopped when they run into other bundles, provided that there is enough yttrium material. In this regime, one often observes wire-bundle junctions and wire-bundle networks that can span across the entire sample area. Even though at the junctions, the nanowires are sitting on different terraces, they are still in physical contact so that electrical contact can also be established [28]. One can also observe nucleation of a second silicide layer on top of these nanowire bundles and eventually the silicide wire starts to grow layer-by-layer.

To study the effects of the substrate temperature during the early stages of nanowire formation in more detail, we have created a 75°C temperature gradient over the sample and placed it far away from the deposition source to ensure a homogenous deposition rate across the sample. The coverage ($\theta = 0.35$ ML) is selected so as to observe the surface close to the

completion of wetting layer growth. On the 600 °C side of the sample, the (2 × 7) wetting layer covers both the A and B type terraces while the nanowires are absent (figure 3(a)). However at the center of the sample where the substrate temperature reached 630 °C, thin nanowires appear (see figure 3(b)). Note that vacancies and phase shifts in the (2 × 7) row structures are uniformly distributed, showing no indication of yttrium or silicon depletion in the immediate vicinity of the nanowires. At 650 °C, on the hot side of the sample, wire-bundles start forming and the single isolated nanowires and (2 × 7) wetting layer have disappeared (figure 3(c)). Hence, at a fixed global yttrium coverage, increased temperature and surface diffusion reduces the (2 × 7) wetting layer coverage, as more yttrium (and silicon) is incorporated into the nanowires.

Further increase of the substrate temperature ($T = 650$ °C) leads to the formation of rectangular YSi_2 islands and total disappearance of the nanowires. Similar islands can be created by post-growth annealing of the nanowires. Depending on the annealing duration, two types of islands have been observed. Their aspect ratios, and possibly their crystal structures, are different.

Figure 4(a) shows a representative STM image of a sample (yttrium coverage 0.6 ± 0.1 ML) annealed at 670 °C for two minutes. Here, wire bundles coexist with quasi 2D islands, or 'Type I' islands. These Type I islands grow up to several silicides layers in height. Their

orientation is identical to those of the nanowires (long side parallel to the $\text{Si} \begin{bmatrix} 1 & \bar{1} & 0 \end{bmatrix}$ direction). Strong height modulations create a stripe like pattern that runs perpendicular to $\begin{bmatrix} 1 & \bar{1} & 0 \end{bmatrix}$ direction. They are interpreted as Moire fringes. The wavelength of the Moire fringes is expressed in terms of the $\text{Si}(100)$ and YSi_2 lattice parameters as follows:

$$d = \frac{a_{\text{Si}} a_{\text{YSi}_2}}{\|a_{\text{YSi}_2} - a_{\text{Si}}\|} \quad (1)$$

The calculated Moire-fringe separations are 164 nm along the "a" direction and 5.2 nm along the "c" directions for the hexagonal YSi_2 phase ($a = 3.849$ Å and $c = 4.147$ Å [29]), consistent with the stripe-like appearance in the STM images (figure 4 (a) and (b)). Experimentally, the distance between the Moire fringes is $5.5 \text{ nm} \pm 0.4 \text{ nm}$, which strongly suggests that the Type I islands also exhibit the hexagonal AlB_2 structure. The orthorhombic phase of YSi_2 has a high mismatch with the $\text{Si}(100)$ substrate along both directions (5.6 % along the "a" direction and 3.3 % along the "b" direction), which would give rise to a more mesh-like Moire pattern.

The surface of the Type I islands presented in figure 4(b) exhibits a $c(2 \times 2)$ reconstruction with many vacancies. Similar $c(2 \times 2)$ surface reconstructions have been observed on other silicide islands [5, 30] although Moire patterns had not been reported. In the case of ErSi_2 islands on $\text{Si}(100)$, the $c(2 \times 2)$ reconstruction was interpreted as a $c(2 \times 2)$ arrangement of Si adatoms [30].

Increasing the post-growth annealing duration results in the ultimate disappearance of all nanowires and Type I islands, in favor of more 3D silicide islands, named 'Type II' islands. These islands burrow through the silicon. Figure 4 (c) reveals three Type II islands, obtained after post-growth annealing to 700 °C. These islands locally inhibit Si surface diffusion and one often observes step bunches near the islands. These Type II islands have a lower aspect ratio but a volume estimate from STM is difficult because they are partially buried.

Type II islands also exhibit the $c(2\times 2)$ reconstruction, as shown in the inset of figure 4 (c). Close inspection of the surface reveals the presence of "ripples" separated by 2.1 nm that may appear as a stress release effect. Similar observations were made for other rare earth silicides islands [8, 31]. Transmission electron microscopy (TEM) studies of similar GdSi₂ islands indicated that their structure is orthorhombic or tetragonal [8]. Based on the close resemblance with Gd silicide islands, we suggest that the Type II YSi₂ islands are probably orthorhombic.

Figure 5 is a schematic diagram, illustrating the various stages of YSi₂ nanostructure formation for different coverages and growth temperatures. This is not a true phase diagram as the exact compositions and homogeneity ranges of the various nanostructures are unknown. Furthermore, most structures are non-equilibrium structures. Occasionally observed (2×4) wetting layer patches and the clean Si(100) (2×1) reconstruction have been omitted for clarity, so as to better highlight the main features.

3.2. Structure and Spectroscopy

3.2.1. Ultrathin nanowires—As mentioned in the previous section, extremely-thin nanowires are formed at low coverage ($0.4 < \theta < 0.5$) (figure 2(a)). These single nanowires have discrete widths that vary between $3a_0$ and $7a_0$ where a_0 is the in-plane Si lattice constant (0.384 nm). The majority of these wires are $3a_0$ and $4a_0$ in width. Together, they amount for about 80% of all wires. If the wire width is an odd multiple of the Si lattice constant, then the wire exhibits mirror plane symmetry. Here, the mirror plane is defined by the $\begin{bmatrix} 11 & \bar{2} & 0 \end{bmatrix}$ direction of the hexagonal silicide and the surface normal. Alternatively, if the wire width corresponds to an even multiple of the Si lattice constant, then the wire does not have mirror plane symmetry [6, 15].

To elucidate the structure and electronic properties of these wires, we implemented DFT calculations to find the total-energy minimized structure and electronic properties of the most plausible structure models. STM images and STS spectra were calculated for the various models and compared to experiment. To ensure good convergence of the calculated images we have focused on biases over 1 Volt. At small biases, very few states across the Brillouin zone contribute to the tunnelling. Extremely dense k-point meshes are therefore required for convergence, which is not practical in the large supercells employed here. At larger biases the features can be readily resolved since away from the Fermi level many more states typically contribute for a given k-point sampling. Because the structure of the wetting layer is unknown, the wires are placed directly on top of the Si(100) surface and aligned parallel to the dimer rows [32, 33]. For the $5a_0$ wires, the structures considered are built in accord with the structures of the $3a_0$ and $4a_0$ wires determined before [6, 15]. Here, the challenge is to reproduce the difference in the apparent height of the $5a_0$ wires and presence of a period doubling surface reconstruction. For the sake of clarity and completeness, we start with a discussion of the $3a_0$ and $4a_0$ wires.

For the thinnest wire, $3a_0$ or 1.1 nm wide, theory and experiment are in very good agreement; however, the observed charge order fluctuations at low temperatures could not be reproduced [6]. Here, the total-energy-minimized structure of the wire consists of two parallel rows of dimerized Si adatoms (figure 6 panels (a),(c) and (f)). The yttrium atoms are located directly underneath the dimers and in the channel between the two dimer rows [6]. The second thinnest wire, which is only 1.6 nm wide, is referred to as the $4a_0$ wire (figure 6 panels (b), (d), (e), and (g)). During our previous investigations [15] we determined the $4a_0$'s most probable structure, based on the best agreement between experimental and theoretical STS data. This structure is shown in figure 6(g). The simulated STM images for filled and empty states are presented in figure 6 (d) and (e). They reproduce the

experimental STM image in figure 6(b) quite well. Similar to the $3a_0$ wire, the surface of the $4a_0$ wire reveals two dimer rows with a 0.384 nm repeat distance along the wire direction. The $4a_0$ wire is about 0.21 eV higher in energy than the $3a_0$ wire, which is presumably due to the existence of additional dangling bonds in the $4a_0$ structure [15]. Dangling bonds also explain their higher reactivity, as they are often decorated with adatoms.

For the next wire widths, $5a_0$, $6a_0$ and $7a_0$, the situation becomes more complicated. Figure 7 shows several segments of $5a_0$, $6a_0$ and $7a_0$ wires. The $5a_0$ wire exhibits two prominent surface reconstructions. In the first case, figure 7(a), the surface consists of three parallel rows, similar to the calculated image in figure 8, except for the fact that the periodicity along the wire has doubled. Defects such as vacancies or adatoms induce some other local restructuring. A second appearance of the $5a_0$ wire is shown in figure 7(b) and (c). Here the appearance is different at -0.2 V and $+0.2$ V. At -0.2 V, the image consists of faint row segments running perpendicular to the growth direction. They are spaced by $2 \times a_{Si}$. At $+0.2$ V the image is more checker board like. A higher resolution STM image, presented in panel (d) of figure 7, shows one more surface arrangement for the $5a_0$ wire. Finally, figure 7 (e) and (f) show some segments of the $6a_0$ and $7a_0$ wires. Both wires have (2×1) reconstructed surfaces with a period doubling along the growth direction. Note that the surface reconstructions of the $5a_0$ wire in panel (c) and the $6a_0$ wire in panel (e) are similar.

STM is a local electronic structure probe and therefore the STM images contain both topographical and electronic structure information [34]. It is well known that STM images of the Si(100)(2×1) dimer reconstruction are strongly bias-dependent, as electrons tunnel into different orbitals at different bias [35]. Here, we also notice a significant change in the appearance of the wires, depending on the bias polarity. (The images are much less sensitive to the bias magnitude). Figure 7 (g) shows the apparent height of the $3a_0$, $4a_0$ and $6a_0$ wires as a function of applied voltage. The heights are measured relative to the wetting layer. We emphasize the apparent height difference between the $3a_0$ nanowire and all the others, especially at negative bias, which amounts to $0.4 \text{ \AA}$ in average. Same height difference is observed between $3a_0$ and $5a_0$. The height histogram, presented in the inset of figure 7 (g), clearly distinguishes the $3a_0$ wire from the others at negative bias. The $4a_0$ and $6a_0$ wires are indistinguishable in such histogram due to their similar apparent heights. Note that the height variations with bias are purely an electronic effect.

Figure 8 shows the calculated structure for a $5a_0$ wire based on the previously introduced model of the $3a_0$ and $4a_0$ wires. The relaxed structure of the $5a_0$ wire shows a small increase in height ($+0.07 \text{ \AA}$) from the $3a_0$ wire due to a slight vertical relaxation of the central Si atoms, which is qualitatively consistent with the experimentally observed height variation. The simulated STM images for the $5a_0$ wires are calculated at various biases used in the experiment and presented in figure 8 panels (c) to (h). Note at biases larger than 1 V, the appearance of the wire surface is independent of the bias magnitude. At lower biases (0.4 V), greater detail can be seen in the images but overall the appearance is similar as to the high bias case, i.e. the $5a_0$ wire surface consist of three dimer rows separated by two channels where part of the yttrium atoms reside. The slight symmetry breaking across the wires visible in the STM images results from the supercell choice, which is not perfectly comensurate with the $5a_0$ structure. The silicon dimers are separated by $1a_{Si} = 0.384 \text{ nm}$ along the wire direction.

Visual inspection of the experimental images (figure 7) and calculated ones for the $5a_0$ wires (figure 8) indicates poor agreement for this model. The reason is obvious because the model doesn't reproduce the period doubling along the $5a_0$ wire. In fact, all wires broader than $5a_0$ exhibit doublings of the periodicity along the wire direction, which include the $c(2 \times 2)$ surface reconstruction reported for Dy silicide nanowires [5]. To identify the origin of these

doublings we considered three possibilities: (i) spontaneous Peierls-like reconstructions, (ii) adatoms of silicon, (iii) ordering of yttrium vacancies. The large variety of possibilities precludes an exhaustive search. Instead our search was guided based on observing how specific structural changes influence the simulated STM data.

We searched for possible spontaneous reconstructions by making small random perturbations to the geometry, but always recovered the starting unreconstructed geometry. Trials with extra Si atoms on top of the wires demonstrated that this geometry was not unreasonable. However, in all cases the additional height (relative to the $3a_0$ wire) turned out to be much larger than observed experimentally, ruling out adatoms as the source of the observed reconstructions.

We tested fifteen $\times 2$ structures with yttrium deficiency. Note that *silicon* deficiency is very common for bulk silicides with the AlB_2 structure. However, the present wires are formed under silicon-rich conditions. Figure 9 illustrates simulated STM images of three $5a_0$ wires having yttrium atoms removed following a specific pattern. The images show similar features for potentials up to 1.2 V. However, since the larger potential images are more converged (more states available at a given Brillouin zone sampling) we are focusing on those. The wires are labeled according to their yttrium content. The '11111-11111' wire represents the 'perfect' wire where the yttrium atoms fill all the available yttrium sites as indicated in the cross-sectional view of Figure 8(a); yttrium vacancies will be marked by zeros. Note that there are two cross-sectional population sequences within a $\times 2$ unit cell. Removal of select yttrium atoms in the channels or those that would normally be located under the silicon dimer rows can create a rich diversity of surface reconstructions (figure 9). Such yttrium deficiency creates the $2 \times a_S$ periodicity seen in experiment. Indeed, the STM simulation of the '01010-10101' checker board structure in figure 9(a) resembles the high-resolution image in figure 7(c). Note that such vacancy ordering would produce a $c(2 \times 2)$ pattern in wider structures. On the other hand, our combined STM and computational results indicate that the wires can display significant vacancy disorder.

To determine the electronic properties of the individual wires we rely on STS. STS was performed at room temperature on isolated wires of different widths and the dI/dV spectra are compared with the DFT-calculated density of states (DOS). Figure 10(a) displays the calculated projected density of states (PDOS) for the four $5a_0$ wires discussed above. The measured STS spectra for a $5a_0$ wire are shown in panel (b), together with some of the theoretical PDOS spectra. Here, the two experimental spectra represent different parts of the wire. They differ primarily in the energies of the empty bands, while the filled bands are located at approximately the same energies. Again, this suggests inhomogeneity within the nanowire. The nonzero slope at the Fermi energy in the I/V spectra indicates that wires are metallic. This was further verified by our transport measurements [28]. Our experimental findings are in agreement with recent ARPES measurements performed on Er and Dy wires showing metallic band dispersions [11].

The next step in the determination of the structure of the wire is to ascertain which of the theoretically proposed structures display the same electronic properties as the ones measured in the experiment. To quantify the agreement between the experimental and the calculated DOS of the wires, we previously proposed [15] to use the Pendry R-factor [36] because it emphasizes peak positions rather than peak intensities; the latter are strongly dependent on the tip conditions. The Pendry R-factor was first introduced LEED I-V analysis to quantify the agreement between the experimental and calculated positions of Lorentzian diffraction profiles. The R-factor ranges from 0 to 1 approaching zero when experiment and theory are in perfect agreement. The computed R-factor values for the two thinnest YSi_2 nanowires are $R(3a_0) = 0.4$, $R(4a_0) = 0.5$ [15, 37]. The factor values for the $5a_0$ wires, considering

the 'perfect' wire as well as the three Y deficient wires, are presented in table 1. According to this reliability factor, the experimental curves are best reproduced by the '11111-11111' and '01010-10101' wires. The PDOS of these two wires are plotted in figure 10(b) together with the experimental dI/dV's. The best agreement is met between the experimental dI/dV II curve and the PDOS of the '01010-10101' structure. Note, for instance, that the peak at about -0.65 eV in the PDOS is reproduced by a weak shoulder in the dI/dV II spectrum. The dI/dV I spectrum and the '11111-11111' PDOS are also in quite good agreement for the higher energy states above and below the Fermi level. However, neither case can claim good agreement in the vicinity of the Fermi level (zero bias), which could possibly be related to the localized nature of the conduction electrons of these wires [28].

The lowest R-factor (0.39) is obtained for '01010-10101' wire. Moreover this sequence also displays the observed checker board pattern observed in STM, making this the most likely structure. The '11100-00111' structure has a slightly worse R-factor than the '01010-10101' but it is still worth considering especially because the simulated STM data are also close to some of the experimental images (see figure 7(d)).

3.2.2. Wire assemblies—Increased yttrium coverage leads to nanowire agglomeration and wire-bundle formation as was mentioned in the first section and reported for other silicides [5, 31, 38]. The interwire distance within a given bundle is one silicon lattice constant, i.e., 0.384 nm. Wire-bundles can also be created at low coverage if the sample temperature is increased few tens of degrees (650 °C) during growth or by a short post-growth annealing step (figure 3 (c)). While both preparation schemes mentioned above lead to wire-bundle covered sample, the organization of bundles differs in the two cases. On one hand at increased yttrium coverage and moderate substrate temperatures there are more nucleation centers on the terrace, resulting in higher wire density (figure 11 (a)). These thinner bundles all terminate at the step edges, hence they do not cross, forming locally parallel array architectures as seen in Ce silicide nanowires [39]. On the other hand at higher substrate temperatures, increased surface diffusion leads to formation of "fat" bundles that often run across the step edges into orthogonal domains where they terminate at an orthogonal wire creating "Tee" junctions, as can be seen in figure 2(c).

Figure 11 (a) shows a STM image of wire-bundles with the wetting layer reconstruction in the background formed at 0.6 ± 0.1 ML Y coverage, 620 °C, and no post-annealing. The bundles consist on average of 2-3 nanowires and are evenly distributed across the surface. Nucleation of a second layer silicide is best developed on the wider wires inside the bundles. Occasionally, deformations in the wetting layer are seen close to wide bundles. One can often observe abrupt junctions along the bundle length with wires having different widths on both sides of the junction. Exceptional wide bundles as illustrated in figure 11 (b), can be created at 650 °C with no wetting layer remaining.

The STM image in the figure 11 (c) illustrates a two-wire bundle formed by a $3a_0$ and a $5a_0$ wire. A total-energy-minimized structure of a $3a_0$ - $5a_0$ bundle is indicated in panel (d) of figure 11. Inside the bundle (figure 11 (c)), the wires look similar to isolated wires, displaying the same top-layer reconstructions as mentioned in the previous section. A line profile measured across the bundle is shown in panel (e) for $+0.2$ V and -0.2 V. The apparent height difference between the $3a_0$ and $5a_0$ wire at negative bias remains unchanged when the wires form a bundle. All the facts presented above indicate that wires keep their properties unchanged upon bundle formation. However, at slightly higher coverages the bundles are abundant, indicating a lower formation energy relative to the single wires.

To explain the formation of bundles we performed an analysis of their formation energy relative to that of separated single wires. We computed the energies of pairs of wires at

various spacings, within the confines of a supercell containing two formula units of each wire. Figure 12 plots the supercell energy versus the wire spacing index. An index of 2($3a_0$) or 3 ($5a_0$) corresponds to adjacent wires, while a wire index of 5 corresponds to the two wires ($3a_0$ or $5a_0$) being maximally and evenly separated. Lower energies indicate a more preferred structure. The energies are not symmetric due to the surface Si reconstructions between the wires that break the symmetry of the supercell. The energies are lower when the wires are adjacent, indicating that a $3a_0$ - $3a_0$ or $5a_0$ - $5a_0$ wire combinations prefers to be adjacent, their total energy being lower by at least 0.2 eV per paired formula unit than for the isolated wires. Similar results were found for mixed bundles of $3a_0$ and $5a_0$ wires. This indicates that the likely origin of the bundling is the recovery of interfacial energy (both strain and electronic), primarily from the nanowire silicon, when wires are adjacent. In the absence of sufficient kinetic barriers, this will drive formation of progressively larger wires or islands.

4. Summary and Conclusions

YSi₂ nanostructures presented here were created via the process of self-assembly on heated Si(100)(2 × 1) substrates. The various stages of yttrium silicide growth were investigated in detail with scanning tunneling microscopy and spectroscopy, performed at room temperature, and first-principles density functional theory calculations. Ultrathin nanowires start growing upon completion of a Si(100)(2×7)-Y reconstructed wetting layer and only exist over narrow ranges of coverage ($0.4 < \theta < 0.5$) and temperature (600 to 630 °C). Higher growth temperatures or post-growth annealing results in the formation of thick wire bundles and ultimately 3D islands. Except for the thinnest $3a_0$ and $4a_0$ nanowires, YSi₂ nanophases exhibit various surface reconstructions that can be attributed to the (local) ordering of yttrium vacancies, indicating that these phases are non-stoichiometric. Wire-wire interactions result in the formation of nanowire bundles, the thickest of which extend over many microns, forming a robust network of conducting wires that could possibly be employed in nanodevice applications.

Acknowledgments

The experimental research was sponsored by NIH Grant No. R01HG002647 and NSF Grant No. DMR-1005488. The computational research (PRCK) used resources of the National Energy Research Scientific Computing Center, National Center for Computational Sciences, and the Center for Nanophase Materials Sciences at ORNL, which are all sponsored by the DOE Office of Science.

6. References

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Figure 1. (Color online). (a) STM image showing an incomplete (2×7) wetting layer. The two types of steps, S_A and S_B , and the respective terraces, T_A and T_B , are indicated. Inset illustrate an enlarged area for a better visualization of the reconstruction with the Si dimer rows in the background. The image was recorded at 1.5 V, 0.1 nA. (b) and (c) Filled-state (-1.3 V) and empty-state ($+1.3$ V) STM images of a complete wetting layer. Arrows point to extra rows on top of the (2×7) atom rows. The image size is $27 \text{ nm} \times 27 \text{ nm}$.

Figure 2.

(Color online) STM images illustrating different sample morphologies at different coverages and growth temperatures. (a) In the low-coverage regime the wires are found to be isolated. (b) With increasing coverage ($\Delta\theta = 0.1$ ML), wires self-assemble into bundles. (c) Increased surface diffusion ($\Delta T = 30$ °C) results in wider and extremely long bundles. The imaging parameters are 0.1 nA and -1.8 V for (a), 1.8 V for (b) and 2.2 V for (c).

Figure 3.

(Color online) STM images illustrating the different sample morphologies at fixed coverage ($\theta = 0.35$ ML) but different growth temperatures. (a) At 600 °C the surface is almost completely covered with the (2 $\times$ 7) surface reconstruction and nanowires are still absent. (b) At slightly higher temperature, thin nanowires form and structural deformations in the wetting layer can be observed. (c) At 650 °C increased surface diffusion leads to wider and extremely long bundles and the (2 $\times$ 7) reconstruction has almost disappeared. The tunneling parameters are 0.07 nA, 1.4 V in (a), -1.8 V in (b) and 1.4 V in (c).

Figure 4.

(Color online) YSi_2 islands. (a) STM image showing wire-bundles and a YSi_2 Type I island. (b) Atomic resolution image ($10\text{ nm} \times 9\text{ nm}$) of the surface of the Type I island illustrating the $c(2 \times 2)$ surface reconstruction. (c) STM image showing three Type II YSi_2 islands. Inset shows an atomic-resolution image ($20\text{ nm} \times 14\text{ nm}$) of the Type II island displaying a $c(2 \times 2)$ surface reconstruction. Arrows indicate the orientation of the island's edges. Tunneling parameters are 0.1 nA and 2 V for (a), -1 V for (b) and -1.2 V for (c). Nominal coverage is $0.6 \pm 0.1\text{ ML}$.

Figure 5.
(Color online) YSi_2 structures observed at different yttrium coverages and substrate temperatures. Solid colors indicate the dominant structures while stripes indicate mixed phases (see text).

Figure 6.

(Color online) Characterization of the thinnest YSi_2 nanowires from STM and DFT. (a) and (c) display the experimental (-1.6 V, 0.18 nA) and the simulated (1.2 V) STM images of the $3a_0$ wire, respectively. (b), (d) and (e) are the experimental (3.5 nm $\times$ 2.2 nm, 20 mV, 0.1 nA) and simulated STM images of a $4a_0$ wire, respectively. [(d) represents the filled states (-1.2 V) and (e) the empty states (1.2 V)]. Panels (f) and (g) show cross-sectional views of the total-energy-minimized structures. Silicon atoms are shown in yellow and yttrium atoms are shown in red.

Figure 7.

STM images of 'higher-multiple' wires, showing different surface reconstructions. (a) STM image (-1.7 V, 0.1 nA) of a 20 nm long wire segment of a $5a_0$ wire showing local restructuring near defects. (b) and (c) A $5a_0$ wire segment measured at 40 K at -0.2 V and $+0.2$ V, respectively, with doubled periodicity along the wire; (d) STM image (1 V, 0.1 nA) showing a $5a_0$ wire fragment indicating a different reconstruction than seen in panel (c). (e) and (f) wire fragments of $6a_0$ (20 mV, 0.1 nA) and $7a_0$ (-0.8 V, 0.1 nA) wires. (g) Graph showing the apparent height for three wire-widths versus bias voltage at 0.1 nA. The inset displays height histograms for the three wires.

Figure 8.

(Color online) Cross-sectional view (a) and side view (b) of the total-energy-minimized structure of the $5a_0$ wire. The silicon atoms are shown in yellow and the yttrium atoms are shown in red. Simulated STM images obtained for the structure in (a) are illustrated at different voltages: (c) -0.4 V, (d) $+0.4$ V, (e) -1.2 V, (f) $+1.2$ V, (g) -1.7 V and (h) $+1.7$ V.

Figure 9.
(Color online) Simulated STM images of Yttrium deficient $5a_0$ wires.

Figure 10.

(Color online) Electronic properties of the $5a_0$ wires. (a) PDOS spectra for the 'perfect' $5a_0$ wire and three Y deficient wires that are presented in figure 8 and 9, respectively. (b) Experimental dI/dV spectra for the $5a_0$ wire plot together with the calculated PDOS for two wires (see text). The curves are vertically shifted for better visualization. Tunneling set point for the dI/dV spectra is 0.1 nA, -1.6 V.

Figure 11.

(Color online) Wire assemblies on Si(100). (a) STM images ($250 \text{ nm} \times 200 \text{ nm}$, 50 pA , 1.8 V) showing YSi_2 wire bundles formed by increasing the yttrium coverage at 620°C . (b) STM image showing a 35 nm wide bundle formed at 650°C ; the brighter rows are segments of a second silicide layer. (c) High resolution STM image (-0.2 V , 0.1 nA) of a $3a_0-5a_0$ wire-bundle. A line profile measured across this bundle at $+0.2 \text{ V}$ and -0.2 V is presented in (e). (d) Total-energy-minimized structure of a $3a_0-5a_0$ bundle. The spacing between the wires is $1a_0$. The silicon atoms are shown in yellow and the yttrium atoms are shown in red.

Figure 12.

(Color online) Computed energies of bundled wires consisting of pairs of either $3a_0$ or $5a_0$ wires. The energies are lowest when the wires are adjacent. The index gives the relative location of the second wire in the supercell: at 2 & 8 ($3a_0$) or 3 & 7 ($5a_0$) the wires are adjacent. At 5 they are maximally separated.

Table 1R-factor values for the $5a_0$ YSi₂ nanowires

YSi ₂ NW	dI/dV I	dI/dV II
11111-11111	0.56	0.76
01010-10101	0.90	0.39
11100-00111	0.74	0.56
11111-01010	0.85	0.68