Improvement of polycrystalline silicon wafer solar cell efficiency by forming nanoscale pyramids on wafer surface using a self-mask etching technique

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The creation of nanostructures on polycrystalline silicon wafer surface to reduce the solar reflection can enhance the solar absorption and thus increase the solar-electricity conversion efficiency of solar cells. The self-masking reactive ion etching (RIE) was studied to directly fabricate nanostructures on silicon surface without using a masking process for antireflection purpose. Reactive gases comprising chlorine (Cl_2), sulfur hexafluoride (SF_6), and oxygen (O_2) were activated by radio-frequency plasma in an RIE system at a typical pressure of 120–130 mTorr to fabricate the nanoscale pyramids. Poly-Si wafers were etched directly without masking for 6–10 min to create surface nanostructures by varying the compositions of SF_6 , Cl_2 , and O_2 gas mixtures in the etching process. The wafers were then treated with acid ($\text{KOH}:\text{H}_2\text{O} = 1:1$) for 1 min to remove the damage layer (100 nm) induced by dry etching. The damage layer significantly reduced the solar cell efficiencies by affecting the electrical properties of the surface layer. The light reflectivity from the surface after acid treatment could be significantly reduced to $<10\%$ for the wavelengths between 500 and 900 nm. The effects of RIE and surface treatment conditions on the surface nanostructures and the optical performance as well as the efficiencies of solar cells will be presented and discussed. The authors have successfully fabricated large-area ($156 \times 156 \text{ mm}^2$) subwavelength antireflection structure on poly-Si substrates, which could improve the solar cell efficiency reproducibly up to 16.27%, higher than 15.56% using wet etching. © 2013 American Vacuum Society. [<http://dx.doi.org/10.1116/1.4795862>]

I. INTRODUCTION

Among all renewable energy resources, solar energy is the most abundant energy source. At present, crystalline silicon wafers remain the most widely used materials in the solar cell industry with relatively high efficiencies and reasonable costs to convert solar energy into electric energy. However, polycrystalline and single crystalline silicon wafers have high solar reflectivity, around 40%, in the wavelength range of 500–900 nm. In order to improve the cell efficiency, light trapping structures such as surface texturing¹ and antireflection multilayer coatings² can be applied to the fabrication of solar cells. The surface texturing in crystalline silicon solar cells can reduce light reflection at the wafer surface. As the dimensions of surface textures are larger than or comparable to the wavelengths of incident photons, the texture will induce light reflection between the surface of textures, resulting in light trapping and reducing light reflection. As the dimensions of surface textures are much smaller than the wavelengths of incident photons, antireflection will be observed due the gradual increase of refractive index for photons entering the nanostructured silicon surface based on homogeneous media theory. As a result, the cell efficiency can be improved due to light trapping or antireflection.^{3–5} By reducing the light reflectance of the silicon surface, surface texturing decreases the

loss of solar intensity, and therefore increases the short circuit current and the efficiency in the solar cells. The wet texturing commonly used in single crystal silicon (100) solar cell process by using alkaline or acidic solution.^{6–8} The dry etching method such as laser-structuring,⁹ mechanical diamond saw cutting,¹⁰ photolithographically defined etching,¹¹ porous-Si etching,¹² and maskless reactive ion etching (RIE) etching^{13–16} have recently been studied to prepare the ideal surface textures. In this paper, we adjust the compositions of gas mixtures as well as process conditions in reactive ion etching process to achieve self-masking for fabricating the nanoscale pyramids over a large area within a short process time. The self-masking etching improves the solar cell efficiency without using nanoscale lithography and masking, and is particularly suitable for manufacturing large-area solar cells at low costs. The process should be suitable for the mass production of antireflective solar cells.

II. EXPERIMENT

P-type crystalline silicon wafers, with a size of $156 \times 156 \text{ mm}^2$ and a thickness of $200 \mu\text{m}$, are used as the substrates. These substrates were etched in 20 wt. % KOH solution at 65°C for 300 s. In RIE processes, radio-frequency (RF) power was applied to the substrate electrode inducing a negative dc self-bias on the substrate. The gas reactants for RIE comprised chlorine (Cl_2), sulfur hexafluoride (SF_6),

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FIG. 1. (Color online) Experimental procedures for the fabrication of solar cell devices.

and oxygen (O_2). After plasma etching, the substrate was immersed in 5 wt. % KOH for 1 min to etch away the damage layer due to RIE process. Both the front and the rear sides of the substrate were treated with phosphorus diffusion in $POCl_3$ environment at $800^\circ C$ for 40 min to about $70 \Omega/sq$ for a diffusion thickness of around $0.2\text{--}0.5 \mu m$, followed by cleaning with 5 wt. % hydrogen fluoride (HF) solution for 20 s. To etch away the p-type vertical edges of the wafer for isolating both sides, the substrate was floated on the surface of liquid acid solution (5 wt. % HF + 25 wt. % HNO_3 + 20 wt. % H_2SO_4). Plasma enhanced chemical vapor deposition using SiH_4 and NH_3 reactants was employed to deposit

a SiN_x film of about 80 nm in thickness as the antireflective layer. The front side of the substrate was coated with a silver paste of around $20 \mu m$ in thickness and $100 \mu m$ in width as the Ag electrodes by screen printing. The rear side was coated alternately with aluminum paste and silver paste. Finally, the substrate was baked at $550^\circ C$ for 40 s. The solar cell devices were product process in Fig. 1.

III. RESULTS AND DISCUSSION

The surface texture could be varied by controlling several process parameters including the composition of gas

FIG. 2. (Color online) Substrates etched under various SF_6 flow rates: (a) 3.25 sccm, (b) 6.5 sccm and (c) 9.75 sccm; with the Cl_2 and O_2 flow rates at 25 and 10 sccm, respectively, an RF power of 100 W and an etching time of 6 min.

mixture, RF power, and etching time of RIE system. Figure 2 shows the picture of the substrates etched under various SF₆ flow rates with the Cl₂ and O₂ flow rates fixed at 25 and 10 sccm, respectively, the RF power of 100 W, and an etching time of 6 min. The substrate surface gradually turned black with increasing the SF₆ flow rate. Particularly, the surface of polysilicon wafers etched at SF₆ = 6.5 sccm [Fig. 2(b)] completely turned black after visual inspection. The sample etched at SF₆ = 9.75 sccm in Fig. 2(c) was slightly lighter in color than that in Fig. 2(b). Therefore, the lowest reflectivity was obtained for an optimized SF₆ flow rate at 6.5 sccm in Fig. 2(b) under the above conditions.

The effects of O₂ flow rate in RIE process on the reflectance of substrate were studied, as shown in Fig. 3 for the Cl₂ and SF₆ flow rates of 25 and 6.5 sccm, respectively, at an RF power of 100 W for an etching time of 6 min. The darkness of the substrate increased with the increase of O₂ flow rate from 5 sccm, as shown in Fig. 3(a), reaching the darkest

TABLE I. Experimental conditions of self-masking RIE process.

No.	Power (W)	Time (min)	Cl ₂ (sccm)	SF ₆ (sccm)	O ₂ (sccm)	Pressure (mTorr)
A49	300	6	25	6.5	15	120
A50	200	10	25	6.5	15	130
A51	300	10	25	6.5	15	120
A53	300	10	25	6.5	10	130

surface at 10 sccm O₂, as shown in Fig. 3(b), and then decreased for a further increase of O₂ flow rate to 15 sccm, as shown in Fig. 3(c). The SEM images in Fig. 3 provide us information on surface textures. At the O₂ flow rate of 5 sccm, the nanopylramids were not well formed yet. For the O₂ flow rates at 10 and 15 sccm, the high-aspect-ratio nanopylramids with heights higher than 100 nm were well formed. The shapes of nanopylramids formed at 10 sccm O₂ flow were slightly better than those at 15 sccm O₂ flow. Due to

FIG. 3. (Color online) Substrates etched at various O₂ flow rates: (a) 5 sccm, (b) 10 sccm, (c) 15 sccm with Cl₂ and SF₆ flow rates at 25 and 6.5 sccm, respectively, an RF power of 100 W, and an etching time of 6 min.

FIG. 4. (Color online) SEM images of polycrystalline silicon wafers etched by RIE at various conditions described in Table I.

redeposition, the top surface of the nanopyramid arrays at a high O₂ flow rate was covered with a thin layer of silicon oxide, which could be easily removed by HF acid. Therefore, among all three O₂ flow rates, the surface etched at an O₂ flow rate of 10 sccm has the lowest reflectivity under 100 W RF plasma and 6 min etching. The self-masking effect during RIE was clearly observed by the formation of nanopyramid arrays due to different etching rates for silicon oxide and silicon under the reactive fluorine and chlorine species. The

formation and shapes of nanopyramids were therefore highly dependent on the compositions of gas mixtures during RIE.

To improve antireflection properties, we further increase the RF power or the etching time during RIE. With the processing conditions described in Table I, the SEM images of the etched poly-silicon wafers are shown in Fig. 4. As shown in Fig. 4(a) (300 W, 6 min) and Fig. 4(b) (200 W, 10 min), the sizes of pyramids were about 100 nm in height and 50 nm in width for 15 sccm oxygen flow. However, thin

FIG. 5. (Color online) Light reflectance measured as a function of the wavelength for (a) the original poly-Si substrate before RIE and (b) the substrates etched by RIE under several conditions described in Table I.

FIG. 6. (Color online) Optical images of the substrates etched by RIE at various process conditions describe in Table II followed by KOH etching for 1 min.

layers were redeposited on top of the nanopyramid arrays. With increasing both the RF power to 300 W and the etching time to 10 min for 15 sccm O_2 flow, the heights of pyramids were slightly increased to the range of 100–150 nm with a width of 50 nm, as shown in Fig. 4(c). By decreasing the O_2 flow rate down to 10 sccm at the same RF power and etching time as those in Fig. 4(c), the sizes of pyramids evidently increased up to about 300 nm in height and 100 nm in width as shown in Fig. 4(d). Besides, surface layer deposition on top of nanopyramid arrays was much less for Figs. 4(c) and 4(d). The reflectance spectra of the poly-silicon wafers after RIE were measured by ultraviolet-visible spectroscopy and shown in Fig. 5. The reflectance of original poly-silicon (before etching) approached 40% in the range from 500 to 900 nm, while the reflectance of the substrates after RIE was reduced to below 7% in the same wavelength range. Figure 5 indicated that the O_2 composition during RIE was the most critical parameter in fabricating the low-reflectivity substrates, although an appropriate increase of RF power or etching time is also effective in reducing the reflectivity. The self-masking RIE was resulted from the small amount of slow-etching silicon oxide formed in the majority of fast-etching silicon. The lowest reflectivity achieved was 2% for A51 sample [Fig. 4(c)] with an RF power of 300 W, etching time of 10 min, and 15 sccm O_2 flow.

After the RIE process, the surface of poly-silicon wafers was damaged inducing poor electric conductivity and deterioration of solar cell efficiency. Therefore, 5 wt. % KOH solution was always used to remove the damage layer on the etched substrates. The pictures in Fig. 6 show that the deep darkness of the poly-silicon substrates after RIE was reduced by KOH etching, indicating that antireflection was deteriorated by KOH etching. The reflectance of the substrates

after KOH etching was measured by ultraviolet-visible spectrometer and shown in Figure 7. The reflectance for A50 (less than 7% after RIE) was increased to higher than 20% by KOH etching. The nanopyramids of A50 were 100 nm in

FIG. 7. (Color online) Reflectance measured as a function of wavelength for the substrates etched by RIE at several process conditions described in Table I, followed by KOH etching for 1 min.

Fig. 8. (Color online) Optical images of solar cell devices fabricated by (a) wet etching only (b) RIE process, followed by 5 wt. % KOH etching to remove the surface damage layers induced by RIE.

height and 50 nm in width. As shown in Fig. 6(b), KOH etching obviously increased the reflectivity by damaging the nano-pyramids, particularly those with small heights and widths. On the other hand, the originally not-so-dark A53 had the lowest reflectance, lower than 15%, after KOH etching, since the pyramids of A53 had the largest heights and widths (300 and 100 nm, respectively) before KOH etching, and were more resistant to KOH etching.

The solar cell efficiencies of the poly-silicon wafers after various RIE treatments and subsequent KOH etching were measured and shown in Table II. The nanopyramids formed on polycrystalline silicon wafer surface were shown to effectively reduce the solar reflection and enhance the solar cell efficiencies to the values higher than 16%. On the other hand, the solar cell efficiency with surface texturing by wet etching was only 15.56%, and not highly reproducible. The solar cell with lower surface reflectance after KOH etching always had higher solar cell efficiency. A53 had the lowest reflectance after KOH etching and the highest solar-electric conversion efficiency up to 16.27%. The solar cell devices using the wet etching method to texture the surface had dark blue surface, as shown in Fig. 8(a). On the other hand, large-area solar cell devices with completely black surface can be fabricated reproducibly and uniformly across the whole wafer surface for a size of $156 \times 156 \text{ cm}^2$, as shown in Fig. 8(b), under RIE conditions as follows: an RF power of 300 W, etching time of 10 min, Cl_2 , SF_6 , and O_2 flow rates of 25, 6.5, and 10 sccm, respectively. The self-masking RIE process was found to be reproducible in fabricating nanopyramids for reducing light reflection to increase solar cell efficiency up to 16.27%, compared with 15.56% using wet etching.

TABLE II. Comparison of solar cell efficiency under several process conditions.

	V_{oc} (mV)	J_{sc} (mA/cm ²)	FF (%) °C	Efficiency (%)
Wet etching	0.611	33.07	77.02	15.56
A49	0.608	34.81	76.49	16.19
A50	0.606	34.61	76.08	16.08
A51	0.609	34.78	76.61	16.23
A53	0.609	34.78	76.79	16.27

IV. SUMMARY AND CONCLUSIONS

In this study, the effects of gas composition, RF power, and etching time in self-masking RIE process were studied to optimize the antireflection results. The nanostructures formed on polycrystalline silicon wafer surface could be modulated by adjusting self-masking RIE process conditions to tune the amount of slow-etching silicon oxide in fast-etching silicon matrix. We have successfully fabricated the large-area ($156 \times 156 \text{ mm}^2$) antireflective surface of solar cell devices by self-masking RIE process. The lowest-reflectivity surface ($<15\%$) were fabricated at an RF power of 300 W, an etching time of 10 min, the Cl_2 , SF_6 , and O_2 flow rates of 25, 6.5, and 10 sccm, respectively, followed by 5 wt. % KOH solution for 1 min to remove the surface damage layer. The solar cell efficiency could reach 16.27%, compared with the value of 15.56% using wet etching. The self-masking RIE process for fabricating nanopyramids to increase solar cell efficiency was found to be highly reproducible. On the other hand, the efficiency of solar cells textured by wet etching method was lower and not so reproducible.

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