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Component Level Modular Design of a Solid State X-ray Image Intensifier for an MxN Array

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Abstract

The Solid-State X-ray Image Intensifier (SSXII) is a novel dynamic x-ray imager, based on an array of electron-multiplying CCDs (EMCCDs), that can significantly improve performance compared to conventional x-ray image intensifiers (XIIIs) and flat panel detectors (FPDs). To expand the field-of-view (FOV) of the SSXII detectors while maintaining high resolution, a scalable component level modular design is presented. Each module can be fit together with minimum dead-space and optically coupled to one contiguous x-ray converter plate. The electronics of each of the modules consists of a detachable head-board, on which is mounted the EMCCD, and a driver board. The size of the head-boards is minimized to ensure that the modules fit together properly. The driver boards connect with the head-boards via flat cables and are designed to be plugged into the main mother-board that contains an FPGA chip that generates the driving clock signals for the EMCCDs and analog-to-digital converter (ADC). At the front-end, a high speed ADC on each of the driver boards samples and digitizes the EMCCD analog output signal and an extensible modular digital multiplexer back-end is used to acquire and combine image data from multiple modules. The combined digital data is then transmitted to a PC via a standard Camera Link interface. Eventually, this modular design will be extended to a 3x3 or larger array to accomplish full clinical FOVs and enable the SSXII to replace conventional lower-resolution XIIIs or FPDs.

I. Introduction

X-ray imaging is widely used as a powerful technique for diagnosis and invasive treatment in the medical field. Current state-of-art medical x-ray detector technologies, including x-ray image intensifiers (XIIIs) and flat panel detectors (FPDs), have inherent limitations [1]. XIIIs convert light from the x-ray converting phosphor to electrons, which are focused and accelerated across a large potential difference to produce an intensified image of light photons with large and variable gains. XIIIs are physically cumbersome and suffer from various problems such as veiling glare, pincushion distortion due to the curved x-ray sensitive phosphor and S distortion due to the earth's magnetic field. FPDs employ an array

of solid state photodiodes with thin film transistors (TFT) to digitize the electronic signal from the x-ray/light sensitive region and thus supersede XIs by eliminating the veiling glare and distortion problems. However, current FPD technology lacks sufficient signal amplification and the performance of FPDs degrades with low exposure procedures during which the excessive electronic instrumentation noise and poor signal to noise ratio is severe. Moreover, FPDs have image lag or persistence and ghosting due to charge retention in the photodiode TFT array. In addition, for both XIs and FPDs, the spatial resolution is limited and the capability is roughly 3 line pairs per millimeter (lp/mm) [2]. To overcome these limitations, our group has been developing a high resolution, high sensitivity Solid State X-ray Image Intensifier (SSXII) from the component level. The SSXII can provide real-time, high spatial-resolution, and low noise (hence, high dynamic range) images even at very low exposures because of the high variable on-chip gain of the EMCCDs [2].

To achieve larger FOVs and provide the most flexibility in building an optimized system, the modularized SSXII detector is designed and built from the component level. Each module that forms the array of the SSXII detector contains a fiberoptic taper (FOT) that focuses light from an x-ray converting phosphor, such as structured CsI(Tl), onto an EMCCD. The large end of the FOTs are machined to fit together with minimum dead-space and optically coupled to one contiguous x-ray converter plate. The small ends of the FOTs are coupled onto individual EMCCD sensors as shown in Fig. 1.

II. System Design

A. Optical Head Design

The optical portion of the SSXII, including the FOTs and CsI(Tl) phosphor plate, is enclosed in an optically-black box shown in Fig. 2. The EMCCDs are mounted on the back plate of the box and can be adjusted horizontally and vertically using positioning screws through the mounting holes on the EMCCDs. The center-to-center distance between the adjacent EMCCDs should be equal to the side length (27.9mm) of the large end of the FOTs. The screws on the side plates are used to support the FOTs. The optical head shown in Fig. 2 can support up to a 2×2 modular array with a FOT ratio of 3.3 to 1.

B. Electronic Driver Design

Similar in function to an image intensifier, the EMCCD has a variable on-chip gain (up to a factor of 2000), which is achieved by an impact ionization process when electrons are transferred through higher voltage potential gates than are normally used for CCDs [3]. This electron multiplying gain enables the EMCCD to reduce the relative read noise to less than 1e- with moderate gains [4] thus boosting the signal above the noise floor even at high pixel rates.

EMCCDs require dedicated voltage and clock signals to obtain the best charge transfer efficiency. However, the higher voltage potential and higher clock switching speed may cause problems in driver design, especially the charge multiplication gate (CMG) driver signal, which may temporarily generate excessive heat.

We offer a scalable modular design which separates the clock driver circuit from the EMCCD chip. The electronics of each of the modules consists of a driver-board and a detachable head-board, on which is mounted the EMCCD (Fig. 3 and 4).

- The size of the head-boards has been minimized to the dimensions of the EMCCD to enable use of smaller FOT magnification ratios. Damping resistors are included on the head-boards to reduce clock induced charge (CIC) – a source of vertical-line artifacts in the image. The cut-out holes on the head-boards allow placement of a

0.5"; by 0.5" heat-sink that has highly conductive aluminum fins underneath the built-in EMCCD peltier-cooler;

- The driver boards connect to the head-boards via flat cables and are designed to be plugged into the main mother-board. An on-board heat-sink is used to help dissipate the excessive heat generated from the higher voltage, high-switching-speed CMG driver circuit. A high speed 12-bit ADC (72dB dynamic range), which implements 36 MHz correlated double sampling (CDS) and supports maximally 36fps for each module, is placed close to the EMCCD output on the driver boards;
- The mother-board contains an FPGA running at 280MHz to generate all clocking signals. The phase of each driver signal for each module is independent and adjustable to finely tune and optimize the EMCCD clock signals;
- The power-board has a set of positive and negative voltage regulators to change the amplitude of each output driver signal. A 10-bit digital potentiometer is applied to adjust the CMG voltage accurately.

C. Image Acquisition

For a single module camera, the standard Camera Link port is sufficient to acquire the image with a maximal clock frequency of 85 MHz. For a multiple-module camera, an extensible modular digital multiplexer back-end can be used to acquire and combine image data from multiple modules. This multiplexer can selectively disable/enable a desired subset of modules and thus it can acquire pixels from an arbitrary size modular array for larger FOVs. The combined digital data is then transmitted to a PC via a standard Camera Link interface. For more details, see our companion presentation M09-31 [5].

D. System Assembly

The cross-section view of the assembled system with a single module is shown in Fig. 5. The system can be mounted in front of the XII/FPD detector, C-arm system (Toshiba Medical Systems Corp.) for in-vivo clinic application as done for other detectors previously reported by our group [6].

III. Results

The EMCCD (IMPACTRON-CCD, Texas Instruments, Dallas, TX) has 1004 x 1002 active pixels in the image sensing area and each line of the output contains 28 optical black (OB) pixels for dark reference, 10 dummy (DM) pixels, 1004 active pixels and 4 tail OB pixels at the end of the line. The amount of the gain is adjustable from 1 to 2000. The charge multiplication level depends on the amplitude of the multiplication pulses (approximately 15V to 22V) applied to the charge multiplication gate (CMG). The analog output signals of the EMCCD with different gains are shown in Fig. 6.

As seen from the analog output signal, the active output signal amplitude increases with increasing CMG peak voltage.

The SSXII is designed to run at least at a frame rate of 15fps and 30fps with binning for a pixel rate of 17.5MHz. Images acquired at 15fps without binning are shown in Fig. 7.

From the acquired images in Fig. 7, we can see the brightness is changed significantly with the different CMG peak voltage. When we analyze the raw image data, we observed digital numbers of 100 to 330 with 17.5V CMG peak voltage and 1300 to 2300 after the CMG peak voltage was increased to 19.5V. In the image with increased gain (Fig. 7b), we can see greater than 8 lp/mm which means that the primary resolution limitation is still the 350 μm

thick CsI(Tl) phosphor since the Nyquist frequency resulting from the pixel size and FOT ratio is approximately 18 lp/mm.

Another analysis was made from the acquired digital numbers (DN) using fluoroscopic x-ray exposure and the results are shown in Table 1. The x-ray parameters were 70kV, 100mA, 10ms with the standard RQA5 beam filter and source image distance (SID) of 85cm. For each of the CMG peak voltages V_{CMG} , we took 150 frames of raw data, and calculated the average mean value $S(DN)$, signal standard variance σ_s^2 and dark frame standard variance σ_{Dark}^2 . From this, we calculated the sensitivity or camera gain constant $k(e-/DN)$, absolute gain and readout noise. The details of the k calculation and analysis are described in the companion presentation M19-170 [7].

The CMG peak voltage from 18.0V to 20.7V increased the mean signal from 36 to 1500, and reduced the equivalent readout noise from 110e- to 2.3e-. If we apply external cooling to EMCCD sensors, we can expect a further decrease of equivalent readout noise to less than 1e-.

IV. Conclusions

The modular SSXII design from component level is inherently scalable and hence enabling of flexible system FOV sizes and shapes. This modular design will be extended to a 3×3 or larger array to accomplish full clinical FOVs and enable the SSXII to replace conventional lower-resolution XIs or FPDs.

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Fig. 1. Schema of a 2×2 SSXII modular array showing its components which include, from the left to right, the CsI(Tl) plate, the FOTs and the EMCCDs on the head-boards.

Fig. 2.

Assembly of optically-black box with FOTs. EMCCD sensors are mounted on the back of the optical head box.

Fig. 3. Single module. 1) driver board, 2) EMCCD on head-board, 3) ADC, 4) FOT, 5) 350 μm thick CsI(Tl) phosphor, 6) on-board and 7) EMCCD heat-sink.

Fig. 4.
Electronic control and data acquisition part. 1) mother board, 2) power board, 3) Camera Link board, 4) extensible modular multiplexer board.

Fig. 5. SSXII detector. 1) optical head box, 2) EMCCDs mounted on the backplane, 3) plugged-in driver boards, 4) mother board and power board, 5) Camera Link interface board.

Fig. 6. Output analog signal of an EMCCD obtained with different CMG peak voltages shown in (a) to (c), all with a pixel clock frequency of 17.5MHz.

Fig. 7.
Acquired line pair pattern images with different CMG peak voltages; x-ray parameters:
70kV, 50mA, 12ms, SID = 85cm.

TABLE I

X-ray Measurement with RQA5 Attenuation Filter

V_{CMG} (V)	S (DN)	σ_s^2 (DN)	σ_{Dark}^2 (DN)	k (e-/DN)	Abs gain	σ_{Read}^2 (e-)
18.0	36.83	5.81	5.65	19.49	>1	110.06
19.0	75.18	8.80	5.91	1.76	7.49	10.42
19.5	132.43	13.45	6.47	0.95	13.87	6.16
20.0	283.34	28.70	9.27	0.38	34.41	3.56
20.5	907.59	91.87	23.13	0.11	115.07	2.66
20.6	1259.90	131.32	32.01	0.08	170.09	2.49
20.7	1522.19	162.58	37.35	0.06	217.31	2.28