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CMUT Fabrication Based On A Thick Buried Oxide Layer

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Abstract

We introduce a versatile fabrication process for direct wafer-bonded CMUTs. The objective is a flexible fabrication platform for single element transducers, 1D and 2D arrays, and reconfigurable arrays. The main process features are: A low number of litho masks (five for a fully populated 2D array); a simple fabrication sequence on standard MEMS tools without complicated wafer handling (carrier wafers); an improved device reliability; a wide design space in terms of operation frequency and geometric parameters (cell diameter, gap height, effective insulation layer thickness); and a continuous front face of the transducer (CMUT plate) that is connected to ground (shielding for good SNR and human safety in medical applications). All of this is achieved by connecting the hot electrodes individually through a thick buried oxide layer, i.e. from the handle layer of an SOI substrate to silicon electrodes located in each CMUT cell built in the device layer. Vertical insulation trenches are used to isolate these silicon electrodes from the rest of the substrate. Thus, the high electric field is only present where required – in the evacuated gap region of the device and not in the insulation layer of the post region. Array elements (1D and 2D) are simply defined by etching insulation trenches into the handle wafer of the SOI substrate.

I. Introduction

Various fabrication processes have been introduced for capacitive micromachined ultrasonic transducers (CMUTs) in the last 15 years. To this day, both sacrificial release layer technique [1] and high-temperature assisted direct wafer bonding method [2] are in use for CMUT fabrication. Only recently, the latter was shown [3] to be suitable for the fabrication of CMUTs in a 2D array configuration as well, while for sacrificial release-based CMUTs this has been demonstrated more than a decade ago [4].

The fabrication process described in this work is intended to expand the applicability of the direct wafer bonding method for CMUT fabrication in general. The main idea addresses the fabrication of all ultrasonic transducer configurations, which are single element transducers, 1D and 2D arrays. The goal is to demonstrate that the process has the potential to satisfy all relevant requirements in terms of simplicity, performance, and reliability. All in addition to the inherent advantages of direct wafer-bonded CMUTs compared to sacrificial release based devices, such as good uniformity, reproducibility, predictability, and design space flexibility.

II. Problem Statement and Main Idea

The wish list in terms of a versatile CMUT fabrication process, capable to fulfill the requirements for various applications (medical imaging and therapeutic applications, sensor applications, airborne ultrasound, just to name a few), is long. Apart from simplicity (low number of lithographic steps, no complicated wafer handling, only requiring standard

MEMS tools) even for 2D array fabrication and the well-known advantages of single-crystal silicon plates for CMUTs, the following requirements can be listed:

First, it should allow fabricating all basic transducer configurations, i.e. single element transducers, 1D, and 2D arrays (including reconfigurable arrays with electrical access to every single CMUT cell), and all array elements should be fully populated.

Second, direct wafer bonding requires clean and particle free surfaces. Thus, a CMUT process in which the bonding step takes place as early as possible is preferred. After the bonding step, the CMUT cells are protected in terms of particles and contaminations (hydrocarbons, alkali ions, etc.) of the insulation layer (charging effects).

Third, the process must feature a reliable cell structure (no electrical breakdown) with low intrinsic parasitic capacitance. Further, it should allow a completely independent choice of insulation layer thickness in the region of the gap and in the region of the support post for the plate [5].

Fourth and probably the most important requirement, in particular for medical applications (imaging and therapeutic, any intravascular ultrasound application) the front face of the transducer should not contain any openings and it must be connected to ground and not to the hot electrode (large DC bias voltage). The reasons for this are the requirement for good signal to noise ratio, requiring a good grounding and shielding concept, and, even more important, human safety. Further, a flat continuous transducer front face, even for 1D and 2D arrays, significantly simplifies any encapsulation (e.g. Polydimethylsiloxane, Sylgard, etc.) and packaging (probe fabrication) task.

Fifth, this process is ideal for implementing other CMUT operation mode ideas, such as recently proposed in [6] and [7]. For example, the idea of a CMUT with substrate-embedded springs for non-flexural plate movement [7], requires a well-defined length of the vertical spring elements. The thick-BOX process inherently provides an etch stop, and, thus, guarantees a constant spring element length over the entire wafer. In this example, only one via through the thick BOX layer per CMUT element would be required.

Before describing our process flow, which fulfills all these requirements, we will explain the background of the main idea.

A closer look at the CMUT cell structure of a sacrificial release based device [Fig. 1(a)], compared to the structure of a direct wafer-bonded CMUT with single crystal silicon plate [Fig. 1(b)], illustrates a significant difference. For the wafer-bonded device with vacuum-sealed cavities and electrically conductive silicon plate, the insulation layer thickness at the post region is the limiting factor in terms of reliability (electrical breakdown) and performance (parasitic capacitance). This is in particular the case for cell designs in which the gap height is supposed to be small. Note that for most sacrificial release devices, the plate material is electrically insulating, i.e. a metal electrode on top of the plate material is inevitable. Using electrically insulating materials, such as low-stress silicon nitride or nanocrystalline diamond films, for the CMUT plate is feasible in wafer-bonded CMUTs. However, this can become challenging in terms of bond strength quality (yield) and cell-to-cell and element-to-element uniformity of such films when used as CMUT plate material. Further, in many applications, such as therapeutic ultrasound (e.g. high intensity focused ultrasound), the conductive (electrically and thermally) silicon plate is advantageous because no metal electrodes, as indicated in [Fig. 1(b)], (except for ohmic contact points) are required. This is beneficial in terms of transducer heating, thermal stress effects, and magnetic resonance imaging tool compatibility.

In previous work [5], we introduced the idea of extending the insulation layer [Fig. 1(c)] into the substrate to address the aforementioned drawbacks (electrical breakdown and parasitic capacitance). However, the question of how to incorporate such an improved cell structure into a 2D array process was not addressed by this approach. The basic question [Fig. 1(d)] we are facing here is how to realize a cell structure in which the high electric field (for high coupling efficiency and good receive sensitivity) is only applied where really needed – the gap region of the CMUT cell.

One answer might be using an electrically insulating substrate, as suggested in [8]. This is indicated in Fig. 1(e). For example, fused silica on silicon wafers are commercially available for such endeavors, and advanced oxide etching of a BOX layer through a silicon via hole has been demonstrated [9].

Instead of using an electrically insulating substrate, we propose a silicon-on-insulation (SOI) wafer as a substrate [Fig. 1(f)]. Such substrates are widely available (e.g. Ultrasil Corporation, Hayward, CA) with buried oxide (BOX) layer thicknesses of up to several microns.

A zoomed-in version [Fig. 1(g)] illustrates the idea in more detail: In each evacuated cavity of the CMUT, vertical insulation trenches are used to form completely insulated silicon electrodes below the plate. According to the shown biasing scheme (dc and ac), the high electric field only occurs below each movable portion of the plate. At the post region, however, the thick BOX layer gives additional protection against electrical breakdowns and, further, reduces the parasitic capacitance. The hot electrode is fed through the thick BOX layer by using a doped polycrystalline silicon via or any other electrically conductive material, i.e. each cell has its own individual connection to the hot electrode.

Initially, we developed this idea for the fabrication of CMUTs for high temperatures, in which very thick insulation layers (reduced electrical breakdown voltages occur at elevated temperatures) are the key. Such a CMUT structure not only can be fabricated very easily, it also features the fabrication of 1D and 2D array configurations, which fulfill all aforementioned requirements for a versatile CMUT fabrication process.

III. Fabrication Process

The fabrication begins with an SOI substrate with thick BOX layer [Fig. 2(a)]. Device layer thickness, BOX layer thickness and handle layer thickness depend on the type of CMUT device (frequency, element configuration, airborne, immersion, etc.).

The first litho step is for defining the gaps in the device layer [Fig. 2(b)]. For devices that require small gap heights, local oxidation, preferably with thick oxide as diffusion barrier, can be used to achieve good gap height uniformity across the entire wafer. For larger gap heights (airborne devices), plasma etching can be used for this step.

Then, a second litho step is required for etching the vertical insulation trenches, down to the thick BOX layer [Fig. 2(c)]. The BOX layer acts as etch stop during this deep reactive ion etch (DRIE) step. This step results in electrically insulated silicon electrodes located in each cavity.

Then, the wafer is oxidized to create the insulation layer in the cavities [Fig. 2(d), oxide on backside is not shown]. The wafer is then high-temperature assisted direct bonded to a second SOI wafer, with the device layer thickness according to the designed plate thickness [Fig. 2(e)]. This is a huge advantage of this process, because no further contaminations are accumulated in the insulation layer oxide, in addition to the advantage that the bonding step

takes place early in the process. As soon as the annealing step for the direct wafer bonding is concluded, the cells are protected in terms of contamination and mechanical influences.

Now, the top SOI wafer acts as carrier wafer, which can be exploited to thin down the handle wafer of the substrate [Fig. 2(f)]. In particular for medical imaging arrays, a thinner substrate helps to avoid substrate ringing effects, and for smaller cell geometries it simplifies the tool requirements in terms of the second DRIE step to form the via holes (too high aspect ratio) on the backside of the substrate [Fig. 2(g)]. This DRIE step again benefits from the thick BOX layer acting as etch stop. Note that, as indicated in [Fig. 2(g)], the thick BOX layer must be opened in this step as well.

Doped polycrystalline silicon can be used in a low pressure chemical vapor deposition (LPCVD) step to finish the electrical via connection through the thick BOX layer [Fig. 2(h)]. At this stage the fabrication of a single element transducer can be finished by removing the handle and BOX layer of the top SOI wafer and dicing the wafer to singulate the devices from the substrate. In case 1D or 2D arrays are fabricated, an under-bump metallization (lift-off technique) [Fig. 2(i)] and one additional DRIE step to form element defining vertical trenches in the backside of the substrate wafer [Fig. 2(j)] are required, before removing the top handle wafer and BOX layer, and integration with integrated circuit, interposer solutions, or printed circuit board.

In particular for 2D arrays, one additional litho step for connecting the plate to ground using the top via, as shown in [Fig. 2(l)], can be used. Several elements, without gaps, at the perimeter of the 2D array ensure a complete electrical shield for good SNR and human safety.

IV. Results and Discussions

We started with fabricating CMUTs for airborne applications in single element configuration for proof-of-concept. The lower frequencies, required for airborne applications, only require larger cell geometries, and, thus, are easier to fabricate in terms of tool requirements, in particular for the DRIE steps. We successfully fabricated various types of CMUTs with cell radii ranging from 315 to 240 μm for frequencies ranging from ~300 to ~800 kHz, respectively. The plate thickness for these CMUTs is 10 μm , the gap height is 2 μm , the insulation layer thickness is 3 μm , and the thickness of the *thick* BOX layer is 5 μm . For some wafers we even used a 10- μm thick BOX layer, as it is the case for the exemplary SEM cross-section view of one cell of a CMUT shown in Fig. 3(a).

For larger via hole diameters, as used in the device from Fig. 3(a), liquid buffered oxide etchant (BOE) [12] or plasma oxide etching [9] can be used. Our experience, however, is that hydrofluoric acid (HF) vapor etching is the ideal method of opening the thick box layer. An example of such a via through a 5- μm thick BOX layer, etched with HF vapor, and then filled with conformal LPCVD doped polycrystalline silicon, is shown in Fig. 3(b). Interestingly, in case HF vapor etching is used, the BOX layer can not contain an oxide-to-oxide bonding interface, because the horizontal etch rate at such an interface is by far too high. For more details on this see [13].

Two exemplary measurement results, obtained from a device with a 5- μm thick BOX layer, demonstrate the strong acoustic response in the electrical impedance [Fig. 4(a)] and displacement at the center of a plate of a single cell [Fig. 4(b)]. At a dc bias voltage of 115 V (70% of pull-in voltage) and an ac excitation signal of 1 V_{pp}, the maximum center displacement of the plate is 550 nm peak-to-peak [Fig. 4(b)]. At this operation point electrical nonlinearities start to become visible [14].

The typical total capacitances (measured and calculated) for these devices are 400 pF and 280 pF for devices with 5 μm and 10 μm thick BOX layer, respectively. These numbers correspond to 48% and 63% reduction in total capacitance due to a lower parasitic capacitance. The assumption for this calculation are devices of equal cell geometry based on the conventional fabrication process [2], i.e. using the cell structure as shown in Fig. 1(b). Several of these devices were tested up to 1000 V dc bias voltage, repeatedly over a time period of six months, without a single occurrence of an electrical breakdown.

V. Conclusion

A versatile fabrication process for wafer-bonded CMUTs is presented. The process is simple and improves the reliability of wafer-bonded CMUTs in terms of electrical breakdown. The proof-of-concept of the main idea was demonstrated in this work by fabricating highly reliable single-element transducers, intended for airborne applications, such as ultrasonic gas flow metering at elevated temperatures. Furthermore, we expect this process to be ideal for fabricating large and reliable 1D and 2D arrays. Thus, at the moment we are fabricating large 2D arrays for medical applications, based on this thick BOX layer process.

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Fig. 1. Cross-section views of various existing CMUT cell structures (a–c), including the proposed cell structure (f, g). Blue, green, and purple indicate electrically conductive materials; red and yellow are electrically insulating materials.

Fig. 2.

Illustration of main fabrication steps. Only a small portion of the CMUT is shown, i.e. one quarter cell next to one half cell of a neighboring CMUT element. Depending on the target frequency, the transducer configuration (single element, 1D, 2D array), and the application, some of these steps are optional.

Fig. 3.

SEM of cross-section view (a) of one CMUT cell (polished sample) based on thick BOX fabrication process. We fabricated a larger device structure in single element configuration for proof-of-concept. In this example, four donut-shaped PolySi vias are used per cell (only one is visible at the cleaving plane). The second SEM (b) shows a circular-shaped PolySi via (polished sample) from a test wafer for the HF vapor etching and PolySi filling step.

Fig. 4.

Two preliminary measurement results (electrical impedance of a CMUT (a) and plate displacement of one single cell of the same device (b) as a function of dc bias voltage). The thick BOX layer for this device is 5 μm .