Complex three-dimensional high aspect ratio microfluidic network manufactured in combined PerMX dry-resist and SU-8 technology

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In this paper we present a new fabrication method that combines for the first time popular SU-8 technology and PerMX dry-photoresist lamination for the manufacturing of high aspect ratio three-dimensional multi-level microfluidic networks. The potential of this approach, which further benefits from wafer-level manufacturing and accurate alignment of fluidic levels, is demonstrated by a highly integrated three-level microfluidic chip. The hereby achieved network complexity, including 24 fluidic vias and 16 crossing points of three individual microchannels on less than 13 mm² chip area, is unique for SU-8 based fluidic networks. We further report on excellent process compatibility between SU-8 and PerMX dry-photoresist which results in high interlayer adhesion strength. The tight pressure sealing of a fluidic channel (0.5 MPa for 1 h) is demonstrated for 150 μm narrow SU-8/PerMX bonding interfaces. © 2011 American Institute of Physics. [doi:10.1063/1.3613668]

I. INTRODUCTION

Recent applications in the field of Lab-on-a-Chip led to the development of microfluidic systems with a high degree of functionality and three-dimensional (3D) multi-level fluidic networks.^{1–3} This trend towards dense and complex fluidic systems, which has been mentioned in a comprehensive review,⁴ requires a straightforward and versatile technology for the reliable fabrication of highly integrated microfluidic chips.

The most common approach for the manufacturing of integrated and complex fluidic systems nowadays is bonding. An open channel network is patterned on a substrate and then subsequently bonded onto a second substrate to form sealed cavities. This technique has been transferred to poly(dimethyl-siloxane) (PDMS),⁵ poly-methyl-methacrylate (PMMA),^{6,7} cyclic olefin copolymer (COC),⁸ and SU-8^{9–12} photoresist. Complex multilevel fluidic devices in SU-8¹² and PDMS^{13–16} have been achieved with the sequential stacking and bonding of multiple layers. These modular assembly techniques are rather time-consuming and difficult to control precisely. The proposed method for SU-8 microfluidic chips¹² includes sensitive fabrication steps for the manual release of thin wafer-size SU-8 layers from Kapton films. Multi-layer PDMS fluidic networks require delicate manual alignment and bonding steps. Activation of PDMS in an O₂ plasma, the following alignment and pressing of the PDMS slabs have to be carried out within a few minutes¹³ to achieve a strong and reliable bond. Consequently, time consuming alignment using conventional tools is replaced by manual alignment under a

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microscope.¹⁴ In very recent publications^{14,15} which report on PDMS multi-level microfluidics, this drawback remains unsolved. Fluidic networks are also realized in a sacrificial layer technique, where fluidic channels are the result of the selective removal of material from its surrounding medium.^{17–19} However, the complete removal of the sacrificial material from long channel networks is rather time-consuming, and the fluidic chip can be damaged due to the prolonged exposure to removal chemicals¹⁷ or to temperatures above 200 °C required for the diffusion of sacrificial material.^{18,19} A different approach for the fabrication of complex fluidic networks is the lamination of dry-photoresist,^{20–22} where a thin layer of soft baked resist is transferred onto a substrate to enclose fluidic networks. The lamination technique is fast and robust; however, thick resist layers are only available by multiple lamination, which has the disadvantage of decreased process yield. Each additional lamination step increases the probability of defects in the resist. In particular, the manual removal of the protective coversheet from the laminated dry-resist in order to add an additional layer may cause wrinkles or areas where the resist is locally peeled off from the substrate. High material costs and low flexibility regarding the adjustment of the resist thickness are further disadvantages.

We demonstrate a fabrication method that removes the mentioned constraints associated with bonding, sacrificial layer, and dry-resist lamination techniques. The described method is accurate compared to PDMS multi-layer bonding^{14,15} as multi-level fluidic chips with 25 μm alignment accuracy are fabricated. Our technique allows three fluidic levels compared to two fluidic levels using bonding techniques^{9,12} and further achieves high substrate adhesion strength of 29 MPa. Compared to the use of sacrificial layers,^{17–19} standard and straightforward UV-lithography procedures of SU-8 and PerMX photoresist are applied. As opposed to dry-resist lamination,^{20–22} in the presented technique it is possible to integrate thick SU-8 resist technology thus removing the need for multiple dry-resist lamination that decreases the process yield. These are clear improvements for the manufacturing of topologically complex 3D fluidic networks.

II. METHODS AND MATERIALS

A. Dry-resist processing

In this study, we have used 50 μm thick PerMX 3050 (DuPont) dry-photoresist, which is processable with standard UV-photolithography. The optically transparent negative dry film is based on photo-sensitive epoxy polymer that defines high-resolution permanent structures with vertical sidewalls. The dry-photoresist is laminated onto the substrate and does not require spin-coating and soft-baking compared to liquid photoresist. A dry-resist layer with precise thickness and high uniformity over the entire substrate is achieved by controlling the lamination parameters “roll pressure” and “roll gap.” The height profile of a laminated 4 in. wafer was measured at 32 equally distributed spots, and a mean resist thickness of 48.72 μm with a standard deviation of 0.45 μm was obtained.

Regarding microfluidic fabrication, dry-resist has the capability to bridge over gaps. Fluidic chips are sealed with the lamination of dry-resist onto the open fluidic channel network. Lamination onto a non-planar surface, e.g., due to elevated fluidic chips on the substrate is possible. Then, the resist is exposed to UV-light with i-line filter followed by post exposure bake at 95 °C for 5 min. In a last step, PerMX is developed in standard SU-8 developer PGMEA (propylene-glycol-methyl-ether-acetate) followed by an isopropanol rinse and a nitrogen stream dry. Figs. 1(a)–1(d) illustrate the complete lamination process.

Epoxy-photoresist is a suitable structural material for BioMEMS applications. The chemically²³ and thermally²⁴ stable as well as optically transparent material has been employed for the fabrication of devices used for drug delivery²⁵ and single cell manipulation²⁶ as well as for biosensor chips²⁷ and microarrays.^{28,29} The suitability for implantable medical devices has been reported by Kotzar³⁰ and demonstrated with microneedles for neural recording.³¹ Kalkandjiev²² reported on the biocompatibility of dry-resist on epoxy-basis.

For fluidic applications, homogeneous surface properties of the channel sidewalls are a major requirement for the precise handling and manipulation of fluids. With the combination of

FIG. 1. Lamination process to seal fluidic chips: (a) Dry-resist is hot-roll laminated onto the open fluidic networks on the substrate. (b) Laminated dry-resist is cut to the shape of the wafer. (c) Exposure to i-line UV-radiation (365 nm). PerMX is a negative photoresist-shadowed areas will be dissolved after development. (d) Post exposure bake and development to remove unexposed resist.

SU-8 and PerMX for the channel surface we are able to meet this requirement. Measurement of the contact angle (Krüss easy drop standard) with deionized water indicates for both resists an intrinsically weak hydrophilic character. The measured contact angle for PerMX is 75° and the contact angle for SU-8 is 80° . Available surface modification techniques are oxygen plasma exposure³² and chemical treatment.^{33–35}

B. Process compatibility of PerMX and SU-8

With the method presented here for the fabrication of multi-level fluidic networks, PerMX is combined for the first time with conventional SU-8 photoresist. As we use two different resist materials, process compatibility between them is a major prerequisite for this fabrication strategy to succeed. Processing steps and the corresponding parameters are similar for both epoxy-polymer based resists SU-8 and PerMX. In order to evaluate the process compatibility, we quantified the adhesive force present at the SU-8 and PerMX material boundary in a shear force experiment using a DAGE 4000 Bondtester. For this purpose, SU-8 2150 posts were fabricated on predefined PerMX plateaus [Fig. 2(a)]. As explained in Sec. III, post exposure baking temperatures are set to 55°C (15 h) for PerMX and 65°C (5 h) for SU-8, instead of the conventional 95°C to reduce thermal stress. Surface treatment prior to lamination and spin coating was not applied. Test configuration details are given in Fig. 2(a).

The chisel of the shear tester is positioned in front of the post. After a touchdown to the substrate, the chisel moves to the desired shear height h_s of $100\ \mu\text{m}$ above the substrate and pushes with increasing force against the post. The chisel width is 1 mm and the velocity of the chisel is $50\ \mu\text{m/s}$. The force required to shear off the post determines the substrate adhesion. Silicon is used as a reference substrate to compare for both measurements, namely: (1) adhesion between the PerMX and SU-8 boundary and (2) substrate adhesion of the test posts with and without a PerMX plateau. The experiments 1 and 2 are done on quartz glass and silicon substrates. The main result of this test is that for posts with a diameter of $500\ \mu\text{m}$ the failure occurs at the PerMX-substrate boundary as a result of the strong bond between SU-8 and PerMX. As it can be seen in Fig. 2(b), the plateau is entirely removed from the substrate where it was in contact with the SU-8 post. For $500\ \mu\text{m}$ posts, only this failure mechanism was observed. Thus, for large contact areas the bonding strength between SU-8 and PerMX is larger than the substrate adhesion of PerMX. This result is a proof of the excellent compatibility of both PerMX and SU-8 photoresists. For posts with diameters less than $500\ \mu\text{m}$, the bonding strength between SU-8 and PerMX is lower than the adhesion of PerMX on the substrate [Fig. 2(b)]. In this case, the failure occurred at the boundary between PerMX and SU-8.

FIG. 2. (a) Schematic test setup for the measurement of the failure force of SU-8 posts formed on top of PerMX plateaus. (b) SEM picture showing test posts on a PerMX plateau before (left) and after (right) the shear test. (c) Results of the shear test: Each adhesion value is obtained from 20 measurements. (d) Defect free fabrication of both large-scale and compact multi-layer fluidic chips is possible due to high inter-layer adhesion strength.

On silicon wafers, the test posts without a PerMX plateau showed a substrate adhesion of (11.4 ± 0.92) MPa. Hwang *et al.*³⁶ obtained a similar value of (11.7 ± 1.87) MPa. With the PerMX plateau, the computed substrate adhesion for the test posts on silicon substrates is (26.5 ± 1.64) MPa. On quartz glass substrates, the adhesion strength is (29.9 ± 2.16) MPa [Fig. 2(c)]. Thus, with the PerMX plateau the substrate adhesion of the test posts is increased by a factor of more than two, and high adhesion strength can be achieved.³⁷

The practical benefit of such a high interlayer adhesion is that fluidic chips can be reliably fabricated with a high degree of freedom regarding the fluidic design. For this study, we have manufactured both large scale fluidic chips ($25 \times 75 \text{ mm}^2$) and compact 3D multi-layer fluidic chips ($5 \times 7 \text{ mm}^2$) with small features [Fig. 2(d)] on quartz glass substrates without observing delamination.

C. Liquid sealing of the PerMX/SU-8 interface

The reliability and quality of the fluidic channels in terms of liquid sealing is tested in this section, and the results of a leakage test as well as a pressure resistance test are presented. For the leakage test, a fluidic channel as shown in Fig. 3(a) was flushed for 5 min with fluorescent sodium (0.3 g/l) with a flow rate of 10 ml/h. A fluorescent microscope image (Olympus BX51) of the channel showed no leakage of the fluorescence at the channel sidewalls indicating high PerMX/SU-8 interface sealing quality against the test medium. After the channel was flushed with distilled (DI) water for 5 min with the same flow rate, the SU-8 and PerMX bulk material showed no visible fluorescence. This result indicates no uptake from the fluorescence molecules by the PerMX and SU-8.³⁸

FIG. 3. (a) Schematic layout of the channel used for testing of the sealing strength against pressure loads. The minimum width of the bonding area for the PerMX cover is set to 150 μm . (b) Top view on the fluidic channel filled with blue dye before it was connected to a pressure of 0.5 MPa. (c) Top view of the fluidic channel after it was connected to a pressure of 0.5 MPa for 1 h. (d) SEM image of the cross section along the dashed line in (c).

The aim of the pressure test is to quantify the maximum pressure the PerMX/SU-8 fluidic chip can be operated without failure. For this purpose, the channel was filled with water, closed at the outlet, and the inlet was connected to a N_2 gas supply. The pressure of the N_2 gas was increased in 0.05 MPa steps starting from 0.0 MPa up to a maximum pressure of 0.5 MPa and finally held for 1 h. During the complete test, the fluidic chip was placed under water to visualize potential failure due to the applied pressure. After this test, the channel was filled with blue dye and inspected for defects along the channel using an optical microscope (Keyence VHX 100 k) [Fig. 3(c)]. For comparison, the same channel geometry was filled with blue dye before the test [Fig. 3(b)]. Neither defects such as delamination in the top view [Fig. 3(c)] nor mechanical deformation of the PerMX cover is visible in the SEM picture [Fig. 3(d)]. This result proves the excellent PerMX/SU-8 interface sealing quality against a pressure load of 0.5 MPa.

Robust and compact fluidic devices can be realized when PerMX is combined with SU-8 resist. The bonding area that is required to reliably seal an SU-8 fluidic channel with a layer of PerMX dry-resist does not significantly add additional area to the overall size of the fluidic chip and enables the fabrication of fluidic networks with closely spaced channels. The fluidic channel we used for the pressure test was sealed over a length of 1 mm with a minimum bonding width of only 150 μm , as highlighted in Figs. 3(a) and 3(b).

III. FABRICATION OF 3-LEVEL MICROFLUIDIC NETWORK

In terms of microfluidic design, the strategy of combining PerMX with SU-8 additionally offers the possibility to have SU-8 fluidic designs available for the fluidic chip. Besides the photolithography of PerMX and SU-8, we include high-precision UV-laser-machining in the process to gain a high level of flexibility regarding the topology of the fluidic network. On this basis, we demonstrate a microfluidic network with three individually addressable fluidic levels.

A. Processing of fluidic channel network

For the bottom microfluidic level, a 4 in. quartz glass wafer was structured using UV micro-laser-machining [Fig. 4(a)]. We use a Trumpf TruMark 6330 pulsed nanosecond laser that operates at 355 nm. The lateral geometry of the glass channels was defined in a CAD tool; the vertical dimensions were the result of the parameter set of the laser system (Table I). After lasering, the glass wafer was cleaned in acetone and isopropanol followed by a DI water rinse and dehydration at 120 $^{\circ}\text{C}$ (1 h). In Fig. 4(b), one layer of PerMX 3050 dry resist was laminated onto the glass wafer to enclose the glass channels using a DuPont laminator (Riston HRL). The lamination roll was heated up to 85 $^{\circ}\text{C}$, the lamination speed was set to 1 cm/s, and the applied roll pressure was approximately 0.1 MPa. The dry resist is then exposed to 1125 mJ/cm^2 (i-line). For all photolithography steps, the exposure dose from the data sheets was increased by a factor of 2.25 to take into account the absorption of transparency masks as well as the use of quartz glass substrates. The post exposure bake was

FIG. 4. Process flow for the shown 3D fluidic network: (a) UV-laser machining of substrate embedded glass channels to define the bottom fluidic level. (b) Lamination and UV-lithography of PerMX to seal glass channels. (c) Spin coating and UV-lithography of thick SU-8 layer to define the geometry of the center fluidic level. (c*)-(c**) To open a fluidic via, PerMX is locally removed using UV-laser machining. (d) Lamination onto SU-8 and UV-lithography of PerMX to seal center fluidic level. (e) Lamination of PerMX to define the geometry of the top fluidic level. (f) Lamination and UV-photolithography of PerMX to seal the top fluidic level.

subsequently carried out at 55 °C for 15 h. The low temperature for the PerMX post exposure bake reduces deformations of the dry-resist due to the expanding air volume inside the enclosed channels. The top polyester coversheet of the dry-resist was removed after the post exposure bake. This first PerMX layer was not developed. For the center fluidic level, SU-8 2150 photoresist was spin coated on the wafer at 500 rpm (10 s) and 2000 rpm (30 s) to define a layer of 300 μm thickness. The soft bake was carried out at 65 °C (15 min) and 95 °C (1 h) on a hotplate. We have noticed that this long soft bake has no negative effect on the PerMX layer underneath the SU-8 resist. The applied exposure dose for the SU-8 layer was set to 1125 mJ/cm² (i-line). The post exposure bake was carried out at a reduced temperature of 65 °C to minimize thermally induced stress [Fig. 4(c)]. To compensate for the lower temperature, the time of the post exposure bake was extended to 5 h. Both the SU-8 and the first PerMX layer were then developed simultaneously in PGMEA developer (15 min). The top level for fluid handling was realized by the lamination of three PerMX layers [Figs. 4(d)–4(f)] using the same parameters and steps as in Fig. 4(b). Throughout the whole process, no surface treatment was applied prior to adding the next layer of SU-8 or PerMX.

B. Processing of fluidic vias

Initially, each fluidic level is isolated from the others. Fluidic interconnections (vias) are defined at positions where the PerMX separating two levels is locally removed. Between the center and top fluidic level, vias can be realized with photolithography [Figs. 4(d)–4(f)]. In contrast, the bottom and center fluidic levels cannot be connected with photolithographically removed dry-resist. Since the first PerMX layer functions as a substrate for the subsequent SU-8 processing step, it must provide a closed and planar surface. The straightforward idea of using photolithography for making the vias in the PerMX does not work because of the SU-8 soft bake at 95 °C. Uncured PerMX melts at approximately 60 °C and the viscous SU-8 would flow into the cavity once the via is melt open. Soft baking of the SU-8 below 60 °C does not sufficiently remove the solvents from the resist. As a consequence, the first PerMX layer has to be flood exposed and cured as explained in Fig. 4(b).

Vias between the bottom and center fluidic levels are thus achieved with the local removal of PerMX induced by a focused UV-laser beam [Figs. 4(c*) and 4(c**)]. The laser parameters applied for the removal of the PerMX membrane (Table I) are optimized for low interaction between the laser light and the surrounding resist material. The total thermal energy required for the sublimation of the PerMX membrane is applied in multiple repetitions of low power laser pulses. With the reduction of the thermal power input, the 50 μm thick PerMX membrane is removed entirely without cracking or burning of the fluidic via (Fig. 5).

TABLE I. Processing parameters of fluidic levels and vias.

Fluidic geometry	Processing type	Material	Parameters	
Bottom level	UV-laser	Quartz glass	Power	2 W (100%)
			Focus speed	100 mm/s
			Frequency	20 kHz
			Pulse width	20 ns
			Number of repetitions	1
Center level	Lithography	SU-8 2150	Spin coating	500 rpm (10 s), 2000 rpm (30 s)
			Soft bake	65 °C (15 min), 95 °C (1 h)
			Exposure (i-line)	1125 mJ/cm ²
			Post exposure bake	65 °C (3 h)
			Development	PGMEA (15 min)
Top level	Lithography	PerMX 3050	Lamination	85 °C, 0.1 MPa, 1 cm/s
			Exposure (i-line)	1125 mJ/cm ²
			Post exposure bake	55 °C (15 h)
			Development	PGMEA (5 min)
Via	UV-laser		Power	0.4 W (20%)
			Focus speed	50 mm/s
			Frequency	2 kHz
			Pulse width	20 ns
			Number of repetitions	30

In order to achieve complex fluidic networks at the microscale, the alignment of the individual fluidic levels needs to be controlled thoroughly. In established PDMS multi-layer processes patterned fluidic levels are manually stacked and interconnected. The resulting low alignment accuracy is the limiting factor for the miniaturization of the fluidic system. For example, the dimensions of fluidic through-holes (vias) need to be designed larger to compensate for the

FIG. 5. SEM picture of a fluidic via from the bottom fluidic level to the top fluidic level. The PerMX membrane which blocked the via before the UV-lasering step is entirely removed. The smooth and clean surface of the via shows that the thermal input from the UV-laser beam is not critical and can be applied for the removal of the PerMX membrane. Reprinted with permission from R. Ch. Meier, V. Badilita, U. Wallrabe, and J. G. Korvink, in *Proceedings of the International Conference on Miniaturized Systems for Chemistry and Life Sciences, Groningen, The Netherlands, 3–7 October 2010*, pp. 1145–1147. Copyright 2010 CBMS.

FIG. 6. (a) The complete UV-laser setup showing the alignment system with the camera (μ Eye UI-1645LE) and the $xy\phi$ -stage (Micos PRS-110, LS-110). (b) Schematic drawing of the test chip to characterize the lasering of fluidic vias in terms of positioning accuracy. The laser spot targets at the center of three circular regions with decreasing diameter. (c) Top view of the test chip. The focus of the UV-laser and the resulting ablation of the silicon substrate induced by the UV-laser pulse were positioned with an accuracy of $25\ \mu\text{m}$ with respect to the center of the circular areas marked with a grey cross.

alignment tolerance.¹⁵ However, for the miniaturization of the complete fluidic network, both fluidic vias as well as the fluidic channel network should be of equal dimensions.

With the technique described by us, manual interventions are avoided, and vias $150\ \mu\text{m}$ in diameter are created with $25\ \mu\text{m}$ positioning precision as demonstrated in Fig. 5. This accuracy is achieved with a custom system [Fig. 6(a)] that aligns the substrate to be lasered with respect to the laser coordinate system. After alignment of the wafer, the lasering of the vias is a serial process where the $xy\phi$ -stage drives chip by chip in the focus of the UV-laser. The center of each fluidic chip is positioned in the focus, and a series of laser pulses create the vias at the corresponding coordinates.

The deviation of $25\ \mu\text{m}$ was quantified with a test chip which has three circular holes with decreasing diameters [Figs. 6(b) and 6(c)]. The holes with $100\ \mu\text{m}$, $75\ \mu\text{m}$, and $50\ \mu\text{m}$ in diameter served as a reference structure to determine the deviation of the UV-laser focus from the correct position in the center of the holes. The actual position of the UV-laser focus is indicated by the ablated silicon substrate. As shown in Fig. 6(c), we are able to position the focus of the laser inside a circular area of $50\ \mu\text{m}$ in diameter which corresponds to a tolerance of $25\ \mu\text{m}$. The accuracy is limited by the precision of the mechanical assembly of the alignment system.

C. Demonstration of 3D channel network

To demonstrate the capability of the reported technique for the realization of topologically complex fluidic networks, we chose a 3D helical channel configuration. For this, two individual channels are arranged on a fluidic chip such that one channel forms the shape of a spiral and continuously winds around a second channel. This fluidic geometry, where two channels remain completely separated while crossing each other, has been demonstrated in a different technique for SU-8 microfluidics.⁹ However, in our process it is feasible to go one step beyond in terms of topological complexity. Here, it is generally possible to have a stack of three separate channels all passing each other at the same lateral position. With respect to the proposed helix geometry, in our fabrication method the complexity can be increased to a fluidic double helix. Two separate channels wind around a planar and straight channel such that it is passed over and under at the same xy -position. This topology in SU-8 based microfluidics is realized with three individually addressable fluidic channels that cross each other at 16 places in an area of $4.8\ \text{mm} \times 2.7\ \text{mm}$ [Figs. 7(a)–7(c)].

FIG. 7. Demonstration of the 3D multi-layer fluidic chip: (a) Picture of the full chip (scale bar: 2.5 mm). (b) The whole 3D fluidic network with 24 vias and 16 crossing points (scale bar: 1 mm). (c) The fluidic double helix geometry in a close-up view. The center channel (blue) is passed over and under alternately at the same lateral position by the green and red channel (scale bar: 200 μm). (d) SEM cross section picture along A-A' showing the channel profiles.

Zhang presented the fabrication of a similar geometry in PDMS¹⁴ which required time-consuming bonding steps for each fluidic device. The method developed by us provides wafer-level manufacturing of compact 3D multi-level fluidic devices with fluidic vias and channel crossings. The strategy of combining SU-8 and PerMX further offers exceptional flexibility for the dimensioning of the fluidic chip. The excellent adhesion of the fluidic chip on the glass substrate allows for expanded chip sizes without an increased risk of delamination failure. For each fluidic layer the channel geometry, including the height, can be adjusted separately over a wide range to meet specific design requirements resulting from different application demands. In particular, the SU-8 and the glass channels allow for a considerable freedom in terms of fluidic design as they can cover channel heights over a wide range.

Further advantages arise from the properties of the materials used in this process. With one of the fluidic layers manufactured in SU-8, one can benefit from high aspect-ratio UV-lithography. PerMX dry-resist is of interest for microfluidic applications where highly constant and accurately defined layer thicknesses are essential. Quartz glass, PerMX, and SU-8 are transparent for visible light; thus, the fluidic chip is suitable for applications where optical access is required. Bio-compatibility³⁰ and high chemical²³ and thermal²⁴ stability are further demands from many microfluidic applications that are met.

The presented technique utilizes automatic and precise UV-lasering and standard UV-lithography procedures on wafer-level which simplifies process integration of available fluid handling techniques.³⁹ Compared to bonding methods^{13–15} that achieve the same network complexity, this approach has high alignment accuracy between the fluidic channels on different levels. Sacrificial layer techniques require complicated UV-lithography methods¹⁷ or high-temperature steps^{18,19} that increase the process complexity compared to our strategy.

IV. CONCLUSION

We developed and characterized a new fabrication method to implement 3D multi-level high aspect ratio microfluidic networks. Based on the combined use of straightforward and reliable dry-photoresist lamination and high-resolution SU-8 UV-photolithography, the demonstrated approach for the manufacturing of microfluidic networks facilitates an increase in design flexibility and achievable topological complexity. Both types of permanent photoresists used in this study are suitable for microfluidic applications and further show excellent process compatibility and high interlayer adhesion leading to a high degree of freedom regarding microfluidic design and applications. Those facts will ultimately lead to the ability to manufacture complex and robust 3D fluidic circuits removing many of the constraints currently associated with the 2D manufacturing process for SU-8 photoresist.

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- ¹A. W. Martinez, S. T. Phillips, and G. Whitesides, *Proc. Natl. Acad. Sci. USA* **105**, 19606 (2008).
- ²H. Tani, K. Maehana, and T. Kamidate, *Anal. Chem.* **76**, 6693 (2004).
- ³D. Theriault, S. R. White, and J. A. Lewis, *Nat. Mater.* **2**, 265 (2003).
- ⁴P. S. Dittich and A. Manz, *Nat. Rev. Drug Discov.* **5**, 210 (2006).
- ⁵M. A. Unger, H.-P. Chou, T. Thorsen, A. Scherer, and S. R. Quake, *Science* **288**, 113 (2000).
- ⁶Y. Sun, Y. C. Kwok, and N.-T. Nguyen, *J. Micromech. Microeng.* **16**, 1681 (2006).
- ⁷B. Bilenberg, T. Nielsen, B. Clausen, and A. Kristensen, *J. Micromech. Microeng.* **14**, 814 (2004).
- ⁸C. W. Tsao, L. Hromada, J. Liu, P. Kumar, and D. L. DeVoe, *Lab Chip* **7**, 499 (2007).
- ⁹F. J. Blanco, M. Agirregabiria, J. Garcia, J. Berganzo, M. Tijero, M. T. Arroyo, J. M. Ruano, I. Aramburu, and K. Mayora, *J. Micromech. Microeng.* **14**, 1047 (2004).
- ¹⁰P. Svasek, E. Svasek, B. Lendl, and M. Vellekoop, *Sens. Actuators A* **115**, 591 (2004).
- ¹¹S. Tuomikoski and S. Franssila, *Sens. Actuators A* **120**, 408 (2005).
- ¹²M. Agirregabiria, F. J. Blanco, J. Berganzo, M. T. Arroyo, A. Fullaondo, K. Mayora, and J. M. Ruano-López, *Lab Chip* **5**, 545 (2005).
- ¹³J. R. Anderson, D. T. Chiu, R. J. Jackman, O. Cherniavskaya, J. C. McDonald, H. Wu, S. H. Whitesides, and G. M. Whitesides, *Anal. Chem.* **72**, 3158 (2000).
- ¹⁴M. Zhang, J. Wu, L. Wang, K. Xiao, and W. Wen, *Lab Chip* **10**, 1199 (2010).
- ¹⁵B. Mosadegh, M. Agarwal, Y.-S. Torisawa, and S. Takayama, *Lab Chip* **10**, 1983 (2010).
- ¹⁶Y. Zheng, W. Dai, D. Ryan, and H. Wu, *Biomicrofluidics* **4**, 036504 (2010).
- ¹⁷K.-S. Yun and E. Yoon, *Lab Chip* **8**, 245 (2008).
- ¹⁸H. A. Reed, C. E. White, V. Rao, S. A. B. Allen, C. L. Henderson, and P. A. Kohl, *J. Micromech. Microeng.* **11**, 733 (2001).
- ¹⁹S. Metz, S. Jiguet, A. Bertsch, and Ph. Renaud, *Lab Chip* **4**, 114 (2004).
- ²⁰P. Abgrall, Ch. Lattes, V. Conédéra, X. Dollat, S. Colin, and A. M. Gué, *J. Micromech. Microeng.* **16**, 113 (2006).
- ²¹U. Stöhr, P. Vulto, P. Hoppe, G. Urban, and H. Reinecke, *J. Micro/Nanolith. MEMS MOEMS* **7**, 033009 (2008).
- ²²K. Kalkandjiev, L. Riegger, D. Kosse, M. Welsche, L. Gutzweiler, R. Zengerle, and P. Koltay, *J. Micromech. Microeng.* **21**, 025008 (2011).
- ²³H. Lorenz, M. Despont, N. Fahrni, N. Labianca, P. Renaud, and P. Vettiger, *J. Micromech. Microeng.* **7**, 121 (1997).
- ²⁴K. Y. Lee, N. LaBianca, and S. A. Rishton, *J. Vac. Sci. Technol. B* **13**, 3012 (1995).
- ²⁵G. Voskerician, M. S. Shive, R. S. Shawgo, H. v. Recum, J. M. Anderson, M. J. Cima, and R. Langer, *Biomaterials* **24**, 1959 (2003).
- ²⁶N. Chronis and L. P. Lee, *J. Microelectromech. Syst.* **14**, 857 (2005).
- ²⁷M. G. Jenke, C. Schreiter, G. M. Kim, H. Vogel, and J. Brugger, *Microfluid. Nanofluid.* **3**, 189 (2007).
- ²⁸M. Stangegaard, Z. Wang, J. P. Kutter, M. Dufva, and A. Wolff, *Mol. Biosyst.* **2**, 421 (2006).
- ²⁹R. Marie, S. Schmid, A. Johansson, L. Ejlsing, M. Nordström, D. Häflinger, C. B. V. Christensen, A. Boisen, and M. Dufva, *Biosens. Bioelectron.* **21**, 1327 (2006).
- ³⁰G. Kotzar, M. Freas, P. Abel, A. Fleischman, S. Roy, C. Zorman, J. M. Moran, and J. Melzak, *Biomaterials* **23**, 2737 (2002).
- ³¹A. Altuna, G. Gabriel, L. M. de la Prida, M. Tijero, A. Guimerá, J. Berganzo, R. Salido, R. Villa, and L. J. Fernández, *J. Micromech. Microeng.* **20**, 064014 (2010).
- ³²F. Walther, P. Davydovskaya, S. Zürcher, M. Kaiser, H. Herberg, A. M. Gigler, and R. W. Stark, *J. Micromech. Microeng.* **17**, 524 (2007).
- ³³M. Nordström, R. Marie, M. Calleja, and A. Boisen, *J. Micromech. Microeng.* **14**, 1614 (2004).
- ³⁴S. L. Tao, K. C. Popat, J. J. Norman, and T. A. Desai, *Langmuir* **24**, 2631 (2008).
- ³⁵A. Deepu, V. V. Sai, and S. Mukherji, *J. Mater. Sci. Mater. Med.* **20**, 25 (2009).
- ³⁶K.-Y. Hwang, C.-S. Park, J.-H. Kim, K.-Y. Suh, E.-C. Cho, and N. Hih, *J. Micromech. Microeng.* **20**, 117001 (2010).
- ³⁷H. Kim and K. Najafi, *J. Microelectromech. Syst.* **14**, 1347 (2005).
- ³⁸M. W. Toepke and D. J. Beebe, *Lab Chip* **6**, 1484 (2006).
- ³⁹M. Sadeghi, H. Kim, and K. Najafi, in *Proceedings of the IEEE Conference on Micro-Electro-Mechanical Systems*, Hong Kong S.A.R., China, 24–28 January 2010, p. 15–18.