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Development of a 64 channel ultrasonic high frequency linear array imaging system

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Abstract

In order to improve the lateral resolution and extend the field of view of a previously reported 48 element 30 MHz ultrasound linear array and 16-channel digital imaging system, the development of a 256 element 30 MHz linear array and an ultrasound imaging system with increased channel count has been undertaken. This paper reports the design and testing of a 64 channel digital imaging system which consists of an analog front-end pulser/receiver, 64 channels of Time-Gain Compensation (TGC), 64 channels of high-speed digitizer as well as a beamformer. A Personal Computer (PC) is used as the user interface to display real-time images. This system is designed as a platform for the purpose of testing the performance of high frequency linear arrays that have been developed in house. Therefore conventional approaches were taken in its implementation. Flexibility and ease of use are of primary concern whereas consideration of cost-effectiveness and novelty in design are only secondary. Even so, there are many issues at higher frequencies but do not exist at lower frequencies need to be solved. The system provides 64 channels of excitation pulsers while receiving simultaneously at a 20 MHz–120 MHz sampling rate to 12-bits. The digitized data from all channels are first fed through Field Programmable Gate Arrays (FPGAs), and then stored in memories. These raw data are accessed by the beamforming processor to rebuild the image or to be downloaded to the PC for further processing. The beamformer that applies delays to the echoes of each channel is implemented with the strategy that combines coarse (8.3ns) and fine delays (2 ns). The coarse delays are integer multiples of the sampling clock rate and are achieved by controlling the write enable pin of the First-In-First-Out (FIFO) memory to obtain valid beamforming data. The fine delays are accomplished with interpolation filters. This system is capable of achieving a maximum frame rate of 50 frames per second. Wire phantom images acquired with this system show a spatial resolution of 146 μm (lateral) and 54 μm (axial). Images with excised rabbit and pig eyeball as well as mouse embryo were also acquired to demonstrate its imaging capability.

Keywords

High frequency ultrasound; beamformer; FPGA; Linear array

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I. Introduction

High frequency ultrasonic imaging has found many applications in clinical and preclinical imaging [1–4]. Several high frequency (>20 MHz) ultrasound linear array transducers [1–3] have been designed and fabricated. A prototype imaging system [4] has also been developed as a platform for testing high frequency linear array transducers developed in house. However, because of the limited number of beamforming channels (16 channels) of the earlier system [4], the lateral resolution needs to be improved to achieve an acceptable level [4]. Furthermore, in order to extend the field of image view obtainable with a 64-element 30 MHz ultrasound linear array and achieve a lateral resolution along the azimuthal direction comparable to that with a single element transducer of $f\# = 2$ at 30 MHz, the design and development of an ultrasound imaging system for a 256-element linear array transducer with increased channel count has been undertaken. The progress that has been made is reported in this paper.

Ultrasonic linear arrays allow for dynamic focusing in transmit and receive to improve the lateral resolution throughout the field of view. Progress in the development of high frequency linear arrays has been made in the past few years [1–5]. Preliminary B-mode imaging with a rate of 400 frames per second was achieved with a high frequency analog imaging [6]. Recently linear array based HF digital ultrasound systems have become commercially available (Vevo 2100, Visualsonics Inc., Toronto, Canada) as described in [3]. The system reported in this paper is designed for flexibility and ease of use primarily for the purpose of testing high frequency linear arrays. Cost-effectiveness and novelty are of a lesser concern. Although the approaches taken are similar in many ways to those in low frequency systems, there are many practical issues that occur in high frequency design. These problems which need to be considered and resolved are described in this paper. This system may also be useful for studying new imaging methods and algorithms because pre-beamformer data from each channel are available for storage and can be downloaded for offline processing.

This digital ultrasonic imaging system was completely developed in a laboratory environment. It was designed to 1) be used with a 256 elements 1D linear array transducers; 2) have 64-channel beamformer on both transmit and reception; 3) have a signal bandwidth from 10 MHz to 50 MHz; 4) have the capability of acquiring pre-beamformer data. The block diagram of the overall imaging system is shown in Fig. 1. The system is composed of 256 channels of analog front-end pulser/receiver, 64 channels of Time-Gain Compensation (TGC), 64 channels of high-speed digitizer as well as a beamformer. A PC is used as user interface to display real time images. This system is designed to handle up to 256 elements and to provide 64 channels of excitation pulsers while receiving simultaneously at a 120 MHz sampling rate with 12-bit resolution. The digitized data from all channels are first fed to FPGAs, and then stored in memories. Those raw data are accessed by the beamforming processor to re-build the image or to be downloaded to the PC for further processing. The beamformer that applies delays to the echoes of each channel is implemented with the strategy that combines coarse and fine delays. The coarse delays are integer multiples of the sampling clock rate. The fine delays are accomplished with interpolation. The characteristics of the 64-channel beamformer are shown in Table 1.

Section II describes design considerations for this prototype system. Section III introduces the system hardware details. Section IV summarizes results from system performance evaluation. Section V gives the discussion and conclusion.

II. SYSTEM DESIGN CONSIDERATIONS

One of the limitations of the previously developed linear arrays and digital imaging system is the narrow image width (3mm) because of the small number of array elements (48) [1,4], which is not wide enough to cover such biological targets as a rabbit eye. Therefore, a new linear array with 256 elements providing 9.6mm field of view in lateral direction was developed. A 64-channel beamformer has been designed and developed accordingly to accommodate this larger array. Array transducer parameters used for this system for design consideration are shown in Table 2.

The beam patterns on the azimuthal plane were simulated to illustrate the importance of a large aperture size on the lateral resolution by modifying the activated number of array elements using Field II [7]. The -6 dB contours of the simulated beam patterns on the azimuthal plane and the corresponding -6 dB 1-D intensity profiles at the focal points using different number of active elements for the 30 MHz linear array are plotted in Fig. 2. It is readily apparent that activating more elements, thus yielding a larger aperture size, would result in a better lateral resolution. When the number of activated elements is less than 8, there is a rapid divergence of the -6 dB contour. If 16 elements are used to generate a beam at a focal distance of 6.4mm, the array transducer has a lateral resolution of 400 μm while with 64-elements the lateral resolution is 100 μm , which is comparable to the lateral resolution along the azimuthal direction in the focal plane of a single element transducer with an $f\#$ of 2 at 30 MHz

Delay values for the 64-element beamformer on receive are calculated from the equation:

$$\tau(a_i, d_j) = \frac{\sqrt{d_j^2 + a_i^2} - d_j}{c} \quad (1)$$

where d_j is the distance of pixel j along the axis to the array surface, a_i is the distance from i^{th} element to the center of the aperture, c is the sound velocity, and $\tau(a_i, d_j)$ is the delay for i^{th} element at the depth d_j . The maximum delay value for a 64-element aperture is:

$$\tau_{\max} < \frac{a_i}{c} | i=32 \quad (2)$$

Because the pitch of the arrays (distance between two adjacent elements) is 50 μm , $\tau_{\max}$ is 1.067 μs . In the beamformer design, the dynamic focusing on receive is implemented by dynamic updating the read address of random access memory (RAMs). Delay values need to be converted to the address offset. Therefore, the maximum offset in an address, $\text{Addr_offset}_{\max} < \tau_{\max} \times fs$, where fs is the sampling frequency. In this design, the sampling frequency is set to 120 MHz; the maximum offset thus is 128. Based on this value, 8 bits are used to represent the integer of delay values in FPGA. Two more bits are used to represent the fractional/finer delays. Therefore, a 10 bit look-up table is used to store the delay values so that a 16x center frequency accuracy in both transmit and receive beamformer can be achieved.

III. SYSTEM HARDWARE

After the timing controller receives the start trigger signal from the PC, the transmit beamformer in FPGAs in the analog boards generates 64 independent pulser-trigger signals. They are sent to the high-voltage pulsers and multiplexer control signals which can select 64 elements out of 256 elements at one time. In reception, these same multiplexer control

signals are used to receive the echoes from the group of 64 elements. Time-gain compensation (TGC) controls are used in the receiving chain. These amplified and filtered signals are subsequently fed to Analog-to-Digital Converters (ADCs). Here the FPGAs are used to receive the digitized data and the beamformer is implemented in these FPGAs. The beamformed data are transferred to PC for display. The whole system may be divided into a transmit beamformer, a receive beamformer and a backplane/timing control subsystem.

A. Transmission Beamformer Design

The analog front-end circuit consists of 8 boards and each board has 32 channels of transceiver, amplification and transmission focusing circuit (Fig. 3). On each board, the transceiver circuits are triggered by signals from a FPGA. The trigger signals then pass through 1-of-4 demultiplexers (74AC139, National Semiconductor Inc.) so that 8 adjacent elements are chosen from each board. Therefore, a total 64 adjacent elements are selected to transmit pulsers. The pulser circuit generates a pulse train with a peak to peak voltage as high as ± 100 volt at 30 MHz for each chosen element. Immediately following the T/R switch, Low Noise Amplifiers (LNAs) and Variable Gain Amplifiers (VGAs) (AD8334, Analog Devices Inc.) are used to provide 10 and 48 dB gain respectively along the signal path. Followed by the VGAs, 4-to-1 multiplexers (AD8184, Analog Devices Inc.) are used to select the corresponding activated elements out of 256 elements. The demultiplexers and multiplexers are programmed by the same control signals to maintain synchronization. After multiplexers, Time Gain Compensation (TGC) amplifiers provide another 10 to 30 dB gain to the echoes. AC coupled passive band-pass LC filters with a -3 dB cutoff frequency from 20 MHz to 50 MHz are used directly after TGC amplifiers before the signals are fed into the ADCs. The transmission focusing is implemented by delaying trigger signals used for generating pulsers, with a minimum delay increment of $1/16$ of the transducer center frequency between triggers (Fig. 4). A FPGA (XC3S250E, Xilinx Inc.) is used on each board. Transmission delay values are stored in the internal synchronous dynamic random access memory (SDRAM) in FPGAs and read out on the rising edge of the line trigger. The delay values are then fed to the transmit-delay generator. The time interval between trigger signals is achieved with the delay values from memory. FPGAs also send out control signals to transmission demultiplexers and reception multiplexers.

B. Digital Beamformer Design

The digital beamformer is designed with two boards (32 channels per board) that contain a total of 64 channels. Each channel is digitized by an ADC (AD9627, Analog Devices Inc.) which has dual channels and a wide working bandwidth from 20 MHz to 150 MHz.

A combination of coarse and fine delay strategy is adopted in this design to implement digital beamforming. The coarse delay, which is an integer multiple of the clock period (8.3ns), is accomplished by dynamically updating reading address signal of the RAMs so that the required data are picked up (Fig. 5). The fine delays are accomplished with interpolation by a factor of 4 to achieve the $1/16$ delay accuracy. The FPGAs (XC5V110, Xilinx, Inc) in each beamformer board have distributed RAMs which can be configured into 2K by 16 bit RAM memories. Twenty-two FIFOs memory inside FPGAs are configured and used in one board. Those RAMs are working at a maximum frequency of 400 MHz. The read addresses for RAM are dynamically calculated from the lookup table with delay values in memory, using the coarse delay values. The interpolations by 4 are implemented using Cascaded Integrator-Comb (CIC) filters, an optimized class of finite impulse response filter. A CIC filter consists of one or more integrator and comb filter pairs. In the case of an interpolating CIC, the input signal is fed through an up-sampler, then to one or more cascaded integrators, followed by one or more comb sections. The output data from RAMs are interpolated by a factor of 4. The fine delay values are then fed to the 4:1 multiplexers,

where these fine delay values determine which output of the multiplexer is used for the summation.

C. Backplane and Timing Control Circuit Design

The backplane circuit has 10 board-to-board connectors (VHDM, Molex Inc.) to host daughter boards (8 analog boards and 2 digitizer boards), a transducer connector, a power supply connector and digital acquisition board (NI PCIe-6537, National Instrument Inc.). The data acquisition board running at 50 MHz maximum clock rate and 200 MB/s maximum throughput is based on a PCI Express data transfer protocol. The PC is equipped with 2 GB, 667 MHz DDR2 (Double Date Rate) memory that can be configured as data buffer. The read/write control of each image frame is synchronized through a PCIE bus. A FPGA (XC3S120, Xilinx, Inc) is used as a timing controller, in which the imaging modes are encoded and send to each board. In conventional B-mode imaging, the transmit beamformer, receive beamformer, apodization in reception, aperture growth and excitation cycle numbers are also controllable and programmable in this FPGA. The 16-bit address bus and 8-bit control signals are from this FPGA and shared by all boards.

IV. SYSTEM EVALUATION

A. Wire Phantom

The performance of the digital imaging system interfaced to a recently built transducers was evaluated with a wire phantom consisting of 20 μm diameter tungsten wires (California Fine Wire Co., CA) and arranged diagonally with lateral distance of 1 mm (20 X wavelength) and axial distance of 0.55 mm (11 X wavelength). Cross-sectional images were obtained to assess the lateral and axial beam profiles plotted in Fig. 6. The measured and simulated lateral resolutions were 146 μm and 130 μm respectively. The measured and simulated axial resolutions were 54 μm and 47 μm respectively.

B. Tissue Mimicking Phantom

The contrast resolution was evaluated using a tissue phantom designed specifically for the characterization of high frequency imaging devices (>20 MHz). The phantom has attenuation and scattering properties similar to those of human soft tissues [8]. The phantom contains 0.1–1.09 mm anechoic spherical voids. The images in Fig. 7 were obtained from anechoic spheres of diameters from 1.09mm (A), 0.825mm (B), 0.53mm (C), and 0.3mm (D). The 300 μm diameter anechoic spheres [Fig. 7(D)] were the smallest void that could be resolved by this scanner. The contrast resolution was measured by the clutter energy to the total energy ratio (CTR), which is the ratio of the average energy level of the background to that at the void's center. The measured CTR of the array system was 12.2 dB for the cyst (0.825mm) at the depth of 6.4 mm [Fig. 7(B)].

C. Excised Eyeball and Mouse Embryo

The excised pig and rabbit eye images in vitro were acquired by placing the area of interest (specifically the cornea and lens) near 6.4 mm. The active subaperture of the array was electronically scanned across the eyeball. For the 30 MHz array with 256-element, the width of the field of view in the azimuthal direction is 9.6 mm. The eyeball images from pig eye (A) and rabbit eye (B) are shown in Fig. 8. The anterior region, consisting of structures such as cornea and lens, were clearly seen.

The mouse embryo (E18.5) from a C57B6 (Jackson Lab) was scanned with the long axis of the array transducer oriented along the sagittal direction. Fig. 9(A) shows the image of an excised mouse embryo. Fig. 9(B–D) shows the images when the transducer was placed on the top of left side of the body, the middle of body and right side of the body respectively.

The anatomical details of a fully developed mouse embryo, including legs, paw and head, can be discerned.

D. Prebeamformer Data Acquisition

The prebeamformer data were down downloaded from system to a PC in the pre-beamformer data acquisition mode. In this mode, the raw data from all 64 channels are first temporarily stored in the memory. A read command from the PC downloads the data sequentially from channel 1 to channel 64. The process is repeated until one frame is acquired. The images are then reconstructed offline with methods or algorithms which are hard to be implemented with FPGA. Fig. 10(A) is an image obtained with the conventional delay and sum beamformer. Fig. 10(B) shows the image using the same data but with the coherent factor [9] in the beamformer. The image shows that the sidelobes have been greatly reduced by 10dB. More experimental investigation will be carried out with such methods or algorithms as adaptive coherent factor [9] to improve the performance of the system.

V. DISCUSSION AND CONCLUSION

A 64-channel digital imaging system for a 30 MHz, 256-element linear array transducer primarily developed as a platform for testing high frequency linear arrays fabricated in house has been designed and built. It allows a maximum frame rate of 50 frames per second to be achieved. Wire phantom images show the spatial resolution of 146 μm (lateral) and 54 μm (axial). Tissue images were acquired to demonstrate its imaging performance.

Current system can acquire up to 50 frames per second with 192 lines (9.6mm field of view in lateral and 12.8mm in axial). In recent years, small animals are widely used as a model to investigate cardiac functions because of their genetic similarity with humans [10]. Because small animals, especially mice, have a heart rate over 5 beats per second, this requires that an ultrasound imaging system has a fast imaging capability to image the heart motion over a complete cardiac cycle. For this purpose, the system needs to acquire at least 200 fps (frame per second). Such a frame rate would require in the worst case scenario (i.e. 192 lines per image, a maximum depth of view of 12 mm and a sampling frequency of 120 MHz) a data transfer rate close to 900 Mbps, which can not be obtained using our current digital acquisition board. Future work will involve designing a custom digital data acquisition board using PCI Express x8 technology, which could transfer data from the device to the PC at a rate of up to 5 Gbps [11], allowing the frame rate to be increased to above 200 fps.

A technology, capacitive micromachined ultrasonic transducers (cMUTs), that utilizes MEMS technology, has appeared in the horizon in recent year. It may have the potential in the development of HF linear arrays [2,12]. An even more attractive feature of this technology is its capability of integrating array elements with the imaging electronics [13], which has been demonstrated by preliminary results.

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Research Highlights

The highlights of this manuscript are:

1. This manuscript reports on the design and performances of a high frequency ultrasound imaging system comprising a 30-MHz 256-element array transducer, a 64-channel Tx/Rx and a 64-channel FPGA-based beamformer.
2. The system is an open structure design. It will help researcher in designing imaging systems for high frequency transducer arrays.
3. The system performance has been evaluated using wire phantom, tissue-mimic phantom and *ex vivo* tissues.

Fig. 1. Block diagram of the system. The system consists of 4 different boards: 8 pieces of transmitter board (32 channels on each), 2 pieces of digitizer board (32 channels on each), a backplane board and a timing controller board.

Fig. 2.

The -6 dB contour of simulation beam pattern (Top) and lateral intensity profile at focal point (Bottom) of linear array transducer (30 MHz, 50 μ m pitch) in lateral-depth plane with different active elements.

Fig. 3.

Block diagram of the analog subsystem. The subsystem consists of 8 boards: 32 channels on each board.

Fig. 4. Block diagram of the transmission beamformer. The delay values ($<1.067 \mu\text{s}$) and electrical scanning controls are stored in RAMs in FPGA.

Fig. 5.
Block diagram of the variable delay block.

Fig.6. Spatial resolution. Lateral: 130 μ m (simulation) vs 146 μ m (measured) Axial: 47 μ m (simulation) vs 54 μ m (measured)

Fig. 7. Images of a tissue mimicking phantom. The phantom consists of 1.09mm (A), 0.825mm (B), 0.53mm (C), and 0.3 mm cysts. The images are displayed with 50dB dynamic range.

Fig.8. Excised pig eye (A) and rabbit eye (B) were imaged with 30 MHz, 256-element array. The image is displayed with a 50dB dynamic range.

Fig. 9. Images of excised mouse embryo (E18.5). Transducer is positioned along the body of the embryo. (A) Picture of excised mouse embryo. (B) Bottom part of the embryo. (C) Middle part of the embryo (abdomen and thorax). (D) Top part (thorax and head). The dynamic range is 50dB.

Fig. 10.

In prebeamformer data acquisition mode, the raw data were downloaded from system to a PC. The images were reconstructed offline. (A) Conventional delay and sum beamformer. (B) Coherent factor processing was used in beamformer. The dynamic range is 50dB.

Table 1**CHARACTERISTICS of 64-CHANNEL BEAMFORMER**

Number of transmit channels	64
Number of receive channels	64
Number of bits per sample	12
Transmit delay resolution	2ns
Receive delay resolution	2ns
Transmit focusing	1
Receive focus	dynamic
Prebeamformer acquisition	Yes

Table 2

CHARACTERISTICS OF THE LINEAR ARRAY

Average frequency	30 MHz
Bandwidth	50%–70%
Element dimensions	2 mm × 44 μm
Kerf width	6 μm
Pitch	50 μm
Element	256