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Novel Multiplexer to Enable Multiple-Module Imaging with Adjustable High Spatial Resolution and Predetermined Display Bandwidth for Array Medical Imaging Systems

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Abstract

We describe a custom multiple-module multiplexer integrated circuit (MMMIC) that enables the combination of discrete Electron multiplying charge coupled devices (EMCCD) based imaging modules to improve medical imaging systems. It is highly desirable to have flexible imaging systems that provide high spatial resolution over a specific region of interest (ROI) *and* a field of view (FOV) large enough to encompass areas of clinical interest. Also, such systems should be dynamic, i.e. should be able to maintain a specified acquisition bandwidth irrespective of the size of the imaged FOV. The MMMIC achieves these goals by 1) multiplexing the outputs of an array of imaging modules to enable a larger FOV, 2) enabling a number of binning modes for adjustable high spatial resolution, and 3) enabling selection of a subset of modules in the array to achieve ROI imaging at a predetermined display bandwidth. The MMMIC design also allows multiple MMMICs to be connected to control larger arrays. The prototype MMMIC was designed and fabricated in the ON-SEMI 0.5 μ m CMOS process through MOSIS (www.mosis.org). It has three 12-bit inputs, a single 12-bit output, three input enable bits, and one output enable, so that one MMMIC can control the output from three discrete imager arrays. The modular design of the MMMIC enables four identical chips, connected in a two-stage sequential arrangement, to readout a 3 $\times$ 3 collection of individual imaging modules. The first stage comprises three MMMICs (each connected to three of the individual imaging module), and the second stage is a single MMMIC whose 12-bit output is then sent via a CameraLink interface to the system computer. The prototype MMMIC was successfully tested using digital outputs from two EMCCD-based detectors to be used in an x-ray imaging array detector system.

Finally, we show how the MMMIC can be used to extend an imaging system to include any arbitrary (M $\times$ N) array of imaging modules enabling a large FOV along with ROI imaging and adjustable high spatial resolution.

I. Introduction

IT is highly desirable to have flexible medical systems providing high spatial resolution over a ROI *and* FOV large enough to encompass areas of clinical interest. [1] To provide both of these features, a dynamic imager should be compatible with maintaining a specified display

bandwidth irrespective of the size of the imaged FOV. We present a custom multiplexer that has the capabilities of enabling: a large FOV by multiplexing outputs of an array of imaging modules, adjustable high spatial resolution by allowing use of different binning modes and, ROI imaging by selectively enabling a desired subset of modules at predetermined display bandwidth. Fig.1 depicts an EMCCD based individual imaging detector. Each detector consists of a phosphor (CsI) converting X-ray photons into light photons which are optically coupled to the EMCCD sensor through a fiber optic taper (FOT) and fiber optic plate (FOP), providing high resolution images.

II. Design & Construction

The prototype MMMIC was manufactured in the 0.5 μm ON-SEMI standard analog/mixed CMOS process through MOSIS [4]. Fig.2 shows the microphotograph of the MMMIC depicting important pin names. Each MMMIC consists of three 12 bit input data modules, an enable module and an output 12 bit data module. Each of these modules are described as follows.

A. Enable Module

An enable module as shown in Fig. 3 consists of three input enable signals E1, E2 & E3 (generated off chip) used to select one of the three 12 bit data input modules (Fig.4). Signals M1_E1, M2_E2 & M3_E3 are derived internally on chip using the logic depicted in Fig. 3. An output enable signal E_{out} is used as input enable signal for a MMMIC in a subsequent stage (if needed). The logic is designed such that E_{out} will be high only when one of the three input enable signals E1, E2 or E3 is high. This is done to prevent any false enabling in case more than one input enable signal is high at the same time. If any enable signals or all enable signals are ON at the same time then the E_{out} signal is OFF. Also if none of the signals is ON still E_{out} OFF.

B. Input Data Module

Three 12 bit data input modules M1, M2 & M3 are shown in Fig. 4. These have enable signals M1_E1, M2_E2 and M3_E3 coming from the enable module (Fig. 3). Each module consists of twelve 2-input OR gates.

C. Output Data Module

The final piece is a 12 bit data output module consisting of twelve 3-in-OR gates (Fig. 5). The first OR gate handles the first bits M1_D0, M2_D0 and M3_D0 from each of the three input modules, the second OR gate handles the second bits M1_D1, M2_D1 and M3_D1 from each of the three input modules and so on and so forth till the twelfth OR gate which handles the twelfth bits from each of the three module.

III. Operation

Each of the three 12 bit input modules M1, M2 and M3 receive their 12 bit data M1_{D0-D11}, M2_{D0-D11} and M3_{D0-D11} from their respective imaging arrays. The enable signals E1, E2 and E3 decide data from which module will be propagated to the output data module. Fig. 6 shows some cases depicting different combinations of the enable signals. Green color indicates that that particular module or enable signal is ON and the Red color indicates OFF.

All the possible cases for MMMIC are shown in the logic Table I. given below. As we can see from the logic table only in the cases when any one of the three enable signals are ON the data on the corresponding input modules is valid or in other words propagated to the

output. Whenever any two or all enable signals are ON simultaneously the output module is isolated from the input modules

This is to ensure data integrity so that we do not mix data's coming from multiple modules. Fig. 7 shows the timing diagram of the MMMIC. The final output on the first bit Dout_0 of the output module is shown with respect to the enable signals E1, E2 and E3 depending on the input data on the first bits of the three modules M1_D0, M2_D0 and M3_D0. The state of the Eout signals is also depicted. For example at time t_3 enable signals E1, E2 are OFF and E3 is ON allowing only the data on M3_D0 = '0' to propagate to Dout_0. If we take time t_5 we see that two enable signals E1 and E2 are ON while E3 is OFF. In this condition the output bit Dout_0 is totally isolated from any of the first bits of the three modules and stays in high state. Another case is at t_4 where none of the enable signals E1, E2 and E3 are ON, again rendering output bit Dout_0 in high state.

IV. Array Imaging

As discussed earlier to increase the field of view individual EMCCD detector modules are arranged in an array configuration as shown in Fig. 8. Each detector module gives a 12 bit digital output.

Since MMMIC was designed specifically keeping in mind its use for array imaging, each set of the 12 bit digital outputs from nine modules is fed to an arrangement of MMMICs in a two stage configuration. Fig. 9 given below describes an arrangement of four MMMIC's in a two stage configuration used for 3×3 array imaging.

For 3×3 array imaging we have nine imaging modules as shown in Figs. 8 and 9. Since each MMMIC can handle 12 bit data from three imaging modules, in total we thus have three MMMIC's to acquire data from nine modules. 12 bit outputs from each of the first stage MMMIC's act as 12 bit input data for the second stage MMMIC. Eout1, Eout2 and Eout3 signals from MMMIC I, II and III respectively act as enable signals for the second stage MMMIC. Similarly by adding more number of MMMIC's in multiple stages we can virtually connect any arbitrary ($M \times N$) imaging modules thereby providing virtually infinite field of view.

V. Test Setup and Results

For initial testing we used two EMCCD based cameras [2], [3]. The 12 bit digital outputs from the two cameras were connected to two input modules of a single MMMIC. The enable signals E1 and E3 were generated using a FPGA (Xilinx Spartan 3E XC3S250E). The 12 bit digital output of the MMMIC was fed to the imaging system computer using a standard Camera-Link interface. Fig. 10 depicts the optical images of a CT slice of a head acquired using individual sensors wherein the 12 bit data from the Left sensor ($1K \times 1K$) was fed to module M3 of MMMIC and 12 bit data from the Right sensor ($1K \times 1K$) was fed to module M1 of MMMIC. Fig. 11 shows the final $2K \times 1K$ optical image formed in the imaging computer from the data obtained from two sensors using MMMIC.

Conclusion

We describe the design and operation of a custom multiplexer circuit that has been fabricated on a single integrated circuit. The benefits are as follows:

Extensibility

The MMMIC is extensible to any arbitrary array of ($M \times N$) multiple-module imaging configuration, using a MMMIC configuration similar to that depicted in Fig. (2). This

cannot be practically achieved by other means (e.g. taking all data in parallel to the imaging system computer).

ROI Imaging

We can do region of interest (ROI) imaging by selectively enabling the desired module that contains the region of interest.

Adjustable high spatial resolution

The output will always be of a pre-determined display bandwidth (e.g. 1K×1K) irrespective of the number of modules active which is achieved through selective enabling and binning allowed by the MMMIC, providing an adjustable high spatial resolution.

References

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Fig. 1. An EMCCD based X-ray detector module with following components 1). CsI phosphor 2). Fiber optic taper 3). Fiber optic plate 4) EMCCD headboard 5). An individual EMCCD sensor

Fig. 2.
Microphotograph of MMMIC

Fig. 3.
Enable module in MMMIC

Fig. 4.
Three Input modules M1, M2 & M3 in MMMIC

Fig. 5.
Output module in MMMIC

Fig. 6.

Operation of MMMIC. a) E1 is ON, propagating data from M1 to Output. b). E2 is ON, propagating data from M2 to Output. c). E3 is ON, propagating data from M3 to Output. d). E2 and E3 are ON at the same time, rendering the output invalid irrespective of any incoming data.

Fig. 7.
Timing diagram for MMMIC

Fig. 8.
A 3×3 array of EMCCD based detector module

Fig. 9.
Two stage configuration of four MMIC's for 3x3 array imaging.

Fig. 10.
1K×1K Image from Left Sensor
1K×1K Image from Right Sensor

Fig. 11.

Final 2K×1K Image. Image processing that would eliminate the border artifact is not considered here as it is beyond the scope of this paper

Table I

Logic Table for MMMIC

I/P Enable			O/P Enable	Modules		
E1	E2	E3	Eout	M1	M2	M3
1	0	0	1	Valid	Not Valid	Not Valid
0	1	0	1	Not Valid	Valid	Not Valid
0	0	1	1	Not Valid	Not Valid	Valid
1	1	0	0	Not Valid	Not Valid	Not Valid
1	1	1	0	Not Valid	Not Valid	Not Valid
0	0	0	0	Not Valid	Not Valid	Not Valid