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Quantum Performance Analysis of an EMCCD-based X-ray Detector Using Photon Transfer Technique

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Abstract

The low electronic noise, high resolution, and good temporal performance of electron-multiplying CCDs (EMCCDs) are ideally suited for applications traditionally served by x-ray image intensifiers. In order to improve an expandable clinical detector's field-of-view and have full control of the system performance, we have successfully built a solid-state x-ray detector. The photon transfer technique was used to quantify the EMCCD quantum performance in terms of sensitivity (or camera gain constant, K), read noise (RN), full-well capacity (FW), and dynamic range (DR). Measured results show the system maintains a K of $11.3 \pm 0.9 e^-/\text{DN}$ at unit gain, with a read noise of $71.5 \pm 6.0 e^-_{\text{rms}}$ at gain 1, which decreases proportionally with higher gains. The full well capacity was measured to be $31.3 \pm 2.7 ke^-$, providing a dynamic range of 52.8 ± 0.7 dB using the chip manufacturer specified clocking scheme. Similar performance was measured with other commercial camera systems. The manufacturer data sheet indicates a dynamic range of 66 dB is plausible with improved read noise and full well capacity. Different clocking schemes are under investigation to assess their impact on improving performance towards idealized values. EMCCD driver clock voltage levels were adjusted individually to check the influence on quantum performance. The clocks work to transfer charge from the image area to readout amplifier through

the storage area, horizontal and multiplication registers. Results indicate that the clock that contributes to lateral overflow drain bias is essential to the system performance in terms of dynamic range and full well capacity. The serial register clocks used for transporting charge stored in the pixels of the memory lines to the output amplifier had the largest effect on RN, while others had less of an impact. Initial adjustment of these clocks resulted in a variability of 16% in the performance of dynamic range, 38% in read noise and 56% in full well capacity. Quantifying the quantum performance provides valuable insight into overall performance and enables optimal adjustment of the clocking scheme. Further improvements are expected.

I. Introduction

ELECTRON-MULTIPLYING CCDs (EMCCDs) are a near ideal imaging platform for providing high sensitivity, high speed, high resolution, and low noise images for bio-medical imaging applications. The charge carrier multiplication register directly multiplies charge on chip, in solid state, before its conversion to a voltage signal, thus suppressing the effective read-out noise to negligible levels. We have built an EMCCD imaging module from the component level to be used in a solid state x-ray image intensifier (SSXII) system [1] using the Texas Instruments EMCCD chip TC285SPD to provide full control over the system configuration and to enable expansion towards clinical field of views using an array configuration. The system includes an EMCCD chip, power supply, power board, driver boards, FPGA board, head boards and data acquisition board. In this paper, we present a quantum performance analysis using the photon transfer technique [2] to evaluate the driver clock's voltage levels' contribution to the performance of the EMCCD camera, in terms of sensitivity (camera gain constant, K), read noise (RN), full-well capacity (FW) and dynamic range (DR).

Proper timing (phasing) and voltage levels of the driving clocks are crucial for maximizing performance. The driving clocks for the EMCCD input pins include: Overflow Drain Bias (ODB) for anti-blooming and channel clearing, Image Area Gate (IAG1 and IAG2) for charge transfer through the image sensing area, Storage Area Gate (SAG1 and SAG2) for charge transfer through the image storage area, Serial Register Gate (SRG1 and SRG2) for horizontal charge transfer through the serial register, Charge Multiplication Gate (CMG) for transferring and amplifying the charge through the multiplication register, and Reset (RST) for controlling the readout amplifier. The sensor topology diagram is shown in Figure 1 below.

The typical voltage values in table 1 are recommended by the manufacturer, and the minimum and maximum values were used in the range of values tested, as described in the subsequent sections.

II. MATERIALS

The EMCCD chip used was model TC285SPD from Texas Instruments Japan (TIJ) with a 1046×1004 pixel matrix and 35MHz maximum rated speed. Figure 2(a) shows the sensor and its driver board. The entire system setup includes the enclosure, sensor, driver, power and CameraLink, as shown in Figure 2(b).

III. METHODS

In order to complete the quantum analysis of the system, the photon transfer technique was used. This technique has proven to be a valuable method for calibrating, characterizing, and optimizing performance of CCDs [2].

Incident light photons were generated by using a pulsed green LED bar array. Figure 3 is the test system setup. Uniform light was incident to the surface of the EMCCD and then was converted into electrons, which are digitalized by a double correlated sampling ADC.

Using a measurement of the signal and noise in the digital image of the uniform light source, the camera gain constant (K) can be determined, which provides the conversion factor from arbitrary units of digital numbers (DN) to absolute units of electrons (e^-). Once K is known, parameters including the read noise, full well capacity and dynamic range can be quantified in absolute terms. The following equation yields K [2]:

$$K = \frac{S(DN)}{\frac{\sigma_S^2(DN)}{F^2} - \sigma_R^2(DN)} \quad (1)$$

$$F = \sqrt{2(M-1)M^{-\frac{N-1}{M}} + \frac{1}{M}} \quad (2)$$

Where $S(DN)$ is the mean value of the digital output signal, $\sigma_S^2(DN)$ is the variance of the digital output signal, $\sigma_R^2(DN)$ is the read noise floor variance, and F is the excess-noise factor [3] which is determined by M , the EMCCD gain, and N , the total number of multiplication stages in the multiplication register ($N=400$ for the sensor used).

With knowledge of K , the read noise can be calculated by taking $\sigma_R(DN) \times K$ to convert to units of rms e^- . The full well capacity is measured by multiplying K and the saturation DN value of the $M=1$ signal. Finally, the dynamic range can be derived by taking the ratio of the full well capacity and the read noise and converting to decibels. Analyzing these quantum performance parameters while adjusting the input clock voltage levels, allows optimization of the clocking scheme using the following quantitative objectives: minimizing the read noise while maximizing the full well capacity and dynamic range.

IV. RESULTS AND DISCUSSIONS

The camera gain constant K was measured to be $11.3 \pm 0.9 e^-/DN$ using the manufacturer recommended clocking scheme and the photon transfer technique. K was also inversely proportional to the EMCCD gain. Hence, it was crucial to measure the EMCCD gain response with CMG voltage (which provides the solid state electron multiplication).

The gain curve in Figure 4 shows a plot of the absolute gain versus CMG voltage, which is in agreement with the expected response based on manufacturer specifications [4]. Variable gains can easily be achieved, ranging from 1 to upwards of 200 times, sufficient for a wide variety of incident exposure levels.

The dynamic range is one of the most important parameters in medical imaging applications. Initially, all input clock voltages were set to their typical value, and the dynamic range was measured to be 52.8 ± 0.7 dB, which is indicated in Figure 5. Finer adjustment of the ODB clock indicates its relative importance on performance, as shown in Figure 5. By changing ODB low level from 3.5V to 7V, dynamic range changed by 16%.

On the other hand, no statistically significant change in dynamic range was observed when changing the RST, SRGs, IAGs and SAGs levels, although they were varied separately to their extreme values indicated in Table 1.

Similar investigations were conducted to check the influences of different clock voltage configurations on read noise and full well capacity.

The readout noise was measured to be 71.5 ± 6.0 e- rms at an EMCCD gain of 1. By changing clock configurations, as shown in Figure 6 above, the readout noise varied by 30%. The effective readout noise decreases with the increase of the on-chip gain. At a moderate gain of 50, the readout noise was only 1.43 e- rms.

The serial register clocks (SRG) help transport charge stored in the pixels of the memory lines to the output amplifier. SRG was shown to contribute the most to system readout noise. This clock serves as the last clock before charges are transferred to the readout portion, which waits for the RST clock for eventual read out. Thus it can introduce electronic noise when using different clock voltages.

The full-well capacity was measured to be 31.3 ± 2.7 ke-, and its response with different clock configurations is indicated in Figure 7. The ODB clock was shown to have a significant suppressing influence on the full well capacity, which varied from 33 ke- to 18 ke-. The reason for such performance lies in the function of ODB clock, which sets the bias to drain away extra electrons from the pixels. The higher the ODB low voltage level, the lower the well capacity of each pixel [4]. Setting SRGs at a lower voltage level leads to the enhancement of the full well capacity, but also introduces more readout noise, as shown in Figure 6.

V. CONCLUSION

Using the photon transfer technique, we successfully measured the system sensitivity, readout noise, full well capacity and dynamic range and their variation with different individual input clock voltage values. Results show that readout noise varies greatly with SRGs, but it can decrease with on-chip gain. ODB also is a key factor in the value of full well capacity. Varying the DC bias of ODB enables control of the blooming protection level due to the advanced lateral overflow drain structure, which must be balanced with the full well capacity. Dynamic range is greatly affected by the ODB and SRGs clock voltages, while other clocks have much less effect. Using this analysis, we were able to improve the performance of the detector. Further optimization should lead to even greater improvements.

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Fig 1.
EMCCD TC285SPD sensor topology diagram.

Fig. 2.

(a) EMCCD sensor and its driver board. (b) The system hardware was built based on the EMCCD sensor. This design was constructed to support 4 EMCCDs. Only one is shown on the upper left slot.

Fig. 3. Test system set up diagram. Flat field correction was used to eliminate the residual fixed pattern from the images.

Fig. 4.
EMCCD absolute gain response vs. CMG voltage value.

Fig. 5. Dynamic range response with different clock voltage configurations. The voltage levels were set to their “typical” level unless otherwise noted.

Fig. 6.

Readout noise response with different configurations. The voltage levels were set to their “typical” level unless otherwise noted.

Fig. 7. Full-well capacity response with different configurations. The voltage levels were set to their “typical” value unless noted.

Table I

Range of input clock voltage values specified by the manufacturer

Input Clocks	High Voltage Level (V)			Low Voltage Level (V)		
	Min	Typical	Max	Min	Typical	Max
ODB		12.5		3.5	5.2	7*
IAG1	3.2	3.5	3.8		-5.7	
IAG2	2.9	3.1	3.5		-5.7	
SAG1	3.2	3.5	3.8		-5.7	
RST	5.5	6.0	6.5		0	
SRG1	7.5	7.8	8.1		0	
SRG2	7.5	7.8	8.1		0	
CMG	7.0		22		-3.8	

* ODB low voltage level was expanded Beyond the manufacturer's specified range of 4.9-5.5V to investigate extreme conditions.