Published in final edited form as:

Mater Sci Eng R Rep. 2010 November 22; 70(3-6): 354–370. doi:10.1016/j.mser.2010.07.003.

Graphene-Dielectric Integration for Graphene Transistors

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Abstract

Graphene is emerging as an interesting electronic material for future electronics due to its exceptionally high carrier mobility and single-atomic thickness. Graphene-dielectric integration is of critical importance for the development of graphene transistors and a new generation of graphene based electronics. Deposition of dielectric materials onto graphene is of significant challenge due to the intrinsic material incompatibility between pristine graphene and dielectric oxide materials. Here we review various strategies being researched for graphene-dielectric integration. Physical vapor deposition (PVD) can be used to directly deposit dielectric materials on graphene, but often introduces significant defects into the monolayer of carbon lattice; Atomic layer deposition (ALD) process has also been explored to deposit high- κ dielectrics on graphene, which however requires functionalization of graphene surface with reactive groups, inevitably leading to a significant degradation in carrier mobilities; Using naturally oxidized thin aluminum or polymer as buffer layer for dielectric deposition can mitigate the damages to graphene lattice and improve the carrier mobility of the resulted top-gated transistors; Lastly, a physical assembly approach has recently been explored to integrate dielectric nanostructures with graphene without introducing any appreciable defects, and enabled top-gated graphene transistors with the highest carrier mobility reported to date. We will conclude with a brief summary and perspective on future opportunities.

Keywords

semiconductor; graphene; transistor; dielectrics; nanowires; nanoribbons

1. Introduction: the promise and challenges for graphene electronics

1.1 The promise of graphene electronics

Graphene is a one-atom-thick planar sheet of sp^2 -bonded carbon atoms arranged in a honeycomb crystal lattice (Fig. 1a and b) [1, 2]. Graphene has attracted considerable interest in the past several years due to its significant potential for both the fundamental studies and technological applications [3–21]. Graphene is characterized by a linear dispersion relation with the Dirac point separating the valence and conduction bands with a zero bandgap, which limits the achievable on-off current ratios but does not rule out analogue radio frequency (RF) device applications. In particular, it has been demonstrated that graphene exhibits the highest carrier mobilities exceeding 200,000 $cm^2/V\cdot s$ [11], which is not only

~100 times greater than that of silicon but also about 10 times better than the state-of-the-art high mobility semiconductors lattice-matched to indium phosphide. Along with many other desirable properties, including large critical current densities ($\sim 2 \times 10^8$ A/cm²) [22], a high saturation velocity (5.5×10^7 cm/s) [23], and a micrometer-scale mean free path at room temperature, graphene is currently regarded as a highly promising materials for high-speed electronics [23–28]. These desirable properties promise graphene to offer excellent short-circuit current-gain cutoff frequency (f_T) and for high frequency applications. In particular, it has been recently demonstrated that high speed graphene devices were achieved with a cutoff frequency f_T reaching up to 100 GHz, demonstrating the significant potential of graphene devices for radio frequency (RF) applications (Fig. 1c and d) [25].

Due to the zero-band-gap nature, bulk graphene remains highly conductive even at the charge neutrality point, and therefore cannot be used for effective field-effect transistors (FETs) at room temperature for digital applications. The formation of graphene nanostructures with lateral quantum confinement can open up a finite band gap to enable room temperature FET operation (Fig. 2) [10,29–37]. It has been demonstrated that sub-10 nm graphene nanoribbons (GNRs) can be created, and used to fabricate FETs that can be effectively switched off at room temperature [31,32]. We have recently developed a rational approach to fabricate GNRs with controllable widths from 6–20 nm using chemical synthesized nanowires as the physical etch masks [35]. Importantly, using such GNR as the semiconducting channel, we have fabricated room temperature FETs with on-off ratios >100 (Fig. 2a). It has also been demonstrated that graphene nanomesh, as a mimick of graphene nanoribbon networks, can effectively introduce a finite conduction band gap into the two-dimensional graphene to enable room temperature transistors with comparable on/off ratios (Fig. 2b) [34].

1.2 Graphene dielectric integration and its impact on transistor performance

The gate dielectric is an essential component of a transistor. Compared to the semiconductor channel, the gate dielectrics have received much less attention due to the relative uninteresting nature of an insulator, despite its significant impact on the critical device parameters including transconductance, subthreshold swing and frequency response. Among the various strategies explored to fabricate graphene or graphene nanostructure based FETs, most efforts employ a silicon substrate as a global back gate and a 300 nm thick silicon dioxide (SiO₂) as the gate dielectrics. This substrate is used primarily because the graphene can be readily visualized using optical microscope on this particular substrate due to optical interference [38–42]. The readily viewable graphene on the 300 nm SiO₂ substrate has allowed easy device fabrication and led to many interesting scientific discoveries. The requirement of 300 nm SiO₂, however, can intrinsically limit the resulted device performance in several perspectives. First, optical detection technique to visualize graphene has been demonstrated and widely used for a SiO₂ thickness of 300 nm, but a 5% variation in thickness (e.g. to 315 nm) can significantly lower the contrast [40]. Second, the devices made on 300 nm SiO₂ substrate have small gate capacitance due to the relatively large dielectric thickness and the small dielectric constant, and thus require high switching voltage [43].

Exploring high- κ dielectric substrate may mitigate these problems [43,44]. For example, we have demonstrated that 72 nm Al₂O₃/Si substrate is superior to the 300 nm SiO₂/Si substrate for both the visualization of graphene and improve the transistor performance [43]. Compared to the 300 nm SiO₂/Si substrate, the 72 nm Al₂O₃/Si substrate can enhance the optical contrast of single layer graphene by at least 3 times. Furthermore, using the Al₂O₃ film as the gate dielectrics, the back-gated graphene FETs have been fabricated to exhibit more than 7-fold increase in transconductance.

It is important to note that the carrier mobility of the resulting graphene transistors can be significantly impacted by the nature of the dielectric layer and graphene-dielectric interface. Theoretical studies suggest that the intrinsic mobility of graphene, set by longitudinal acoustic (LA) phonon scattering, can reach $10^5 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ at room temperature [45]. However, the achievable carrier mobility in an actual device can often be limited by extrinsic scattering sources, many of which arise from the surface morphology, chemistry, structural, and electronic properties of the substrate. For example, recent calculation suggests that a mobility as high as $44,000 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ can be achieved in graphene on SiO_2/Si substrate at room temperature, which is limited by the phonon scattering [45–48]. Experimental studies have demonstrated that mobility values in the range of $2 - 20 \times 10^3 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ for the graphene transistor made on SiO_2/Si substrate [49]. The variability in mobility is attributed to various degrees of local disorder in graphene and in the dielectric substrate.

Increasing the mobility beyond the extrinsic limits is one of the central challenges of the graphene community. Recently, two groups have reported a significant improvement in the mobility of suspended graphene after current-heating annealing [12,50]. However, a more device friendly solution may rely on placing graphene on a different substrate. Several alternatives have been explored, however, the mobility obtained so far is comparable to that on SiO_2 [51]. Utilization of high- κ dielectric material as the gate insulator is expected to partially screen charged impurities and enhance the carrier mobility [48]. A recent report demonstrate significant carrier mobility improvement to $7 \times 10^4 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ in graphene transistors using single-crystal epitaxial $\text{PbZr}_{0.2}\text{Ti}_{0.8}\text{O}_3$ (PZT) films as the gate oxide [44]. This remarkable improvement was attributed to the strong screening of PZT film and possible ordered adsorbate molecular layer at interface that may reduce the scattering [52].

On the other hand, most studies of graphene transistors discussed above employ a silicon substrate as a global back gate, which, although useful for fundamental investigations, will be of limited use for practical applications due to the inability to independently address multiple devices on the same chip. Top-gated devices can readily allow independently addressable device arrays and functional circuits, and therefore are of significant interest [53–55]. The formation of top-gated graphene transistors requires direct deposition of dielectric oxide material on top of pristine graphene, which is of significant challenge due to the intrinsic incompatibility between these two types of materials. Deposition of oxide dielectrics onto graphene for top-gated transistors can often introduce substantial defects into graphene lattice and lead to significant degradation in carrier mobilities [23,27,56–61]. Here we review various strategies, including physical vapour deposition (PVD), atomic layer deposition (ALD) and physical assembly approach, for graphene-dielectric integration for top-gated graphene transistors, discussing the potential merits and challenges of each.

2. Physical vapor deposition of top-gate dielectrics on graphene

Physical vapour deposition (PVD) such as electron-beam evaporation or sputtering process is a common approach to deposit a variety of oxide dielectric thin films on many different substrates including graphene. However, the PVD process usually yields lower quality dielectrics and can cause significant damages to graphene.

2.1 Raman characterization of graphene-dielectric integration by PVD

Raman spectroscopy has been used to study the interaction between single layer graphene and PVD dielectrics (Fig. 3) [62]. Various PVD approaches, including electron beam evaporation, pulsed laser deposition (PLD) and radio frequency (RF) sputter, were explored to deposit SiO_2 layer on graphene. Raman spectra of the graphene covered with these PVD SiO_2 layers all show large defect band (D-band), indicating substantial defects introduced

into the graphene lattice. Strong defect-induced D band was also observed in Raman spectra of graphene covered with PLD deposited HfO_2 . In contrast, simple spin coating of polymer dielectric such as polymethyl methacrylate does not introduce D-band. These results clearly demonstrate that PVD process can result in significant damage to carbon lattice, and simple spin coating would not introduce obvious defects.

2.2 Top-gated graphene transistors using PVD dielectrics

The PVD dielectric film can be used as top-gate dielectrics for graphene transistors. However, due to the significant damage the process can cause, the mobility values observed in the top-gated devices fabricated from this process are typically nearly one order of magnitude smaller than what can be achieved in the back-gated devices. For example, Lemme et al. reported the top-gated graphene transistor, in which electron-beam evaporated SiO_2 was used as top gate dielectrics [58]. Before the deposition of the top-gate dielectrics, the charge carrier mobilities in the uncovered graphene are estimated to be $\mu_h = 4790 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ and $\mu_e = 4780 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$. In stark contrast, the room temperature mobility values are severely degraded to $\mu_h = 710 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ and $\mu_e = 530 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ after the deposition of the SiO_2 (Fig. 4). This study highlights that the PVD deposited dielectric layer can significantly disrupt the charge transport characteristics in graphene.

3. Atomic layer deposition of top-gate dielectrics on graphene

Atomic layer deposition (ALD) is a well developed approach for growing high- κ gate dielectric layers, owing to its precise control over the film thickness and uniformity [63]. However, the direct deposition of high- κ dielectric materials, such as Al_2O_3 and HfO_2 , on graphene using H_2O -based ALD is not possible because of the hydrophobic nature of graphene basal plane [64] and the lack of functional groups for molecular absorption which is necessary for ALD.

3.1 Challenges in direct ALD of top-gated dielectrics on graphene

The attempt to directly deposit oxide dielectrics on pristine graphene using ALD failed to produce continuous layer of dielectrics. Given that a perfect graphite surface is chemically inert [65], attempts to grow ALD Al_2O_3 layer on a clean highly oriented pyrolytic graphite surface lead to only a selective growth at the steps between graphite layers, where the broken carbon bonds along the terraces serve as one-dimensional nucleation center for the initial ALD process [66]. Fig. 54a,b shows AFM images of the same area before and after ALD of $\sim 2 \text{ nm}$ Al_2O_3 . Before ALD, the height of the triangular graphene piece at the bottom and the large piece on the left was ~ 1.7 and $\sim 2.0 \text{ nm}$, respectively. Near the edge of the graphene, there was also a narrow $\sim 1.0 \text{ nm}$ high stripe. After ALD, $\sim 2.0 \text{ nm}$ Al_2O_3 was coated on SiO_2 ; The apparent topography height of the three graphene sheets was obviously reduced to a level similar to that of the ALD-coated SiO_2 . The height difference before and after ALD suggests that no Al_2O_3 was effectively coat on pristine graphene sheets. This is because ALD relies on chemisorption and rapid reaction of precursor molecules with surface functional groups [67,68]. As a result, no ALD can occur on the pristine graphene plane since it does not have any dangling bonds or surface functional groups to react with the precursors. Interestingly, quasicontinuous bright lines of Al_2O_3 preferentially grown on the edges of graphene sheets, suggesting dangling bonds on the edges or possible termination by $-\text{OH}$ or other reactive species. Some bright dots in the middle of graphene sheets may correspond to ALD Al_2O_3 island around the defects such as pentagon-hexagon pairs or vacancies known to exist in graphite [69].

The unsuccessful ALD attempt to deposit oxide dielectrics on graphene calls for additional surface functionalization to create functional groups for oxide nucleation. The key idea

enabling the high- κ dielectric layer growth on graphene by ALD is to provide intentional nucleation sites on the inert surface of graphene. To this end, Lin et al. have used a functionalization layer consisting of 50 cycles of NO_2 -TMA (trimethylaluminum) in ALD process prior to the growth of gate oxide. This NO_2 -TMA functionalization layer was essential for the ALD process and allows to achieve a uniform thin (<10 nm) coating of oxide dielectrics on graphene without producing pinholes [70]. The dielectric constant of ALD-grown Al_2O_3 in this way was determined to be about 7.5 by capacitance-voltage measurements.

Top-gated graphene transistors have also been fabricated using dielectric deposited with this method [27]. Fig. 6a and b shows an schematic view and SEM image of the device with the e-beam lithography defined Ti/Au (1 nm/50 nm) thin film as the source and drain electrodes, a 12 nm thick Al_2O_3 layer was then deposited by ALD at 250 °C as the gate insulator, and Pd/Au (10 nm/50 nm) thin film the top gate. DC electrical characterization was conducted to determine the device performance. Fig. 6c shows the conductance, $G = I_D/V_D$, of a graphene device before ALD oxide deposition using the silicon substrate as the back gate and a DC source-drain bias V_D of 100 mV, and the inset of Fig. 6c shows the transfer characteristics after ALD oxide deposition. Based on these plot, it is evident that there was significant reduction in both the device conductance and field-effect mobility after the deposition of top gate dielectrics by ALD. The current and mobility degradation in the oxide-covered devices may be attributed to charged impurity scattering associated with the NO_2 functionalization layer and interface phonon scattering in the oxide [45]. Other similar attempts by using O_3 functionalization [64], or simply nucleating the dielectric growth from impurities on graphene without prior cleaning [23] has resulted in devices with significant degradation in carrier mobility. These results indicate that further optimization or alternative dielectrics deposition method are required in order to retain the high intrinsic mobilities in graphene [71,72].

3.2 Molecular buffer layer for ALD deposition of oxide dielectrics on graphene

The functioning of graphene surface for ALD growth of oxide will inevitably break the chemical bonds in the graphene lattice, leading to severe degradation in the electronic performance of the graphene devices. To mitigate this problem, various buffer layers have been introduced to help the nucleation and growth of the oxide dielectrics on graphene and at the same time minimizes the potential damage to the carbon lattice.

Wang et al. carried out the initial studies to investigate the ALD deposition of dielectrics on graphene using a molecular buffer/nucleation layer [73]. In their studies, the mechanical peeled graphene sheets were soaked in 3,4,9,10-perylene tetracarboxylic acid (PTCA) solution for ~30 min, thoroughly rinsed, and blown dry. The chip was immediately loaded into the ALD chamber to prevent contamination by molecules in the air. The deposition of Al_2O_3 film was carried out at ~100 °C using trimethylaluminum and water as the precursors [74]. Atomic force microscopy (AFM) imaging was used to characterize the few-layer graphene sheets and their integration with graphene.

The PTCA-treatment of the sample introduces a high density of carboxylate-terminated perylene molecules and achieves densely packed functional groups to allow ALD deposition of continuous uniform layer of ultrathin Al_2O_3 on graphene (Fig. 7a). Fig. 7b,c shows AFM images of the same area before and after deposition of ~2 nm Al_2O_3 . Before ALD, the height of the graphene under the line cut was ~1.6 nm, which increased to ~3.0 nm after ALD. The relative height increase of Al_2O_3 -coated graphene was partly attributed to the thickness of PTCA layer, which was usually ~0.5–0.8 nm observed by AFM after PTCA coating step. The actual Al_2O_3 on graphene was $\sim 2.8 \pm 0.2$ nm thick in Fig. 7c. AFM images show continuous coverage of dielectric layer on the entire graphene area with a root of mean

square roughness of the Al_2O_3 film on graphene about 0.33 nm, suggesting the uniform packing of the underlayer PTCA molecules. Previous high vacuum STM studies have confirmed two modes of epitaxial packing of the PTCA precursor, perylene tetracarboxylic dianhydride, along the lattice lines of highly oriented pyrolytic graphite [75,76]. As the partitioning of PTCA from methanol to the graphene interface is highly favorable, it is likely that similar epitaxial packing is occurring in the solution phase, yielding dense, uniform coating on graphene. This self-assembled PTCA layer on graphene is responsible for uniform Al_2O_3 film coating. The noncovalent functionalization method is not destructive to graphene lattices and can be used for depositing ultrathin high- κ dielectrics for future graphene electronics [27].

3.3 Metal oxide buffer layer for ALD of dielectrics on graphene

An alternative buffer layer is oxidized metal thin film. In this approach, a very thin layer of metal film is first deposited on graphene and allowed to oxidize to form a thin oxide layer, which can function as the nucleation layer for subsequent oxide deposition by ALD. For example, Kim et al. introduced a thin nucleation layer of oxidized aluminum between the graphene layer and the Al_2O_3 dielectric [77]. Prior to the Al_2O_3 layer growth by ALD, a 1–2 nm thick aluminum layer was deposited on the graphene surface by e-beam evaporation. This aluminum nucleation layer is completely oxidized as soon as the sample is exposed in air before transferring into ALD chamber [78,79]. The samples were transferred to the ALD chamber for the deposition of Al_2O_3 using trimethylaluminum as the aluminum source and H_2O as oxidizer. Initial stage of ALD growth starts with an H_2O oxidizing cycle at elevated temperatures to ensure the complete oxidation of aluminum.

Top-gated graphene transistors have been fabricated to test the dielectric quality and its impact on the graphene devices. To fabricate the device, nickel thin film as the source and drain electrodes were first defined using electron beam lithography on mechanically peeled graphene, followed by an annealing step in a hydrogen atmosphere at 200 °C to remove possible contaminants such as resist residues [80]. Al nucleation layer was then deposited by high vacuum e-beam evaporator. The sample was then exposed in air and transferred into the ALD chamber and go through 167 cycles of Al_2O_3 deposition, resulting in a 15 nm thick Al_2O_3 film deposition. A 50 nm thick nickel top-gate electrode was subsequently fabricated to obtain the final device (Fig. 8a,b).

The electrical transport characterizations were conducted at room temperature in a vacuum probe station. The top-gate electrode and the silicon substrate are used as a local gate and global back-gate, respectively, to control the carrier concentration and polarity in the graphene layer. Fig. 8c shows the total device resistance (R_{tot}) as a function of top-gate voltage measured at different back-gate biases from – 40 to 40 V and a drain bias of $V_{\text{D}} = 0.1$ V. At $V_{\text{BG}} = 0$ V, the sample resistance reaches a maximum (Dirac point) at $V_{\text{Dirac,TG}} = 0.08$ V. This observation indicates that there is little unintentional doping of the graphene sample after the top-gate stack deposition. As $|V_{\text{TG}} - V_{\text{Dirac,TG}}|$ increases, the electron or hole concentration in the graphene channel increases and R_{tot} decreases, resulting in V-shaped traces. Importantly, the top-gated device shows a very small hysteresis less than 0.05 V, and low leakage current less than 0.75 pA/ μm^2 through the Al_2O_3 dielectric, highlighting a high dielectric quality and a low interface state density.

The R_{tot} versus V_{TG} measured at different V_{BG} values shows an applied V_{BG} bias changes the position of the Dirac point and also shifts vertically the measured resistance values (Fig 8c). The change in the Dirac point position can be explained as follows: a positive (negative) V_{BG} bias induces a finite concentration of electrons (holes) in the active area, which is proportional to the back-gate capacitance (C_{BG}). In order to restore the device to the Dirac point, where the carrier concentration is minimum, a negative (positive) applied V_{TG} is

required. The vertical shift is caused by the resistance change in the un-top-gated regions of the graphene flake. The shift of the top-gate Dirac points as a function of V_{BG} can be used to determine top-gate and back-gate capacitances, $C_{TG}/C_{BG} \sim 28$ (inset of Fig. 8c). Using the back-gate capacitance value of $C_{BG}=11 \text{ nF/cm}^2$, the top-gate capacitance can be estimated to be $C_{TG}=306 \text{ nF/cm}^2$, corresponding to a relative dielectric constant of 6.0 for the Al_2O_3 film.

To determine the impact of the dielectric deposition, it is important to determine the carrier mobility. To accurately derive the mobility value, the contact resistance should be carefully excluded as it is comparable to the graphene transistor channel resistance. The authors have adopted a model to exclude the impact of the contact resistance as detailed below. The carrier concentrations (electrons or holes) in the graphene channel regions n_{tot} can be approximated by

$$n_{tot} = \sqrt{n_0^2 + n[V_{TG}^*]^2} \quad (1)$$

where n_0 represents residual carrier concentration at Dirac point, which should be zero for an ideal, disorder-free graphene layer and none zero in present of charged impurities located either in the dielectric or at the graphene/dielectric interface [81]. $n[V_{TG}^*]$ represents the carrier concentration induced by the top-gate bias away from the Dirac point, $V_{TG}^* = V_{TG} - V_{TG,Dirac}$. The expression for $n[V_{TG}^*]$ is obtained from the following equation relating V_{TG} , C_{ox} , and the quantum capacitance of the two-dimensional electrons in the graphene channel:

$$V_{TG} - V_{TG,Dirac} = \frac{e}{C}n + \frac{\hbar v_F \sqrt{\pi n}}{e} \quad (2)$$

The total device resistance R_{tot} is given by

$$R_{tot} = R_{contact} + R_{channel} = R_{contact} + \frac{L/W}{ne\mu} = R_{contact} + \frac{L/W}{\sqrt{n_0^2 + n[V_{TG}^*]^2}e\mu} \quad (3)$$

where $R_{channel}$ is the resistance of the graphene channel covered by top-gate electrode, the contact resistance $R_{contact}$ consists of the uncovered graphene section resistance and the metal/graphene contact resistance, and L and W represent the channel length and width the top-gated area [23]. By fitting this model to the measured data, the authors extracted a phenomenal mobility μ of $8600 \text{ cm}^2/\text{Vs}$, representing the highest value achieved in top-gated transistors at the time of their report. This approach to use aluminum nucleation layer for ALD was also adopted to IBM scientists to fabricate top-gated graphene devices to achieve field effect mobility about $2700 \text{ cm}^2/\text{Vs}$ [24], a respectable value, although not as high as the first report (Fig. 9).

The metal oxide as the buffer/nucleation layer has also been explored for the deposition of oxide on graphene using other approach such as molecular beam epitaxy (MBE). Wang et al. demonstrated that the growth of atomically smooth magnesium oxide (MgO) films on graphene surfaces by MBE [82]. By examining AFM images of MgO films with different growth rates on highly oriented pyrolytic graphite (HOPG) substrates, they find that the high

surface diffusion leads to nonuniform MgO films with root mean square roughness > 0.8 nm. To reduce the mobility of surface atoms, they deposit Ti atoms to dress the graphene surface prior to the MgO deposition. Remarkably, with as little as a 0.5 ML (monolayer) coverage of Ti, the root mean square roughness of a 1 nm MgO film is dramatically reduced to be near the atomic spacing in MgO (0.211 nm). Because the metallic Ti islands on graphene may be undesirable for lateral transport, they oxidize the Ti prior to MgO growth and find that the MgO layer is atomically smooth under this condition as well. However, the mobility of these devices is still limited, as low as $800\text{--}1700\text{ cm}^2/\text{V}\cdot\text{s}$.

The use of a thin metal (Al or Ti) film as a nucleation layer has enabled the ALD of continuous oxide dielectric (e.g. Al_2O_3) on graphene. The device results show mobility values of several thousand at room temperature, a finding which indicates that the top-gate stack does not severely increase the carrier scattering and consequently degrade the device characteristics.

3.4 Low-k polymer buffer layer for ALD dielectrics on graphene

Farmer et al. reported that the introduction of a low-k polymer buffer layer on graphene for ALD of high- κ dielectrics, and demonstrated top-gated devices without significant mobility degradation [14]. The low-k buffer layer consists of a commercially available polymer NFC 1400-3CP, which is a derivative of polyhydroxystyrene that is conventionally used as a planarizing underlayer in lithographic processes. It can be diluted in propylene glycol monomethyl ether acetate (PGMEA), and spin-coated onto the graphene surface. The dilution and spin speed can be adjusted to control the desired thickness and uniformity of the buffer layer. Methyl and hydroxyl groups contained within the polymer structure serve as functional groups for ALD of HfO_2 using tetrakis(dimethylamido)-hafnium and water as precursor. In a typical process, approximately 10 nm thick polymer buffer layer was first spin coated and cured at 175°C for 5 minutes to remove residual solvent, 10 nm thick HfO_2 is deposited onto the buffer layer to complete the dielectric stack. The ALD was conducted at a relatively low temperature of 125°C to produce HfO_2 films with a dielectric constant of $\kappa = 13$. Capacitance analysis of the complete gate stack yields a dielectric constant of $\kappa = 2.4$ for the buffer layer.

The impact the buffer dielectric processing on the transport properties of the back-gated graphene devices was examined by comparing two-point transfer characteristics (Fig. 10a) and transconductances (inset of Fig. 10a) at different stages of the processing. The two-point transconductance is defined as $g_m = dI_D/dV_G$, where I_D is the drain current and V_G is the gate voltage. The Dirac point voltage (V_{Dirac}) of the device before processing is $V_{\text{Dirac}} = 3.5$ V, in close proximity to 0 V, which signifies that the graphene is not significantly doped by the supporting 300 nm SiO_2 substrate. The doping level became highly p-doped after application of the buffer layer ($V_{\text{Dirac}} = 42.5$ V), and then moderately p-doped after HfO_2 ALD ($V_{\text{Dirac}} = 13.25$ V). After ALD, the device is subjected to an O_2 plasma treatment which further shift the device toward neutral doping ($V_{\text{Dirac}} = 5.75$ V), but did not damage the graphene as indicated by relative little change in resistance or transconductance. This also demonstrates that the dielectric stack can effectively protect graphene from damaging by the plasma that is known to etch graphene. Beyond changing the doping level, buffered dielectric processing has a minimal effect on the transfer characteristics. Both the minimum current value at V_{Dirac} and the maximum hole transconductance remain within 15% of their initial values. There is a 40% decrease in the maximum electron transconductance, which is likely associated with doping-induced conductance asymmetry caused by the electrodes [83,84]. The mobility values achieved here is $8500\text{ cm}^2/\text{Vs}$ for back gated configuration (with top-gate dielectrics) and $7600\text{ cm}^2/\text{Vs}$ for top-gate configuration. Overall, the results obtained using this buffer dielectric is a dramatic improvement compared to other methods of dielectric coating (Fig. 10b). Indeed, the authors have demonstrated in parallel

experiments that devices made with the polymer buffer layer are significantly better than those made with the other approaches, such as NO₂ functionalization and oxidized Al deposition discussed above.

The addition of a low- κ polymer buffer layer between graphene and conventional gate dielectrics helps minimize mobility degradation in top-gated graphene transistors. Possible reasons include the suppression of extrinsic surface phonons by the buffer layer and the reduction of the impurity concentration due to the inherent properties of the polymer. This new coating procedure represents a significant improvement over previous efforts, and will hopefully further the advancement of graphene transistors.

4. Physical assembly of high- κ oxide nanostructures as top-gate dielectrics for graphene transistors

Despite significant efforts devoted to the functionalization of graphene surface or introduction of buffer layer for ALD deposition of oxide dielectric on graphene, and significant advancements in this direction, these processes usually breaks the chemical bonds or introduces undesired impurities in the graphene lattice, inevitably leading to a significant degradation in device performance. Many of these processes can result in mobility degradation by nearly one order of magnitude. The use of aluminum buffer layer for high- κ deposition was demonstrated with improved device mobility, which, however, is still lower than that of normal back-gated graphene devices [4,45,49,85,86]. Introduction of a polymer buffer layer prior to high- κ deposition can mitigate the potential damage to graphene lattice, which however can limit the effective gate coupling due to the low- κ polymer layer. To eventually realize high-performance graphene-based electronics, continued effort is necessary to develop alternative approaches that can enable graphene-dielectric integration without damaging the pristine graphene lattice. To this end, we have recently reported an entirely new strategy to integrate graphene with high- κ dielectrics by physical assembling free-standing oxide nanowires or nanoribbons on top of graphene [87–89]. Here we review the recent advancements in this regard.

Nanowire and nanoribbons can be synthesized at high temperature with nearly perfect crystalline structure, but manipulated and assembled at room temperature. This flexibility allows the integration of normally incompatible materials and processes and can enable unique new functions in electronics or photonics [53,90–93]. Physical assembly of freestanding dielectric nanostructures on graphene represents the mildest approach for graphene-dielectric integration. Specifically, high quality dielectric nanostructures were first synthesized, and then transferred onto graphene as the gate dielectrics for top-gated graphene transistors. This integration approach preserves the pristine nature of the graphene and allows us to achieve the highest room temperature carrier mobility in top-gated graphene transistors to date. Fig. 11 illustrates our approach to fabricate top-gated graphene transistors using oxide nanostructures as the gate dielectrics. Oxide dielectric nanostructures (e.g. nanoribbons) were first aligned on top of the graphene through a physical dry transfer process, followed by lithography and metallization process to define the source and drain electrodes (Fig. 11a). Oxygen plasma etch was then used to remove the exposed graphene, leaving only the graphene protected underneath the dielectric nanostructure and the source drain electrodes (Fig. 11b). The top gate electrode was then fabricated to obtain a functional transistor (Fig. 11c).

4.1 Dielectric properties of Al₂O₃ nanoribbons

Aluminum oxide (Al₂O₃) nanoribbons were used as an initial example to demonstrate the concept of using free-standing chemical nanostructures as the top gate dielectrics for

graphene transistors [89], due to their excellent dielectric properties, thermal and chemical stability [94]. Al₂O₃ nanoribbons were synthesized through a physical vapour transport approach at 1200 °C [95]. Transmission electron microscope (TEM) studies show that the Al₂O₃ nanoribbons typically have a width of 1–3 microns, and a length on the order of 10 microns (Fig. 12a). Selected area electron diffraction (SAED) study shows the nanoribbon has a single crystalline α -Al₂O₃ structure, oriented along <110> direction in its long axis, and along <001> direction (c-plane) in its thickness (inset of Fig. 12a). The high resolution TEM image (HRTEM) confirms that the nanoribbon is a single crystal with nearly perfect crystalline structure free of any obvious defects (Fig. 12b). Atomic force microscopy (AFM) studies show the nanoribbons typically have a thickness around 15–150 nm (Fig. 12c), and nearly atomically smooth surface with root mean square roughness less than 0.2 nm (Fig. 12d).

The intrinsic dielectric properties (current tunnelling, breakdown and dielectric constant) of the Al₂O₃ nanoribbons were characterized using a metal-insulator-metal (MIM) device (Fig. 12e). Current-voltage (I-V) measurements of the MIM device show typical Fowler–Nordheim (F-N) tunnelling behaviour with a breakdown field of ~8.5 MV/cm (Fig. 12f and inset), comparable to the best quality ALD Al₂O₃ film [94]. This type of field assisted tunnelling can be described by charge carrier tunnelling through a triangular barrier with:

$$J = AE_{ox}^2 \exp(-B/E_{ox}) \quad (4)$$

where

$$A = 1.54 \times 10^{-6} \left\{ \frac{1}{m^* \Phi_B} \right\} \quad (5)$$

and

$$B = 6.83 \times 10^7 (m^*)^{1/2} (\Phi_B)^{3/2} \quad (6)$$

J is current density, E_{ox} is the oxide electric field, m^* is the effective mass of the charge carrier, which is about 0.23 m_e , and Φ_B is the barrier height [94]. Fitting the I-V characteristics with F-N tunnelling model gives a tunnel barrier of about 2.0 eV between Al₂O₃ and Ti, comparable to previous reports of the barrier height between ALD Al₂O₃ and metals of similar work function [94,96]. The relative dielectric constant is also determined as 8.5 from capacitance-voltage measurement, which is larger than typical values observed in ALD Al₂O₃ films. These studies clearly demonstrate that the Al₂O₃ nanoribbons have dielectric properties comparable to or better than the best quality ALD Al₂O₃ film, and can function as an excellent dielectric material for top-gated graphene transistors.

4.2 Dielectric nanostructure-graphene integration and interface

The Al₂O₃ nanoribbons can be aligned onto the top of the graphene through a solution assembly or physical transfer process. Previous studies have shown that the deposition of oxide on top of graphene often introduces significant defects into the graphene structure with an obvious defect band (D-band) emerging around 1350 cm⁻¹ in Raman spectra [62]. To this end, micro-Raman spectroscopy was employed to investigate the interaction between an Al₂O₃ nanoribbon and the underlying graphene (Fig. 13a). Micro-Raman spectra were

collected from bare graphene (point a) and Al₂O₃ nanoribbon covered graphene (point b). Significantly, there is no clear difference between two Raman spectra and there is no obvious D-band (Fig. 13b), in contrast to previous study in which an obvious D-band was observed [109]. Cross-sectional TEM was used to study the graphene-dielectric interface (Fig. 13c). The image of the device shows that the graphene layers are intimately integrated with the crystalline Al₂O₃ nanoribbon without any obvious gap or impurities between them (Fig. 13d). Together, these studies clearly demonstrate that the physical assembly approach can effectively integrate Al₂O₃ nanoribbon with graphene without introducing any appreciable defects into the graphene lattice, and thus can effectively preserve the high carrier mobility in the resulting devices.

4.3 Al₂O₃ nanoribbons as the top-gate dielectrics for graphene transistors

The electrical transport studies of the top-gated graphene transistors using Al₂O₃ nanoribbon gate dielectrics were carried out at room temperature. Fig. 14a shows the drain-source current (I_{ds}) versus drain-source voltage (V_{ds}) output characteristics of the transistor at various top-gate voltages (V_{TG}). The device delivers an on-current of 675 μ A at $V_{ds} = 1$ V and $V_g = -1.5$ V. Importantly, the transfer characteristics (I_{ds} versus top-gated voltage (V_{TG}) and back-gated voltage (V_{BG})) shows the required gate voltage swing to achieve similar current modulation in top-gate configuration is more than one order of magnitude smaller than that in back-gate configuration (Fig. 14b dI_{ds} and inset). The transconductance

$g_m = \frac{dI_{ds}}{dV_{TG}}$ can be extracted from the I_{ds} - V_{TG} curve dV_{TG} (Fig. 14c). At $V_{ds} = 1$ V, the top-gated device exhibits a max g_m of about 290 μ S, which is about 15 times larger than that of the back-gated configuration ($g_m \sim 19.5$ μ S).

Fig. 15a further shows two-dimensional plot of the device conductance as a function of varying V_{BG} and V_{TG} bias, from which we can determine the top-gate Dirac point (V_{TG_Dirac}) shift as a function of V_{BG} (Fig. 15b). It gives the ratio between top-gate and back-gate capacitances, $C_{TG}/C_{BG} \approx 14.3$. This gate capacitance ratio is consistent with the improvement factor (~ 15) in transconductance of top- versus back-gated configurations. Using the back-gate capacitance value of $C_{BG} = 11.5$ nF/cm², the top-gate capacitance is estimated to be $C_{TG} = 164.5$ nF/cm², corresponding to a relative dielectric constant of 8.4 for Al₂O₃ nanoribbon, which is also consistent with the value obtained from MIM devices.

We have used the same model described above [section 3.3] to fit the measured data and extract the relevant parameters, n_0 , $R_{contact}$ and μ . Fig. 15c shows the measured R_{tot} versus V_{TG} (black line), along with the fitted curve derived from Eq. (3) (red line). The fitted curve agrees well with the experimental data, with a single value of the residual concentration $n_0 = 4.1 \times 10^{11}$ cm⁻², $R_{contact} = 1240$ Ω , and the mobility = 22,400 cm²/V.s, which represents the highest carrier mobility value observed in top-gated graphene devices to date. Multiple devices were fabricated and tested with the same approach, all of which exhibited carrier mobilities well exceeding 10,000 cm²/V.s with highest mobility of reach 23,600 cm²/V.s, comparable to the best reported values in back-gated devices and significantly better than typical values previously reported for top-gated devices (Fig. 16). Together, these studies clearly demonstrate that the presence of Al₂O₃ nanoribbon on top of graphene does not lead to any mobility degradation, in contrast to previous efforts in using ALD or PVD to deposit dielectrics on graphene.

4.4 ZrO₂ nanowire as top-gate dielectric for graphene nanoribbon transistors

Taking a step further, ZrO₂ nanowires with even higher dielectric constant (up to 23) [97,98] were also explored as the gate dielectric for top-gated devices [88]. An additional attribute of using ZrO₂ nanowires is that narrower graphene channels (e.g. graphene nanoribbons,

GNR) can be readily fabricated to facilitate gap-opening and improve the transistor on-off ratio [30–33,35,99]. ZrO₂ nanowires were synthesized through a chemical vapour deposition (CVD) process using ZrCl₄ as the precursor. Scanning electron microscope (SEM) image shows that ZrO₂ nanowires are about several tens of microns in length and 20–100 nm in diameter (Fig. 17a). TEM and SAED studies reveal that ZrO₂ nanowires are amorphous (Fig. 17b and inset). The top-gated graphene transistors using ZrO₂ nanowires as the gate dielectric can be fabricated using the same approach described above (Fig. 17c). Here the ZrO₂ nanowire also functions as a nanoscale etch mask to define a narrow graphene nanoribbon with width in the 10–20 nm regime through aggressive over etch (inset, Fig. 17c) [35]. The I_{ds} - V_{ds} plots at various top-gate voltages (V_{TG}) show clearly that the device conductance decreases as the gate potential increases towards positive direction (Fig. 17d), demonstrating that the graphene nanoribbon is p-type doped, which can be attributed to edge oxidation or the physisorbed O₂ from ambient or during the device fabrication process. This device delivers an on-current of 28 μ A at $V_{ds} = 1$ V and $V_g = -1.0$ V. Transfer characteristics show a top-gated GNR transistor using ZrO₂ nanowire dielectric can be switched on and off with only ~ 1 volt of gate swing (red curve in Fig. 17e), in contrast to 10–40 V required for back-gated devices (black curve in Fig. 17e). The device shows a room temperature on/off ratio of ~ 12 at $V_{ds} = 0.1$ V, consistent with a graphene nanoribbon with estimated width of ~ 10 – 15 nm [30,35]. The maximum transconductance g_m at $V_{ds} = 1$ V is about 29 μ S, more than 12 times larger than that of the back-gated configuration (~ 2.3 μ S) (Fig. 17f).

It is interesting to compare the top-gated graphene nanoribbon devices with state-of-the-art silicon MOSFETs. The effective *on* current I_{on} for an FET device is usually characterized at $V_{ds} = V_{g(on-off)} = V_{dd}$, where $V_{g(on-off)}$ is the gate voltage swing from off- to on-state and V_{dd} is the power supply voltage. Considering $V_{ds} = V_{g(on-off)} = V_{dd} = 1$ V, the I_{on} of our device at $V_{ds} = 1$ V and 1 V gate swing from the off state is ~ 25 μ A. Taking the channel width of the graphene nanoribbons ~ 15 nm, we obtain the scaled values of I_{on} and g_m of our device to be ~ 1.7 mA μ m⁻¹ and ~ 2.0 mS μ m⁻¹, already exceeding the values of 0.7 mA μ m⁻¹ and 0.8 mS μ m⁻¹ in sub-100-nm silicon p-MOSFETs and comparable to those of n-MOSFET devices employing high- κ dielectrics.[100]. This is significant considering the relatively large channel length (~ 1 μ m) of the current device. It is reasonable to expect that the on-current and transconductance can be further improved to by shrinking the channel length. These studies demonstrate that ZrO₂ nanowires can also function as effective gate dielectrics for high performance top-gated graphene nanoribbon devices.

4.5. Conductor/dielectric coreshell nanowires as the top-gate for graphene nanoribbon transistors

In the above discussions, pure dielectric nanostructures are explored as the top-gate dielectric for graphene transistors, in which the dielectric thickness is controlled by the overall dimension of the nanostructures and may be difficult to scale down to very small thickness (e.g. 1–2 nm), due to the challenges to synthesize and assemble the oxide nanostructures at such small dimensions, and the potential difficulties to fabricate devices using such small structures. Alternatively, one can also explore conductor/dielectric coreshell nanostructures (nanowires or nanoribbons), in which the dielectrics are deposited on a conducting (e.g. metal or highly doped semiconductor) nanostructure using ALD, and can be precisely controlled down to 1 nm regime. Such coreshell nanowires can be used to fabricate top-gated graphene transistors using a similar approach described above, in which the oxide shell functions as the gate dielectrics with controlled thickness, and the conducting core functions as the self-integrated gate. Using such coreshell nanostructures, it is possible to fabricate top-gated graphene transistors with the dielectric thickness down to 1 nm or so (Fig. 18a-h). To establish the electrical contact between the silicon nanowire gate and the

external gate electrode, an additional step of argon plasma treatment is needed to physically remove the HfO_2 film on the top half of the nanowires prior to the deposition of the top gate electrode.

Various type of conducting nanowires (highly doped silicon or metal silicide, NiSi , PtSi) can be explored for this purpose. For example, we have recently synthesized Si/HfO_2 coreshell nanowires by ALD deposition of 2 nm thick HfO_2 on highly-doped silicon nanowires (Fig. 19b and c) [87]. Such coreshell nanowires can be readily explored for top-gated graphene nanoribbon transistors. Here the HfO_2 shell functions as the gate dielectrics with controlled thickness down to 1 nm, and the silicon core functions as the self-integrated gate. To contact the silicon core gate to external electrode, the top-half of the HfO_2 shell was etched away using argon plasma. The cross section TEM image clearly shows the integrated silicon gate, 2-nm thick HfO_2 gate dielectric, and the graphene nanoribbon (Fig. 20b and c).

Electrical transport studies of the top-gated device were carried out in ambient conditions at room temperature. The gate tunnelling leakage current (I_{gs}) from the Si/HfO_2 core/shell nanowire to the underlying GNR is negligible within the gate voltage range of ± 1 V range (Fig. 21a). This measurement demonstrates that the 2 nm thick HfO_2 dielectrics can function as an effective gate insulator for top-gated GNR transistors and afford high gate capacitance critical to the high transconductance. The drain-source current (I_{ds}) vs. drain-source voltage (V_{ds}) plots at various top-gate voltages (V_{TG}) show clearly that the device conductance decreases as the gate potential increases towards positive direction (Fig. 21b), demonstrating that the GNR is *p*-type doped, which can be attributed to edge oxidation or the physisorbed O_2 from ambient or during the device fabrication process. Fig. 21c shows the transfer characteristics drain-source current (I_{ds}) versus top-gated voltage (V_{TG}) curves for the same device at $V_{ds} = 0.1$ and 1.0 V. The transfer characteristics show the device can be switched on and off with < 1 volt of gate swing, the smallest on-off gate swing ever achieved in GNR transistors. The device delivers an on-current of 27 μA at $V_{ds} = 1$ V and $V_g = -1.0$ V, and shows a room temperature on/off ratio of ~ 70 at $V_{ds} = 0.1$ V, consistent with a GNR with estimated width of ~ 10 nm.^{9–11} To evaluate the top-gated devices versus standard back-gated devices, we have measured the transfer characteristics, I_{ds} - V_{TG} and back-gated voltage (V_{BG}). Significantly, the required gate voltage swing to achieve a similar current modulation in top-gate configuration is more than one order of magnitude smaller than that in back-gate

configuration (Fig. 21d). The transconductance $g_m = \frac{dI_{ds}}{dV_g}$ can be extracted from the I_{ds} - V_{TG} curve. The maximum g_m in the top-gated device at $V_{ds} = 1$ V is about 32 μS (Fig. 21e), nearly 20 times larger than the value obtained in the back-gated configuration (~ 1.7 μS) (inset, Fig. 21e).

4.6. Integrated device array from nanowire gated graphene nanoribbon transistors

The ability to fabricate the top-gated graphene nanoribbon devices readily allows integration of multiple GNR FETs into functional device arrays. (Fig. 22a and b), and therefore allowing for diverse electronic functions. For example, a logic OR gate is obtained with two independent gate electrodes fabricated on a GNR in conjunction with a loading resistor (Fig. 22c). The OR function occurs because the output voltage is low only when input to both gates is at low voltages (Fig. 22d). When one or both gates are at high voltages, the GNR channel is electrically shut off, resulting in a high output voltage.

5. Summary

Graphene is emerging as an interesting electronic material for future electronics due to their exceptionally high carrier mobility, tunable band gap and atomically thin structure. The gate

dielectric is an essential component of a transistor and can significantly impact the critical device parameters including transconductance, subthreshold swing and frequency response. Exploring graphene for future electronics requires its effective integration with high quality gate dielectrics, in particular the high-k dielectrics, which is of significant challenge due to the intrinsic incompatibility between pristine graphene and oxide dielectrics. Physical vapour deposition (PVD) such as electron-beam evaporation or sputtering process has been used to deposit dielectrics, although the PVD process usually yields lower quality dielectrics and can cause significant damages to graphene. The deposition of high-k dielectrics using ALD requires reactive surface groups. Functionalization of graphene surface for ALD either introduces undesired impurities or breaks the chemical bonds in the graphene lattice, inevitably leading to a significant degradation in carrier mobilities. As a result, the mobility values observed in the top-gated devices are typically nearly one order of magnitude smaller than what can be achieved in the back-gated devices. Recently, the introducing of polymer or aluminum buffer layer for high-k deposition was demonstrated with improved the device mobility, which, however, is still lower than best values observed in back-gated graphene devices. A newly developed physical assembly approach to integrate graphene with free-standing dielectric nanostructures can minimize potential damage to graphene lattice, and have enabled the highest mobility top-gated graphene transistors ever. This method opens a new avenue to integrate high-k dielectrics on graphene with the preservation of high carrier mobility. With further optimization of dielectric nanostructure growth and assembly process to precisely control their physical dimension and spatial location, large arrays of top-gated graphene transistors or circuits can be envisioned. This physical assembly and integration approach can thus open a new avenue to high performance graphene electronics, which can impact significantly high speed high frequency circuits and enable an entirely new generation of flexible, wearable or disposable electronics for computing, storage and wireless communication.

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Fig. 1.

Graphene as a potential electronic material. (a) Schematic illustration of graphene as an atomic-scale honeycomb lattice of carbon atoms. (b) TEM image of graphene, adapted from [2]. (c) Image of radio frequency devices fabricated on a 2-inch graphene wafer and schematic cross-sectional view of a top-gated graphene FET. (d) Measured small-signal current gain $|h_{21}|$ as a function of frequency f for a 240-nm-gate and a 550-nm-gate graphene FET at $V_D = 2.5$ V. Cutoff frequencies, f_T , were 53 and 100 GHz for the 550-nm and 240-nm devices, respectively. Adapted from [25].

Fig. 2.

Graphene nanostructures for the opening of a conduction gap in graphene.. (a) Schematic view of a graphene nanoribbon and transfer characteristics of a graphene nanoribbon transistor with on/off ratio >100. (c) Schematic view of a graphene nanomesh and transfer characteristics of a graphene nanoribbon transistor with on/off ratio >100. Adapted from [34] and [35].

Fig. 3. Raman spectra of the graphene show a clear defect band emerging at 1350 cm⁻¹ after PVD dielectric deposition using various approaches, suggesting significant defects are introduced into graphene lattice during the dielectric deposition process. Adapted from [62].

Fig. 4. (a) SEM image of a graphene transistor with PVD top-gate dielectrics. (b) Back-gate transfer characteristics of Graphene-FET with and without a top gate. Adapted from [58].

Fig. 5.

ALD of Al₂O₃ on pristine graphene. (a) AFM image of graphene on SiO₂ before ALD. The height of the triangular shaped graphene is ~1.7 nm as shown in the height profile along the dashed line cut. Scale bar is 200 nm. (b) AFM image of the same area as (a) after ~2 nm Al₂O₃ ALD deposition. The height of the triangular shaped graphene becomes ~0.3 nm as shown in the height profile along the dashed line cut. Scale bar is 200 nm. (c) and (d) Schematics of graphene on SiO₂ before and after ALD. The Al₂O₃ grows preferentially on graphene edge and defect sites. Adapted from [73].

Fig. 6.

(a) (False color) scanning electron microscopy image of the graphene channel and contacts. The inset shows the optical image of the as-deposited graphene flake (circled area) prior to the formation of electrodes. (b) Schematic cross section of the graphene transistor. Note that the device consists of two parallel channels controlled by a single gate in order to increase the drive current and device transconductance. (c) Measured conductance as a function of back-gate voltage, V_{BG} , of the graphene transistor before depositing the top-gate dielectric. The inset shows the same device after the deposition of Al_2O_3 by ALD. The two arrows represent the sweeping direction of the gate voltage. Adapted from [27].

Fig. 7.

ALD of Al₂O₃ on PTCA-coated graphene. (a) Schematic illustration of perylene tetracarboxylic acid (PTCA)-coated graphene. PTCA selectively adheres to graphene on SiO₂ surfaces, providing binding sites for TMA deposition. Inset is a top view of PTCA structure. (b) AFM image of graphene on SiO₂ before ALD. The height of the triangular shaped graphene is ~1.6 nm as shown in the height profile along the dashed line cut. Scale bar is 500 nm. (c) AFM image of the same area as (a) after ~2 nm Al₂O₃ ALD deposition. The height of the triangular shaped graphene becomes ~3.0 nm as shown in the height profile along the dashed line cut. Scale bar is 500 nm. (d) and (e) Schematics of graphene on SiO₂ before and after ALD. The Al₂O₃ grows uniformly on noncovalently PTCA-coated graphene. Adapted from [73]

Fig. 8.

(a) Schematic of dual-gated graphene FET structure. (b) Optical microscope image of a graphene FET. (c) R_{tot} vs. V_{TG} data measured at different V_{BG} values. The inset shows the position of $V_{\text{Dirac,TG}}$ at different V_{BG} . Optical microscope image of a graphene FET. Adapted from [77].

Fig. 9.

(a) Device schematic of the dual-gate graphene transistor. (b) SEM image of a double-channel graphene transistor. The channel width is 27 μm, and the gate length is 350 nm for each channel. (c) Measured channel conductance as a function of the back-gate voltage of a graphene device before and after the deposition of 12-nm-thick ALD Al_2O_3 . Prior to the ALD process, a layer of 2-nm aluminum is deposited and oxidized as the nucleation layer. Adapted from [24].

Fig. 10.

Two-point back-gated measurements of graphene flakes. (a) Transfer characteristics and corresponding transconductances (inset) after the different stages of buffered dielectric processing: before processing (gray), after NFC polymer deposition (green), after HfO_2 deposition (blue), and after 50 W O_2 plasma treatments for 30 s (red). The schematic shows the completed device configuration. (b) Transfer characteristics of two devices before (solid lines) and after (dashed lines) alternative coating processes are employed. Two nanometers oxidized Al deposition (red) and NO_2 functionalization (blue) is used instead of polymer coating. Both processes result in significant mobility degradation. $V_D = 10$ mV for all measurements, and V_{BG} is swept forward and backward to show current hysteresis. Adapted from [14].

Fig. 11.

Schematic illustration of the fabrication process to obtain top-gated graphene transistors using dielectric oxide nanostructures (e.g. nanoribbons) as the etching mask and top-gate dielectric. (a) A dielectric nanostructure is aligned on top of graphene using a dry-transfer process without any additional chemical functionalization to minimize the possibility to introduce defects/impurities into the graphene-dielectric interface, and the source-drain electrodes are fabricated by electron-beam lithography. (b) Oxygen plasma etch is used to remove the unprotected graphene, leaving only the graphene underneath the dielectric nanostructure connected to two large graphene blocks underneath the source and drain electrodes. (c) The top gate electrode is defined through lithography and metallization process. Adapted from [89].

Fig. 12.

Evaluation of the Al_2O_3 nanoribbons as dielectric material. (a) TEM image (inset, SAED pattern) and (b) HRTEM image of an Al_2O_3 nanoribbon show nearly perfect crystalline structure with $\alpha\text{-Al}_2\text{O}_3$ structure. (c) AFM image of an Al_2O_3 nanoribbon with thickness ~ 50 nm. The image area is $5\ \mu\text{m} \times 5\ \mu\text{m}$. (d) AFM image of the surface of the Al_2O_3 nanoribbon, highlighting the smooth surface with a root mean square roughness < 0.2 nm. The image area is $250\ \text{nm} \times 250\ \text{nm}$. (e) The schematic device diagram (inset) and SEM image of an Al_2O_3 nanoribbon metal-insulator-metal (MIM) device. (f) Current density-electric field (J-E) curve of an MIM device made from an Al_2O_3 nanoribbon, and the inset shows the corresponding Fowler–Nordheim (F-N) curve. Adapted from [89].

Fig. 13.

Characterization of the graphene/Al₂O₃ nanoribbon interface. (a) An optical image of an Al₂O₃ nanoribbon on graphene, the scale bar is 2 μm. (b) Raman spectra of the graphene with (b) and without (a) Al₂O₃ nanoribbon covering. There is no D-band in either spectrum, indicating that Al₂O₃ nanoribbon does not introduce any appreciable defects into graphene lattice. (c) A cross-section TEM image of the top gate stack, the scale bar is 100 nm. The inset shows an SEM image of a typical device, the scale bar indicates 5 μm. The dotted line in the inset shows the cross-section cutting direction. (d) A cross-section HRTEM image of the interface between Al₂O₃ nanoribbon and a tri-layer graphene. The partially incomplete graphene layers in the image are caused by electron beam damage during the TEM imaging process. Adapted from [89].

Fig. 14.

Room temperature electrical properties of the top-gated graphene device using Al_2O_3 nanoribbon as the gate dielectric. (a) $I_{\text{ds}}\text{-}V_{\text{ds}}$ output characteristics, the channel width and length of the device is $2.1\mu\text{m}$ and $4.1\mu\text{m}$ (b) Transfer characteristics at $V_{\text{ds}} = 1\text{ V}$ for the device using top and back gate (inset). (c) Transconductance g_{m} as a function of top-gate voltage V_{TG} , the inset shows the g_{m} vs. V_{BG} . The plots indicate the top-gate g_{m} is about 15 times higher than the back-gate g_{m} . Adapted from [89].

Fig. 15.

Mobility determination in the top-gated graphene device using Al_2O_3 nanoribbon as the gate dielectric. (a) Two-dimensional plot of the device conductance at varying V_{BG} and V_{TG} bias. The unit in the color scale is μS . (b) The top-gate Dirac point V_{TG_Dirac} at different V_{BG} . (c) Experimental plot (black line) and modelling fitting (red line) of R_{tot} vs. $V_{TG} - V_{TG_Dirac}$ relation to derive the contact resistance and carrier mobility. Adapted from [89].

Top-gate dielectric deposition approach	Maximum mobility
SiO ₂ film by e-beam evaporation [56]	710 cm ² /Vs
Al ₂ O ₃ by ALD after NO ₂ functionalization [27]	400 cm ² /Vs
HfO ₂ deposition by direct ALD [23]	1240 cm ² /Vs
Al ₂ O ₃ deposition by ALD with Al buffer layer [24] and [77]	8000 cm ² /Vs
Al ₂ O ₃ deposition by ALD with low-k polymer buffer layer [14]	7400 cm ² /Vs
Al ₂ O ₃ single crystal nanoribbon [86]	23600 cm ² /Vs

Fig. 16.

Table summarizing highest mobility values obtained in top-gated graphene transistors using various dielectric integration approaches.

Fig. 17.

ZrO₂ NWs as the gate dielectric in top-gated GNR transistors. (a) An SEM image of ZrO₂ nanowires. (b) A TEM image of a ZrO₂ nanowire, and the inset shows the SAED pattern of a ZrO₂ nanowire. (c) The SEM image of a top-gated GNR transistor with ZrO₂ nanowire as top-gate dielectric. The gate length is about 500 nm and the diameter of the nanowire is 50 nm. Inset shows an AFM image of a ~15 nm wide GNR obtained under ZrO₂ nanowire after oxygen plasma etching. The scale bar indicates 200 nm. (d) I_{ds} - V_{ds} output characteristics at variable top gate voltage starting from 0.4 V at bottom to -1.0 V at top in the step of -0.2 V. (e) I_{ds} - V_{TG} (red curve) and I_{ds} - V_{BG} (black curve) transfer characteristics at $V_{ds} = 1$ V. (f) Transconductance g_m as a function of top-gate voltage V_{TG} and back gate voltage V_{BG} (inset). Adapted from [88].

Fig. 18.

Schematic illustration of the fabrication process to obtain top-gated graphene transistors using Si/HfO₂ coreshell nanowires as the etching mask and top-gate. (a) and (e), an Si/HfO₂ coreshell nanowire is aligned on top of graphene using a dry-transfer process, and the source-drain electrodes are fabricated by electron-beam lithography (b) and (f), Oxygen plasma etch is used to remove the unprotected graphene, leaving only the GNR underneath the nanowire connected to two large graphene blocks underneath the source and drain electrodes. (c) and (g), The top-half of the HfO₂ shell was etched away using argon plasma to expose the silicon core gate for contact to external electrode. (d) and (h), The top gate electrode is defined through lithography and metallization process. Adapted from [87].

Fig. 19.

TEM characterization of Si/HfO₂ coreshell nanowires. (a) Schematic illustration of the synthesis of Si/HfO₂ coreshell nanowires. Highly doped p-type silicon nanowire arrays were synthesized using catalytic chemical vapour deposition. Atomic layer deposition was used to grow HfO₂ shell with controlled thickness. (b) TEM and (c) HRTEM images of Si/HfO₂ coreshell nanowires. Adapted from [87].

Fig. 20.

Characterization of the graphene/HfO₂ interface. (a) A SEM image of a typical device. (b) A cross-section TEM image of the top gate stack. (c) A cross-section HRTEM image of the interface between nanowires and a multi-layers graphene, which indicate that the graphene layers are intimately integrated with the Si/HfO₂ nanowire without any obvious gap or impurities between them. A TEM image of multi-layer graphene device is shown here because it is very difficult to visualize the mono- or few-layer of graphene nanoribbon under the nanowire due to significant electron-beam damage while conducting TEM studies. Adapted from [87].

Fig. 21.

Room temperature electrical properties of the top-gated GNR device by using Si/HfO₂ coreshell as the top-gate. (a) Gate leakage current versus top-gate voltage. The leakage current is negligible (at the nA level) within ± 1 V range. (b) I_{ds} - V_{ds} output characteristics at variable top-gate voltage starting from 0.6 V at bottom to -1.0 V at top in the step of -0.2 V. (c) The transfer characteristics I_{ds} - V_{TG} at $V_{ds} = 0.10$ and 1.0 V. (d) I_{ds} - V_{TG} and I_{ds} - V_{BG} transfer characteristics at $V_{ds} = 1$ V. (e) Transconductance as a function of top-gate voltage V_{TG} and back gate voltage V_{BG} (inset). (f) Two-dimensional plot of the device conductance at varying V_{BG} and V_{TG} bias, the unit in the color scale is μS . Adapted from [87].

Fig. 22.

Independently addressable GNR device array. (a) An SEM image of two independently addressable top-gated GNR FETs. (b) Transfer characteristics of two top-gated GNR FETs at $V_{ds} = 0.1$ V. (c) The SEM image of a logic OR gates built from GNR transistors. The inset shows the schematic circuit diagram. (d) The OR gate output characteristics with double top-gates. The operating voltage is $V_{dd} = 1$ V. The inputs for the two gates, A and B, are 1 V for state 1 and 0 for state 0. Adapted from [88].