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High Performance Top-Gated Graphene Nanoribbon Transistors Using Zirconium Oxide Nanowires as High-k Gate Dielectrics

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Graphene has attracted a great deal of interest in the past several years.[1–5] New physics has been predicted and observed, such as ultrahigh carrier mobility,[6] electron-hole symmetry and quantum hall effect,[2,4,7–9] and the strong suppression of weak localization.[10–12] For mainstream logic application, graphene nanoribbons (GNRs), as thin strips of graphene or unrolled carbon nanotubes, are predicted to be semiconducting due to edge effects and quantum confinement.[13–15] Recent experimental studies have also demonstrated that GNRs can effectively function as a semiconducting channel for room-temperature field-effect transistors.[16–22] By varying the width of GNRs at selected points, it is also possible to create graphene quantum dots within a GNR for single electron transistors.[23] These studies represent important advances in GNR based electronics. However, most of the efforts to date employ a silicon substrate as a global back gate and silicon oxide as the gate dielectrics. While such a device has led to many interesting scientific discoveries, it will be of limited use for practical applications due to the high gate switching voltage required and the inability to independently address multiple units on the

same chip.[17,20,21] Top-gated devices with high- k dielectrics can significantly reduce the required switching voltage and allow independently addressable device arrays and functional circuits, and therefore are of significant interest.

The insulating gate dielectric is an essential component of a transistor, which can significantly impact the critical device parameters including transconductance, subthreshold swing and frequency response. High- k dielectrics have been actively pursued to replace SiO₂ gate insulator for silicon devices in the deep nanometer regime.[24] High- k gate insulators can afford high capacitance without relying on ultrathin film thickness, thus can greatly reduce the required gate switching voltage and suppress direct-tunnelling leakage current from the gate. Significant efforts have been directed to the integration of high- k dielectric materials, e.g., zirconium oxide (ZrO₂) or hafnium oxide (HfO₂), with active semiconductor materials (e.g., silicon, semiconductor nanowires or carbon nanotubes) and have enabled devices of extraordinary performance.[25]

Exploring graphene for future electronics requires effective integration of high quality gate dielectrics, in particular the high- k dielectrics. However, it has been rather challenging to deposit oxide dielectrics onto graphene without introducing defects into a monolayer of carbon lattice.[26–28] The deposition of high- k dielectrics is usually achieved using atomic layer deposition (ALD), which requires reactive surface groups. Functionalization of graphene surface for ALD either introduces undesired impurities or breaks the chemical bonds in the graphene lattice, inevitably leading to a significant degradation in carrier mobilities.[29,30] Therefore, to develop an approach that can deposit high-quality high- k dielectrics without damaging the surface bonds of pristine graphene lattice remains a critical challenge towards high-performance, graphene-based electronics.

Here we describe an entirely new method for integrating GNRs with high- k dielectrics by first synthesizing high- k ZrO₂ nanowires at high temperature, and then transferring them onto graphene through a dry transfer process at room temperature. This physical assembly approach can allow flexible integration of distinct materials that are normally not compatible due to material or process incompatibility, and has been used to combine variable nanostructures to enable unique new functions that are not normally possible.[31–33] Exploiting this approach for graphene dielectric integration preserves the integrity of the graphene lattice and affords top-gated GNR devices with unprecedented transconductance of 2.0 mS μm^{-1} , and carrier mobility of $\sim 1300 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$. Furthermore, multiple independent addressable top-gated GNR transistor arrays can be readily achieved to allow functional circuits.

Figure 1 illustrates our approach to fabricate top-gated GNR transistors using dielectric nanowires as the high- k gate insulator. Mechanically peeled graphene flakes on silicon substrate were used as the starting materials in our initial studies. Dielectric nanowires were aligned on top of the graphene through a physical dry transfer process, followed by an e-beam lithography and metallization process to define the source and drain electrodes (Fig. 1a). Oxygen plasma etching was then used to remove the exposed graphene, leaving only the graphene protected by the dielectric nanowire and the source drain electrodes (Fig. 1b). An additional attribute of using nanowire dielectric is that narrow graphene channels (e.g., GNR) can be automatically defined by the nanowire mask during the oxygen plasma etching process. The top gate electrode was lastly fabricated on top of the dielectric nanowire (Fig. 1c). A typical GNR device consists of source, drain, and top gate electrodes (Ti/Au, 50 nm/50 nm), ZrO₂ nanowire as the top-gate dielectric, a highly doped p-type silicon substrate ($<0.004 \text{ ohm}\cdot\text{cm}$) as the back gate, and a 300-nm thermal silicon oxide layer as the back-gate dielectric.

Zirconium oxide (ZrO_2) is an excellent high- k dielectric material with multiple desirable characteristics, including a high dielectric constant (~ 23), a wide band gap (5.1 – 7.8 eV) and good thermal stability.[34,35] ZrO_2 nanowires were grown at 1000 °C through a chemical vapour deposition process in a tube furnace with ZrCl_4 powders as the precursor. Scanning electron microscopy (SEM) image shows that ZrO_2 nanowires are about several tens of microns in length and 40–100 nm in diameter (Fig. 2a). TEM and SAED studies reveal that ZrO_2 nanowires are amorphous (Fig. 2b and inset). Energy dispersive x-ray (EDX) analysis of the nanowires shows only zirconium and oxygen signals, suggesting high purity for the ZrO_2 nanowires (Fig. 2c).

In our fabrication, the ZrO_2 nanowire functions as a nanoscale etch mask to define a narrow GNR with width in the 10–20 nm regime through aggressive over etching (inset, Fig. 2d) as well as top-gated dielectrics for the GNR transistor (Fig. 2d). Electrical transport studies of the top-gated device were carried out under an ambient condition at room temperature. Before starting transistor characterization, we first tested the gate leakage across the ZrO_2 dielectric nanowire. Importantly, the tunnelling leakage current between the gate and GNR channel was negligible in the gate voltages range of $\pm 2\text{V}$ (Fig. 2e). This measurement demonstrates that the ZrO_2 dielectric nanowire can function as an effective gate insulator for top-gated GNR transistors.

The drain-source current (I_{ds}) versus drain-source voltage (V_{ds}) plot at various top-gate voltages (V_{TG}) shows the GNR transistor output characteristics (Fig. 2f). The device conductance decreased as the gate potential increased towards positive direction and increased as the gate potential increased towards negative direction, suggesting that the GNR was p-doped, which can be attributed to edge oxidation or the physisorbed O_2 from ambient or during the device fabrication process. The output characteristics shows that device can deliver an on-current of 28 μA at $V_{ds} = 1\text{ V}$ and $V_g = -1.0\text{ V}$ (Fig. 2f).

Figure 2g shows the transfer characteristics drain-source current I_{ds} versus top-gated voltage V_{TG} curves for the same device at different drain source voltages. The device shows a room temperature on/off ratio of ~ 12 at $V_{ds} = 0.1\text{ V}$, consistent with a GNR with an estimated width of $\sim 15\text{ nm}$. [18, 20] To evaluate the top-gated devices versus standard back-gated devices, we also measured the transfer characteristics in both the top-gated configuration (I_{ds} - V_{TG}) and back-gated configuration (I_{ds} - V_{BG}) (Fig. 2h). Significantly, the gate voltage swing required to achieve a similar current modulation in top-gate configuration is more than one order of magnitude smaller than that in back-gate configuration. Transfer characteristics show a top-gated GNR transistor using ZrO_2 nanowire dielectric can be switched on and off with only ~ 1 volt of gate swing (red curve in Fig. 2h), in contrast to 10–40 V required for the back-gated configuration (black curve in Fig. 2h). [18, 20] The

transconductance $g_m = \frac{dI_{ds}}{dV_g}$ of the device can be extracted from the I_{ds} - V_{TG} curve. The g_m at $V_{ds} = 1\text{ V}$ is about 29 μS in the top-gated configuration (Fig. 2i), more than 12 times larger than that of the back-gated configuration ($\sim 2.3\text{ }\mu\text{S}$, see the inset in Fig. 2i).

To further understand the device performance, it is important to determine the gate capacitance, which is not straightforward due to the complex geometry. To this end, we have employed three-dimensional finite element method to calculate the capacitance of the device, which yields an electrostatic capacitance (C_e) of 1170 nF/cm^2 for a 15-nm ribbon under a 50-nm ZrO_2 nanowire. Taking the top-gate capacitance (C_{top}) as being the serial combination of the electrostatic capacitance (C_e) and the quantum capacitance (C_q), we can obtain $C_{top} = C_q C_e / (C_e + C_q) = 738\text{ nF}/\text{cm}^2$ assuming $C_q = \sim 2000\text{ nF}/\text{cm}^2$. Based on standard

transistor model, we calculated the hole mobility $\mu = \frac{g_m L}{C_{top} V_{ds} W} \sim 1310 \text{ cm}^2/\text{Vs}$, the highest value obtained in GNR devices.[17]

It is important to compare the top-gated GNR devices with the state-of-the-art silicon MOSFETs. The effective *on* current I_{on} for an FET device is usually characterized at $V_{ds} = V_{g(on-off)} = V_{dd}$, where $V_{g(on-off)}$ is the gate voltage swing from off-to on-state and V_{dd} is the power supply voltage. Considering $V_{ds} = V_{g(on-off)} = V_{dd} = 1 \text{ V}$, the I_{on} of our device at $V_{ds} = 1 \text{ V}$ and 1 V gate swing from the off state is $\sim 25 \text{ }\mu\text{A}$. Taking the channel width of the GNRs as $\sim 15 \text{ nm}$, we obtain the scaled values of I_{on} and g_m of our device to be $\sim 1.7 \text{ mA mm}^{-1}$ and $\sim 2.0 \text{ mS mm}^{-1}$, already exceeding the values of 0.7 mA mm^{-1} and 0.8 mS mm^{-1} in sub-100-nm silicon p-MOSFETs and comparable to those of n-MOSFET devices employing high-*k* dielectrics.[36] This is significant because high transconductance is critical to transistor performance and voltage gains of transistor-based devices including amplifiers and logic gates.

These studies demonstrate that ZrO_2 nanowires can also function as effective gate dielectrics for high performance top-gated GNR devices. It should be noted that the current device has a relatively large channel length ($\sim 500 \text{ nm}$) and large dielectric thickness (ZrO_2 nanowire diameter $\sim 50 \text{ nm}$). It is reasonable to expect that the on current and transconductance can be further improved by shrinking the channel length and decreasing dielectric nanowire diameter. With smaller nanowires, we also expect that top-gated devices with higher on/off ratios can be achieved. Furthermore, with the top-gated devices, multiple GNR FETs and FET arrays can be readily fabricated with independently addressable top gates (Fig. 3a and b), and therefore allowing for diverse electronic functions. For example, a logic OR gate is obtained with two independent gate electrodes fabricated on a GNR in conjunction with a loading resistor (Fig. 3c). The OR function occurs because the output voltage is low only when input to both gates are at low voltages (Fig. 3d). When one or both gates are at high voltages, the GNR channel is electrically shut off, resulting in a high output voltage.

In summary, we have developed a new strategy to integrate high-*k* dielectrics for top-gated GNR transistors. Using the high-*k* oxide nanowires as the gate dielectrics and etch mask, high-performance, top-gated GNR transistors have been fabricated with the highest transconductance ($29 \text{ }\mu\text{S}$ per GNR, $2 \text{ mS}/\mu\text{m}$) and mobility ($\sim 1300 \text{ cm}^2/\text{Vs}$) reported for GNR transistors to date. With the top-gated devices, independently addressable GNR device array and a logic OR gate have also been demonstrated for the first time for GNR devices. This method opens a new avenue to integrate high-*k* dielectrics on GNRs. With further optimization of dielectric nanowire growth and assembly process to precisely control their physical dimension and spatial location, large arrays of top-gated GNR transistors or circuits can be envisioned.

Experimental

Synthesis and characterization of ZrO_2 nanowires

ZrO_2 nanowires were grown at $1000 \text{ }^\circ\text{C}$ by a chemical vapor deposition process in a tube furnace with ZrCl_4 powders as the precursor. In brief, the ZrCl_4 powder in a quartz boat was placed at the upstream with a temperature of $\sim 200 \text{ }^\circ\text{C}$ and a piece of silicon was placed at the center of the tube furnace as the deposition substrate at a temperature of $1000 \text{ }^\circ\text{C}$. Form gas ($5\% \text{ H}_2$ in Ar) with a flow rate of 200 sccm was used as the carrier gas and the reaction medium. The temperature was maintained for 2 hours and then naturally cooled to room temperature. The microstructures and morphologies of the ZrO_2 nanowires were characterized by a JEOL 6700 scanning electron microscope (SEM). The lattice image of the ZrO_2 nanowires was observed by an FEI Titan high-resolution transmission electron

microscope (HRTEM) with energy-dispersive X-ray spectroscopy (EDX). The height and width were obtained using atomic force microscope (AFM, Veeco Dimension 5000).

Contact printing of nanowires on graphene

The overall process involves physical transfer of ZrO_2 nanowires directly from a nanowires growth substrate to a graphene substrate via contact printing. Specifically, a graphene device substrate was first firmly attached to a benchtop, and the nanowire growth substrate was placed upside down on top of the graphene substrate such that the nanowires were in contact with the graphene. A gentle manual pressure was then applied from the top, followed by slightly sliding the growth substrate. The ZrO_2 nanowires were aligned by sheer forces during the sliding process. This process resulted in the direct dry transfer of ZrO_2 nanowires from the growth substrate to the graphene substrate. The sample was then rinsed with isopropanol, followed by nitrogen blow-dry, in which the capillary drying process near the nanostructure could help the nanowires be firmly attached to the substrate surface.

Top-gate graphene nanoribbon transistor fabrication and characterization

Oxygen plasma (Diener Electronic) was used to selectively etch away the unprotected graphene region and leave graphene ribbons underneath the ZrO_2 nanowires mask protection. The etching time was about 160 s at a power level of 40 W. The electrical transport properties were measured by a Lakeshore probe station with home built data acquisition system in ambient condition at room temperature.

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Figure 1.

Schematic illustration of the fabrication process to obtain top-gated graphene transistors using dielectric oxide nanowires as the etching mask and top-gate dielectric. a) A dielectric nanowire is aligned on top of graphene using a dry-transfer process without any additional chemical functionalization to minimize the possibility to introduce defects/impurities into the graphene-dielectric interface, and the source-drain electrodes are fabricated by electron-beam lithography. b) Oxygen plasma etch is used to remove the unprotected graphene, leaving only the GNR underneath the dielectric nanowires connected to two large graphene blocks underneath the source and drain electrodes. c) The top gate electrode is defined through lithography and metallization process.

Figure 2.

Characterization of ZrO_2 nanowires and top-gated GNR transistors with ZrO_2 nanowires as the gate dielectric. a) An SEM image of ZrO_2 nanowires. b) A TEM image of a ZrO_2 nanowire, and the inset shows the SAED pattern of a ZrO_2 nanowire. c) The EDX spectrum of ZrO_2 nanowires shows only zirconium and oxygen signals. The carbon signal comes from the carbon membrane on TEM grid. d) The SEM image of a top-gated GNR transistor with ZrO_2 nanowire as top-gate dielectric. The gate length is about 500 nm and the diameter of the nanowire is 50 nm. Inset shows an AFM image of a ~ 15 nm wide GNR obtained under ZrO_2 nanowire after oxygen plasma etching. The scale bar indicates 200 nm. e) Gate leak current versus top-gate voltage. The leak current is negligible within $V_{\text{gs}} \pm 2$ V. f) $I_{\text{ds}}-V_{\text{ds}}$ output characteristics at variable top gate voltage starting from 0.4 V at bottom to -1.0 V at top in the step of -0.2 V. g) The transfer characteristics $I_{\text{ds}}-V_{\text{TG}}$ at various $V_{\text{ds}} = 0.01$, 0.10 and 1.0 V. h) $I_{\text{ds}}-V_{\text{TG}}$ (red curve) and $I_{\text{ds}}-V_{\text{BG}}$ (black curve) transfer characteristics at $V_{\text{ds}} = 1$ V. i) Transconductance g_{m} as a function of top-gate voltage V_{TG} and back gate voltage V_{BG} (inset).

Figure 3. Independently addressable GNR device array. a) An SEM image of two independently addressable top-gated GNR FETs. b) Transfer characteristics of two top-gated GNR FETs at $V_{ds} = 0.1$ V. c) The SEM image of a logic OR gates built from GNR transistors. The inset shows the schematic circuit diagram. d) The OR gate output characteristics with double top-gates. The operating voltage is $V_{dd} = 1$ V. The inputs for the two gates, A and B, are 1V for state 1 and 0 for state 0.