Published in final edited form as:

Mater Res Soc Symp Proc. 2008 ; 1066: 457–462.

Noise Characterization of Polycrystalline Silicon Thin Film Transistors for X-ray Imagers Based on Active Pixel Architectures

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Abstract

An examination of the noise of polycrystalline silicon thin film transistors, in the context of flat panel x-ray imager development, is reported. The study was conducted in the spirit of exploring how the 1/f, shot and thermal noise components of poly-Si TFTs, determined from current noise power spectral density measurements, as well as through calculation, can be used to assist in the development of imagers incorporating pixel amplification circuits based on such transistors.

INTRODUCTION

Active matrix, flat panel imagers (AMFPIs) are based on large area arrays (presently up to $\sim 43 \times 43 \text{ cm}^2$) whose pixels typically consist of a single hydrogenated amorphous silicon (a-Si:H) thin film transistor (TFT) coupled to a pixel storage capacitor. While such imagers are used in many medical applications, the relatively modest size of the signal generated per detected x-ray by the imager, relative to the electronic (i.e., dark) noise, results in significant loss of imaging performance under conditions of low exposure or very small pixel sizes. To overcome this limitation, a significant increase in signal relative to noise is required [1]. One approach, which preserves the advantages of conventional AMFPIs (e.g., large area, compact), involves the use of polycrystalline silicon (poly-Si) TFTs to create an amplification circuit in every pixel - analogous to the pixel architecture of CMOS active pixel sensors. The considerably higher electron and hole mobilities of poly-Si TFTs, compared to those of a-Si:H TFTs, enable faster switching times and considerably more complex pixel circuits. Initial prototype arrays with 1- and 2-stage poly-Si pixel amplifiers have been developed and show encouraging results [2,3].

For such arrays, a critical issue is the degree to which noise properties of the individual poly-Si TFTs in the pixel circuit limit the performance of the entire imager. In order to fully explore this question, a detailed knowledge of the noise behavior of the individual transistors is required. While many studies of poly-Si TFT noise have been reported [4,5], it is highly desirable to acquire noise data from individual TFTs having the same design, and made in the same manner as those used in actual prototype arrays, since the results should be representative of their performance in pixel circuits. This paper describes a methodology for acquiring and utilizing noise data obtained from individual poly-Si TFTs for purposes of imager development. The methodology is illustrated through measurements of current noise power spectral density. This research was conducted in the spirit of a pilot study toward understanding the relationship between the range of conditions over which good quality data can be obtained, and how such information can aid the development of poly-Si imagers based on active pixel architectures.

MEASUREMENT METHODOLOGY

The poly-Si imager array development underway in our group is being performed in collaboration with scientists at the Palo Alto Research Center, where the arrays are fabricated.

The present noise measurements were performed on individual poly-Si TFTs located in regions of array substrates reserved for “test devices”. In this study, one transistor design was examined: an n-channel transistor with an 8 μm width (W), and two 5 μm long (L) gates. This design corresponds to the addressing transistor and the reset transistor used both in 3-TFT, as well as in 5-TFT prototype pixel amplifier arrays (“PSI-2” and “PSI-3”, respectively) [2,3]. The transistors were fabricated through pulsed excimer-laser crystallization [2], with a 50 nm thick poly-Si film, and a 100 nm thick gate oxide with a gate capacitance of $3.45 \times 10^{-8} \text{ F/cm}^2$.

Current measurements on the TFTs were performed using a methodology described below, involving the apparatus shown in Figure 1. Micro-positioning probes made electrical contact to the TFT in a light-tight aluminum box constructed to reduce the effect of external electromagnetic noise. To further minimize noise, the voltages applied to the TFT gate, V_{GS} , and drain, V_{DS} , were supplied by NiMH batteries (housed in a shielded box), with fine adjustment of V_{GS} performed using a high precision potentiometer. The source current, I_{DS} , was amplified by a high-sensitivity current preamplifier (SRS, model SR570), with selectable gain settings, and digitized by a standard data acquisition card (National Instruments, NI PCI-6280). The reported results correspond to measurements obtained from a single, high-quality TFT whose behavior is believed to be representative of properly functioning transistors in the prototype array designs.

DETERMINATION OF CURRENT NOISE POWER SPECTRAL DENSITY, S_I

For this study, current data was acquired at a sampling frequency of $\sim 606 \text{ kHz}$ over an interval of $\sim 443 \text{ s}$, resulting in a total of $\sim 2.68 \times 10^8$ samples. This allowed empirical examination of the poly-Si TFT noise properties over as large a frequency range as possible, limited only by practical considerations imposed by the preamplifier bandwidth and noise, as well as by limitations associated with our ability to maintain mechanically and electrically stable conditions over the course of a measurement. For a given set of current data acquired for a particular combination of V_{DS} and V_{GS} voltages, the data was subjected to a linear detrending correction, to account for small drifts in the measured current (e.g., arising from battery discharge).

The results presented in Figure 2 and Table I correspond to a V_{DS} value of $\sim 1.3 \text{ V}$, supplied by a single battery cell, and for V_{GS} values ranging from ~ 0.9 to 10.5 V . The V_{GS} values are listed in column 1 of Table I, where the lowest voltage corresponds to the lowest TFT current that allowed extraction of valid results, given the aforementioned preamplifier and measurement interval limitations. The magnitude of the source current, I_{DS} , and the corresponding choice of a preamplifier gain setting, are given for each V_{GS} value in columns 2 and 3 of Table I. Figure 2(a) shows current power density results corresponding to several values of V_{GS} , obtained from the detrended current data via a fast Fourier transform (FFT). Data is presented up to the frequency at which the preamplifier bandwidth and/or noise becomes a limitation. The limiting frequency up to which valid data could be obtained at each V_{GS} value is given in column 4 of Table I.

The results shown in Figure 2(a) correspond to contributions from various noise sources: $1/f$, shot and thermal noise from the TFT, as well as preamplifier noise. Towards obtaining the $1/f$ component, expected to be a major contributor to pixel circuit noise, the spectral density of preamplifier noise was determined through application of the same methodology described above, replacing the TFT with various resistors. The results are shown in column 5 of Table I. The spectral densities of the shot and thermal TFT noise, S_{SHOT} and S_{TH} , were estimated using the expressions [6]:

$$S_{SHOT} = 2qI_{DS} \quad (\text{A}^2/\text{Hz}) \quad (1)$$

and

$$S_{TH} = 4k_B T \cdot I_{DS} / V_{DS} \quad (\text{A}^2/\text{Hz}) \quad (2)$$

respectively, where k_B is Boltzmann's constant, T is temperature and q is the magnitude of the charge of an electron, and the resulting values are shown in columns 6 and 7 of Table I.

For a given value of V_{GS} , the 1/f component of the current power density was obtained as follows. Through application of Welch averaging [7] (in the present case, by dividing the detrended current data into 50 segments, and averaging the FFTs of each segment), the spread of the current power density results was reduced. Subtraction of the spectral densities for TFT shot, TFT thermal and preamplifier noise from the average noise power yields an estimate of the 1/f component. Figure 2(b) shows the resulting 1/f current power density for several values of V_{GS} . The relatively small degree of non-linearity visible in the figure may originate from the intrinsic behavior of the TFT itself [5] - and is under further investigation. For purposes of this pilot study, a linear fit to the results for each value of V_{GS} , based on the expression:

$$S_{1/f} = K/f^\alpha \quad (\text{A}^2/\text{Hz}), \quad (3)$$

where K and α are the fit parameters, was performed and is indicated by dashed lines in the figure. The values of K and α obtained from these fits are given in the last two columns of Table I. The magnitude of K scales closely with I_{DS} over most of the investigated range of V_{GS} , as anticipated [8]. The average value of α is 0.95. Note that, while the variation of α with V_{GS} at values above ~5 V is interesting, the data are insufficient to warrant any definite conclusion on a possible correlation between α and V_{GS} .

USE OF Poly-Si NOISE RESULTS IN IMAGER ARRAY DEVELOPMENT

Poly-Si TFT noise characteristics, such as the results reported above, can assist in the development of x-ray imaging arrays, based on such transistors, in a variety of ways. i) It is important to examine noise for different TFT widths, lengths and channel types, and to monitor how changes to the TFT fabrication process (e.g., increasing the laser power to increase TFT mobility) affect noise. Since the noise depends upon the quality (e.g., the trap density and grain size) of the poly-Si material [4,5], it is also useful to examine how noise varies across a given substrate - as this could introduce non-uniform performance across an array. ii) Investigating changes in TFT noise as a function of radiation dose provides information about the suitability of poly-Si for applications with different lifetime doses to imaging arrays [9]. iii) TFT noise measurements can be compared against predictions from analytical models [10]. iv) Empirically determined TFT noise information can be used as input to circuit simulations that allow more extensive and detailed modeling of the noise behavior of complex circuits than is possible through analytical means alone. An example of such modeling is described below.

The modeling was conducted for a circuit corresponding to the output stage common to prototype poly-Si amplifier arrays [2,3]. The circuit in Figure 3(a) consists of a source-follower, TFT_{SF} , and an addressing transistor, TFT_{ADDR} , both in parallel with their respective current noise sources, I_{NOISE} (i.e., $I_{SFNOISE}$ and $I_{ADDRNOISE}$). The input to the circuit simulation for each noise source is based on the measured 1/f noise power density results reported in Table

I. The simulation was constructed to examine how $1/f$ noise affects charge transfer to the capacitance, C_{DATA} , of an array data line as a function of readout time, t_{RO} (the time after TFT_{ADDR} is switched on). The parameters for this circuit and simulation details are described in ref. [11].

The modeling involved three steps. In the first step, the circuit simulation is run without the current noise sources. For each 1 ns simulation timestep (the smallest timestep that was computationally practical for this pilot study), I_{DS} currents for both TFTs, as well as the dataline voltage V_{OUT} , are recorded, the latter being shown in the top graph of Figure 3(b). Step 2 uses these currents, along with the measured $1/f$ noise results, to generate random noise datasets that are input as $I_{SFNOISE}$ and $I_{ADDRNOISE}$ to another simulation run in Step 3. Six examples of such noise datasets for $I_{ADDRNOISE}$ are illustrated in the middle graph of Figure 3(b), and details of this noise generation step are described below. In Step 3, V_{OUT} is recorded and subtracted from the V_{OUT} values from Step 1, resulting in a waveform for the voltage difference, ΔV_{OUT} . Steps 2 and 3 are repeated many times to build up a statistically meaningful number of ΔV_{OUT} waveforms six of which are illustrated in the bottom graph of Figure 3(b).

For each simulated TFT, the generation of I_{NOISE} in Step 2 involved creating a normalized spectral density, S_N , which is derived from the results presented in Table I. These results were scaled to match the dimensions and operating points of the TFT. It is assumed that the two 5 ! m long gates of the measured device behave like a single 10 μm long gate. The relationship used to derive S_N from Table I results is a first order approximation based on relations shown in references [8] and [12]:

$$S_N = S_{1/f} W^2 L^2 / I_{DS}. \quad (4)$$

A temporal $1/f$ noise data set, Z_N , with one datapoint for each timestep over the simulated period, is generated by taking the inverse FFT of $\sqrt{S_N}$, with a random phase for each frequency. The current noise, I_{NOISE} , for each simulated TFT is created by scaling Z_N by the I_{DS} that corresponds to the TFT current for each timestep, and by the device dimensions according to the equation:

$$I_{NOISE}(t_{RO}) = Z_N(t_{RO}) \sqrt{I_{DS}(t_{RO}) / (WL)} \quad (A). \quad (5)$$

The resulting I_{NOISE} provides a reasonable approximation for $1/f$ noise current behavior of the simulated TFTs. Further improvements to this approximation would include obtaining noise data from a variety of TFTs, making measurements with finer adjustments of V_{GS} and V_{DS} , using a more sensitive current preamplifier for low current measurements, and using a non-linear fit to the current power density to allow a more precise determination of the $1/f$ noise scaling factors.

In the present example, the parameters chosen in the circuit simulation correspond to a 3-TFT, one-stage pixel amplifier array [11] with 2000×2000 pixels, a pitch of 150 μm, and a pixel capacitance of 1.5 pF. In fluoroscopic operation, the inverse of t_{RO} determines the maximum possible frame rate. In the study, Steps 2 and 3 were repeated a total of 100 times. The standard deviation of the resulting ΔV_{OUT} waveforms at a particular t_{RO} corresponds to the rms noise, due to TFT $1/f$ noise contributions, on the data line at that readout time. From these runs, the rms noise is found to be 2.9 and 0.56 μV at readout times of 5 and 50 μs, corresponding to maximum frame rates of 100 and 10 frames per second (fps), respectively. For these two t_{RO} values, ~89% and 97% of the signal is transferred to the data line, and the resulting magnitude

of the noise from the modeled part of the pixel circuit, referred to the pixel storage capacitor, is ~ 31 and 5 e^- [rms], respectively. By comparison, the electronic pixel noise of a conventional AMFPI would be on the order of 10^3 e^- [rms]. Thus, the model suggests that the $1/f$ noise contribution from the output stage of the pixel amplifier circuit, operated in charge readout mode, will not be a limiting factor in noise performance. Of course, significantly larger noise contributions from other circuit elements (e.g., reset TFT), as well as other noise components (i.e., shot and thermal) also need to be considered - and can be modeled using techniques similar to those described above. It is anticipated that such modeling will be valuable in poly-Si array development by helping to optimize noise, readout speed, linearity and other properties [11] through detailed examination of promising pixel circuits, and variation of device and processing parameters.

DISCUSSION

For flat panel imagers based on poly-Si arrays with active pixel architectures, the degree to which large improvements in signal to noise performance can be realized will strongly depend upon the noise properties of the pixel circuit and its constituent TFTs. It is therefore anticipated that the development of such imagers will benefit from noise modeling involving circuit simulations parameterized by detailed information obtained from poly-Si TFT measurements of the type reported in this paper. Further refinement of this methodology is under investigation.

Acknowledgments

We wish to thank Mike Yeakey, Chuck Martelli and Taeyjuana Curry for assistance with instrumentation and data acquisition, and Robert Street and JengPing Lu of PARC for useful discussions. This study was partially supported by NIH grant R01 EB000558.

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Figure 1.

Schematic illustration of the apparatus used to measure source current from individual poly-Si TFTs for purposes of current power density determination. DAQ refers to the data acquisition card.

Figure 2.

Plots of empirically determined current power density, S_I , as a function of frequency, for several values of V_{GS} . (a) The total power density of the TFT, prior to averaging and preamplifier noise correction. (b) The $1/f$ component of the power density, after averaging, and after correcting for other known noise contributions. See text for further details.

Figure 3.

(a) Schematic diagram of the simulated circuit. (b) Results, plotted as a function of readout time, t_{RO} , at 0.5 μs intervals for clarity, for: (top) the output voltage, V_{OUT} from Step 1 of the modeling; (middle) the input noise source, $I_{ADDRNOISE}$, from Step 2; and (bottom) the difference between the output voltage with, and without current noise sources, ΔV_{OUT} , from Step 3.

Summary of information and results related to determination of noise components for the poly-Si TFT at a V_{DS} of 1.3 V. For each value of V_{GS} (column 1): the corresponding source current (column 2); the preamplifier gain setting at which data was acquired (column 3); the limiting frequency of the preamplifier (column 4); the measured preamplifier noise level (column 5); calculational estimates of TFT shot and thermal noise (columns 6 and 7); and the parameters from the fit of the $1/f$ noise, K and α (columns 8 and 9, respectively), are reported.

Table I

V_{GS} (V)	Source Current, I_{DS} (A)	Preamplifier Gain Setting (A/V)	Preamplifier Limiting Freq. (Hz)	Preamplifier Noise (A^2/Hz)	Shot Noise, S_{SHOT} (A^2/Hz)	Thermal Noise, S_{TH} (A^2/Hz)	$1/f$ Noise Parameter, K (A^2)	$1/f$ Noise Parameter, α
0.9	3.9×10^{-11}	2×10^{-11}	0.5	4.1×10^{-29}	1.3×10^{-29}	4.8×10^{-31}	4.1×10^{-27}	0.93
1.3	5.9×10^{-10}	5×10^{-10}	3	5.0×10^{-29}	1.9×10^{-28}	7.2×10^{-30}	3.8×10^{-25}	0.91
1.5	9.1×10^{-10}	1×10^{-9}	5	4.7×10^{-29}	2.9×10^{-28}	1.1×10^{-29}	8.1×10^{-25}	0.97
1.7	2.5×10^{-9}	2×10^{-9}	15	1.9×10^{-27}	8.1×10^{-28}	3.2×10^{-28}	4.1×10^{-24}	0.86
2.6	5.7×10^{-8}	5×10^{-8}	100	2.2×10^{-27}	1.8×10^{-26}	7.0×10^{-27}	3.2×10^{-22}	0.93
3.9	4.0×10^{-7}	2×10^{-7}	1,000	3.6×10^{-25}	1.3×10^{-25}	5.0×10^{-26}	4.8×10^{-21}	0.95
5.2	1.2×10^{-6}	1×10^{-6}	1,000	3.9×10^{-25}	3.9×10^{-25}	1.5×10^{-26}	1.2×10^{-20}	0.92
6.6	2.5×10^{-6}	2×10^{-6}	10,000	5.1×10^{-24}	7.9×10^{-25}	3.1×10^{-26}	3.3×10^{-20}	0.97
7.8	3.9×10^{-6}	2×10^{-6}	10,000	5.1×10^{-24}	1.2×10^{-24}	4.8×10^{-26}	5.2×10^{-20}	1.00
9.1	5.7×10^{-6}	5×10^{-6}	10,000	5.2×10^{-24}	1.8×10^{-24}	7.1×10^{-26}	8.7×10^{-20}	1.01
10.5	7.9×10^{-6}	5×10^{-6}	10,000	5.2×10^{-24}	2.5×10^{-24}	9.7×10^{-26}	1.3×10^{-19}	1.03