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A picoampere A/D converter for biosensor applications

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Abstract

Detection and analysis of biological and biochemical signals via compact sensor systems require low-power and compact analog-to-digital converter (ADC) systems. Here we present a highly sensitive flash current-mode ADC (IADC) design with resolution down to 15pA. The IADC's small-size and low-power capabilities allow integration for stand-alone biological or chemical microsensor applications.

Introduction

Advances in microfabrication technology have allowed integration of microfluidics, photonics and microelectronics for a variety of biomedical lab-on-a-chip applications [1–3]. This technology aids in rapid, selective, and inexpensive analysis of environmental pollutants or medical conditions [4]. However, stringent area and especially power budgets place constraints on electronic circuits for signal detection and processing and require optimization based on *a priori* knowledge of the incoming signals' characteristics. For example, bioluminescence reporter systems or experimental *in-vitro* patch clamp recordings generate signal currents on the order of picoampere (pA) with a relatively narrow dynamic range and bandwidth. Such applications require an IADC design featuring ultrahigh input sensitivity but with only moderate resolution and sampling rate necessary [5,6].

There are currently two major approaches for pA-level detection. The first one uses a voltage-mode ADC with an integration capacitor and a comparator to convert the current into voltage [7–11]. However, this approach has several drawbacks. For example, in a current integrator system, an integration capacitor of at least several pF is typically required in order to minimize noise and clock feedthrough [7,8]. Such a large capacitance necessitates a long integration time from ~30s [9] to several minutes [10] if a resolution at the pA or fA level is desired. The exceedingly long capacitive integration time in the front-end severely limits the overall conversion rate even though the voltage-mode ADCs associated with current integrators are capable of much higher sampling speed from several hundred kHz to several hundred MHz [8,10–13]. Moreover, a pF Metal-Insulator-Metal (MiM) capacitor or poly-poly capacitor also occupies a large area, making it inappropriate to be included on-chip if many channels are needed. Although much smaller capacitors (such

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as moscap) can be used here to reduce the capacitor area, the inherent nonlinearity of these non-ideal capacitors makes it not suitable for accurate measurement. Finally, in a current integrator system, the voltage-mode ADC must constantly reset the capacitor voltage during the presence of a large input current [13], which will introduce additional reset noise. More circuitry then has to be introduced to remove this noise, incurring more complexity and power consumption.

The second approach uses large-gain current mirrors before converting to voltage, increasing power consumption and area [14]. A small mismatch between devices can be translated into large current mismatch. The transistors in the first several stages of the current mirror must be made extremely large to limit the mismatch. This approach is inappropriate for high precision pA current detection.

Advances in CMOS circuit technology with decreasing supply voltages have increased the popularity of IADC designs. Current-mode circuits feature lower voltage swings and low signal line impedance, and are immune to supply node noise. Thus, current-mode circuits can operate at higher frequencies than voltage-mode designs in the face of decreasing power supply voltages [15–17], and allow direct interface with the input current signals. Previous designs of flash current-mode IADCs have focused on ultra-high-speed sampling and operate in the μA range [18–21]. These designs have not been shown to be sensitive for the pA-nA level currents important for bioluminescence and biosensor applications.

Our ADC can be used with nanoscale biosensors in the presence of very small currents (fA-pA). Recent biosensors, including the carbon nanotube array electrodes [22] and the CMOS chemiluminescence sensor [23], have small sizes and generate currents in the pA level. Carbon nanotubes can be possibly integrated with CMOS circuits utilizing die-level post-CMOS processing to minimize the sensor size [24].

We have previously proposed a flash IADC with a resolution of 500pA [25]. Here we present a CMOS IADC with sensitivity down to 15pA and with a programmable dynamic range that allows operation over many orders of magnitude. The compact design, low cost and its ability to interface with digital signal processing circuits makes the present IADC ideally suited to a variety of small, rugged, ultra-low-power devices, such as lab-on-a-chip systems.

Methods

The proposed N-bit IADC is composed of two subcircuits: 1) a 2^N -bit thermometer code generating circuit; and 2) a thermometer-to-binary encoder consisting of 1-out-of- 2^N circuit and fat-tree binary encoder (Fig. 1).

2^N -bit thermometer code A/D converter

Traditionally voltage-mode flash conversion schemes work by dividing a reference voltage into 2^N equal steps, where each step corresponds to the least-significant bit (LSB). V_{IN} is then compared to all 2^N stages concurrently and generates the output code in one conversion cycle. Thus, flash conversion is fastest for any ADC architecture. Flash IADC's have been previously designed to operate at ultra-high speed sampling rates [18–21], but never below the μA current range.

We designed a resistive ladder using diode-connected MOS transistors to divide a tunable reference current I_{REF} into 2^N equal steps (Fig. 2A). Setting I_{REF} to the nA-pA range biased the transistors in weak-inversion resulting in very small voltage swings. The

transconductance (g_m) of a weakly inverted MOS is $g_m = \frac{\kappa I_B}{\varphi_t}$, where I_B is the DC current, κ is the coupling coefficient, and φ_t is the thermal voltage (25 mV in room temperature). The resistor value is thus (Fig. 2A):

$$R_{Eq} = \frac{1}{g_m} = \frac{1}{\frac{\kappa W_A / W_R I_{REF}}{\varphi_t}} = \frac{W_R \cdot \varphi_t}{W_A \cdot \kappa I_{REF}} = \frac{W_R \cdot \varphi_t}{\kappa I_{REF}} \cdot \frac{1}{W_A} = \frac{K_{REF}}{W_A} \quad (1)$$

where W_R is the sum of transistor's widths ($W_A + W_B$), and W_A and W_B are the transistor

widths in Fig. 2A. To first order, $K_{REF} = \frac{W_R \cdot \varphi_t}{\kappa I_{REF}}$ is a constant for a given I_{REF} and W_R , and the resistor value is inversely proportional to its transistor width. R_{Eq} is a small signal (or dynamic) resistor that relies on the bias current I_{REF} . Its resistance changes if the biasing current I_{REF} is different.

The 2^n resistive ladder is implemented based on Eqn. (1), where R_{Eq} is inversely proportional to the transistor width. The resistive ladder includes 2^{n-1} W_R cells (Fig. 2B) and the detailed implementation of W_R cells is shown in Fig. 2A. In this W_R cell, the incoming reference current I_{REF} is divided into two branch currents depending on the width ratio between transistors A and B. The current through transistor A ($I_{REF} W_A / W_R$) and B ($I_{REF} W_B / W_R$) are then compared with the incoming current I_{IN} . Here W_R is defined as the sum of transistor widths W_A and W_B . The comparator generates a digital "HI" for

$I_{IN} > I_{REF} \frac{W_{A/B}}{W_R}$, or a "LO" for $I_{IN} < I_{REF} \frac{W_{A/B}}{W_R}$ (Fig. 2A). I_{REF} may be tuned over a wide current range dictating the converter's input dynamic range $0 < I_{IN} < I_{REF}$.

In the W_R cell shown in Fig. 2A, the subthreshold drain current of transistor A and B is [26]:

$$\begin{aligned} I_{DS,A} &= 2n\mu C_{OX} \frac{W_A}{L} \varphi_t^2 \exp \frac{V_G - V_{T0}}{n\varphi_t} \left(1 - \exp \frac{-V_G}{\varphi_t} \right) \\ I_{DS,B} &= 2n\mu C_{OX} \frac{W_B}{L} \varphi_t^2 \exp \frac{V_G - V_{T0}}{n\varphi_t} \left(1 - \exp \frac{-V_G}{\varphi_t} \right) \end{aligned}$$

where μ is the mobility for electrons, W_A and W_B are transistor widths, L is the transistor length, V_G is the gate terminal voltage, V_{T0} is equilibrium the threshold voltage, n is the slope factor ($=1/\kappa$), and φ_t is the thermal voltage. Since $I_{DS,A}/I_{DS,B} = W_A/W_B$ and $I_{DS,A} + I_{DS,B} = I_{REF}$,

$$I_{DS,A} = \frac{W_A}{W_A + W_B} I_{REF} \quad \text{and} \quad I_{DS,B} = \frac{W_B}{W_A + W_B} I_{REF}$$

Therefore the drain-to-source current of transistor A and B in Fig. 2A only depends on the ratio between their widths given the same external reference current.

The same W_R cell is repeated $2^{(n-1)}$ times in the resistive ladder (Fig. 2B) but with different W_{As} and W_{Bs} . For a particular W_R cell k ($k=1, 2, 3, \dots, 2^{(n-1)}$) in our implementation, the transistor A width $W_{A,k} = k W_A$ and transistor B width $W_{B,k} = (2^n - k) W_A$. Therefore in each cell I_{IN} is compared with different levels of currents.

Mismatch is critical in our resistive ladder design. The mismatch between multiple transistors can be characterized by measuring the standard deviation of the drain-source current $\sigma(\Delta I_{DS}/I_{DS})$. It has been shown that the standard deviation of the drain-source current can be characterized by two statistical parameters: the standard deviation of the threshold voltage mismatch $\sigma_{VT} = \sigma(\Delta V_T)$, and the standard deviation of $\Delta\beta/\beta$, where β is defined as $\mu C_{ox} W/L$. Here μ is the mobility of the device, C_{ox} is the capacitance of the gate oxide per unit area, and W/L is the width to length ratio of the transistor [27]. It has been proved that in the weak-inversion regime the threshold voltage mismatch ΔV_T plays a major role in the overall mismatch [28]. The standard deviation of the drain-source current can be approximated as:

$$\sigma(\Delta I_{DS}/I_{DS}) \cong \frac{\sigma_{VT}}{n\phi_T}$$

where n is the slope factor [28]. To estimate the mismatch we then must first estimate σ_{VT} [29]:

$$\sigma_{VT}^2 = \frac{A_{VT}^2}{W \times L}$$

where A_{VT} is the technology conversion constant. This technology conversion constant is reported to be $\sim 1\text{mV} \cdot \mu\text{m}$ per nm oxide thickness [30]. The typical gate oxide thickness is 32nm in the AMIS 1.5 μm process [31]. In this work $\sigma(\Delta I_{DS}/I_{DS})$ is kept less than 2% when the minimum transistor area WL in the resistive ladder is larger than $64\mu\text{m}^2$.

The noise in the ADC consists of thermal noise and quantization noise. The thermal noise contribution due to current references and the operational amplifier, can be summarized as a single equation according to [32,33]:

$$I_N^2(f) = 4\gamma K T g_m \Delta f$$

where I_N is the thermal noise current, K is Boltzmann's constant, T is absolute temperature, and g_m is the equivalent conductance that combines effects of input referred noise due to current references and operational amplifier. Δf denotes the bandwidth of the converter, and $\gamma = 2/3$ for above-threshold operation and $\gamma = 1/2\kappa$ for sub-threshold operation. Therefore in the sub-threshold region, the thermal noise of the MOS device in a unit bandwidth is modeled as:

$$I_N^2 = 4KT \left(\frac{1}{2\kappa} g_m \right)$$

The Boltzmann constant is 1.38×10^{-23} J/K, and here we assume T is 300K. The transconductance g_m of the W_B device under the sub-threshold region is (see Fig. 2A and Eqn. (1)):

$$g_{m,W_B} = \frac{\kappa \frac{W_B}{W_R} I_{REF}}{KT/q}$$

where q is the charge of $1.6 \times 10^{-19} \text{C}$, $W_R = W_A + W_B$. The thermal noise of the MOS device is:

$$I_N^2 = 2q \frac{W_B}{W_R} I_{REF} = 2 \times 1.6 \times 10^{-16} \times 10 \text{pA}$$

The minimum current in Fig. 2A is 10pA. Therefore the signal-to-noise ratio is:

$$\frac{I_{signal}^2}{I_N^2} = \frac{(10 \text{pA})^2}{2 \times 1.6 \times 10^{-16} \times 10 \text{pA}} = 45 \text{dB}$$

The quantization noise of the ADC is limited by its resolution (4 bits), which is calculated as:

$$\text{SNR (in dB)} = N \times 6.02 + 1.76 = 25.84 \text{ dB}.$$

Therefore the quantization noise is much larger than the thermal noise. As a consequence the ADC is dominated by the quantization noise. When higher SNR is needed, we can extend the ADC resolution to 8–10 bits then the thermal noise dominates. One problem remaining here is the exponential growth of the ADC power and area. The two-step flash ADC architecture can be used here to overcome this difficulty [34]. The area, power, and the delay of the 8-bit two-step ADC are all twice of those in a 4-bit ADC. Its speed is still much faster than the integrator approach with a time frame of several minutes.

This converter operates in current mode and does not require resistors or capacitors. Current-mirror mismatch was minimized by using relatively large transistors and careful layout technique. The independence of transistor drain current on drain-source voltage in subthreshold-biased transistors simplified current-mirror designs. We assumed that all on-chip circuits are subject to the same temperature, and that κ is constant across all transistors. Noise contribution to these signals is a relatively minor effect especially for the coarse resolution of the IADC. We ensured that the mismatch was less than input-current inaccuracy (typically ~10% for bioluminescence signals).

Thermometer to binary conversion

To allow for general-purpose signal processing and storage, the thermometer code is converted into a binary code—a process required for every flash-style converter. First, the thermometer code is converted into a 1-out-of- 2^n code representation by finding the point of the thermometer code where the “1” string changes to “0” by using 2^n exclusive OR cells (Fig 2C). The 1-of- N code is sent to a fat-tree encoder [35] which is smaller, more noise tolerant, and faster than traditional ROM/PLA encoders. The elimination of clocks, sense amps or pull-up resistors results in decreased power consumption. Figure 2D shows an example of a 4-bit Fat Tree Encoder.

On-chip reference current generator

The reference current I_{REF} in Fig. 2A, B can be provided either on-chip or off-chip. Off-chip picoampere or subpicoampere reference currents often require expensive instrumentation with complicated low leakage setups. For our proposed ADC, the reference current may be generated on-chip with high accuracy, and may be calibrated against off-chip reference currents where necessary. For example, the bias current generator presented in [36] can be used to generate accurate reference currents as long as the temperature does not vary

significantly. The circuit includes three sections: a kickstart & power down section, a master bias section, and a current splitter section. The master bias section generates a bias current that is proportional to the absolute temperature T :

$$I_m = \log(M) \frac{U_T}{R}, U_T = \frac{kT}{q}$$

where U_T is the thermal voltage. The resistor R was an off-chip resistor in [36] for flexibility but an on-chip resistor is more accurate.

The N -stage current splitters splits the I_m current by 2^N , where $N=1, \dots, 60$ in [36]. The splitter can generate currents within 10% of the ideal predicted value. Small reference currents can be generated in this manner either by copying the current from one splitter or combining the currents from several splitters. The impact of temperature variations (assuming 15°C–100°C) becomes significant only when the splitter current goes down to the 10pA range, while the reference current used for our proposed ADC is much higher.

Results

The measurement results of the 4-bit IADC is summarized in Table I. As a proof of concept, several 4-bit IADCs were prototyped using the AMIS 1.5μm process on MOSIS. An Agilent 4156C was used to generate both I_{IN} and I_{REF} . Input current was set to $0 < I_{IN} < I_{REF}$, while I_{REF} was tuned over 5 orders of magnitude from single pA to 10s of nA range. For $I_{REF} = 16\text{nA}$, the IADC dynamically followed a 10 Hz sawtooth I_{IN} signal (Fig 3A). For $I_{REF} = 160\text{pA}$, the thermometer bits displayed sensitivity to I_{IN} steps of 15pA at frequencies > 0.1 Hz (Fig. 3B), the best resolution of any available IADC design.

The IADC response bandwidth is determined by the conversion delay, defined as the maximum rise or fall time (whichever is longer) of all cell responses when switching on or off, respectively. For each cell, this value is determined primarily by the corresponding comparator's switching time, $\tau \propto (C_L \cdot V_{DD}) / (I_{IN} - I_{REF})$, where C_L is the load capacitance. The delay in the digital encoding adds a second component. For $C_L \sim 1\text{pF}$ and I_{REF} and I_{IN} in the 10s of pA range, $\tau \sim 1$ sec. Therefore, conversion speed at such low currents is limited by the comparator's capacitance. Other converter designs may aid in faster conversion [37]. Additionally, adding a bias current component to I_{REF} and I_{IN} will significantly increase conversion speed at a cost of additional power consumption.

The IADC accuracy was compared at varying supply voltages, signal frequencies and I_{REF} values. Integral nonlinearity (INL) and differential nonlinearity (DNL) showed that the IADC accuracy was good to $N-1$ (i.e. the 4-bit resolution had accuracy down to 3 bits) (Fig 4A). Interestingly, the offset, gain errors, INL, and DNL were relatively constant independent of operating conditions (Fig 4B–D). This suggested that fabrication-dependent geometric mismatch of current mirrors and comparators were the main culprits. A proper calibration procedure allowed the nullification of the errors and to recapture almost complete 4-bit resolution.

The chip has a dimension of 4.6mm×4.6mm simply because we need many pins for testing (Fig. 5) with a power consumption of 9.05nW. This ADC size decreases directly in proportion to the λ value of the semiconductor process because no capacitors or inductors are involved. For a 1.5μm process the ADC area is about 1.5mm².

Discussion

Integrated biosensors such as chemi- and bioluminescence detection systems or patch clamp electrodes generate currents on the order of pA. Such ultra-low currents must be digitized with sufficient speed to capture chemical reaction dynamics or activation/inactivation dynamics. By combining a flash architecture with a current-mode approach, the present design provides one of the fastest digitization procedures for such ultra-low amplitude currents. The currently fabricated IADC has a resolution of 4 bits. Simulations using T-Spice (Tanner tools, CA) showed an 8-bit version performing as designed and allowing a wider input dynamic range. Most bioluminescence signals have an accuracy of about 5–10% [38], which requires only 3–4 bit resolution so that the flash architecture will suffice. The flash architecture has the advantage of fast conversion. If larger dynamic range is needed and conversion speed is not critical, a sigma-delta ADC may be designed with higher resolution. A tunable reference current allows the IADC to operate at a predetermined dynamic range based on expected input signal. Because each additional bit requires doubling the area and power, a prudent design with appropriate bit-resolution for specific inputs results in tremendous savings. The IADC can be incorporated into a sophisticated stand-alone system for a variety of low-power, portable biosensor systems.

A fundamental design requirement is accurate copies of both I_{REF} and I_{IN} to within 0.5 LSBs. To obtain high fidelity copy, large current-mirrors are sometimes used, but these increase capacitance and decrease conversion speed. A careful common-centroid layout scheme has been used to combat fabrication-dependent mismatch [39]. Current-mirror designs with cascaded transistors may not be useful because of the drain current's independence of drain voltage in MOS transistors biased in weak inversion. However, other design techniques such as tilted current mirrors may increase coping accuracy for currents in the pA range [40]. Nevertheless, inevitable geometric mismatches and offsets require careful calibration of the IADC. The relative independence of these errors on supply voltage, input current levels and signal bandwidth allows the use of a calibration curve to increase accuracy up to the full N-bit resolution.

The proposed ADC represents a proof-of-concept. In practice, a bubble suppression circuitry may be added to increase the reliability of the ADC [34] although the present design should suffice for most biosensor applications. Most input signals have time constants that are much larger than the ADC signal settling time (the time between onset of input signal variation to the stable ADC output). The IADC output signals may have random transitions at the beginning but will eventually settle to their desired values. In addition, bubble suppression circuitry is added in traditional ADC designs mainly to reduce the impact of comparator offset or malfunction [34]. In our proposed IADC, the impact of comparator offset is minimal as the output signal will eventually flip as long as the input signal I_{in} and the bottom current source (e.g., W_A or W_B in Fig. 2A) are not identical. Furthermore, comparator failure is rare in IC design.

Our ADC is designed to detect pA level currents from any biosensors. Any input DC offset current from a biosensor may be removed by including a suitable bias current during initial calibration. Future generations of the IADC design may be integrated along with photodiodes to facilitate fast transmission between the sensor and the IADC. Additionally, application-specific digital logic may be incorporated to allow a fully functional low-power sensor.

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Fig 1.
IADC architecture.

Fig 2. IADC Building blocks. **A).** A conversion cell splits I_{REF} into 2 fractions determined by W_A and W_B , which are independently compared to I_{IN} and generate digital outputs. **B)** The IADC overall architecture. 2^{n-1} conversion cells receive I_{IN} and I_{REF} in parallel and generate the thermometer-code output. **C)** The 1-out-N encoder portion that has thermometer code as input ($N=2^n$). **D)** Fat-tree encoder to generate binary output.

Fig 3. IADC dynamic results. A) IADC binary output for a triangle I_{IN} signal and $I_{REF} = 16\text{nA}$. B) IADC last two thermometer bits in response to a triangle I_{IN} with steps of 15pA and $I_{REF} = 160\text{pA}$.

Fig 4.

IADC accuracy. A) Plot of DNL and INL ($I_{REF}=480\text{pA}$). B) The $I_{IN} - D_O$ conversion curve for several V_{DD} values. C) The $I_{IN} - D_O$ conversion curve for several I_{IN} frequencies. D) The $I_{IN} - D_O$ conversion curve for several I_{REF} values.

(a)

(b)

Fig. 5.
The ADC chip with a dimension of 4.6mm×4.6mm: (a) the layout; (b) the chip photo.

Table I

Summary of the IADC Performance.

Performance	$I_{\text{ref}}=16\text{nA}$	$I_{\text{ref}}=160\text{pA}$
Voltage	1.5V	
Sensitivity	1.0nA	15pA
Chip Area/Active ADC Area	4.6×4.6mm ² /1.5mm ²	
CMOS Technology	CMOS 1.5μm	
Current Mirror Mismatch	<2%	
Max Running Frequency	~10Hz	~1Hz
Power	N/A	9.05nW