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Silicon on Insulator MESFETs for RF Amplifiers

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Abstract

CMOS compatible, high voltage SOI MESFETs have been fabricated using a standard 3.3V CMOS process without any changes to the process flow. A 0.6 μ m gate length device operates with a cut-off frequency of 7.3GHz and a maximum oscillation frequency of 21GHz. There is no degradation in device performance up to its breakdown voltage, which greatly exceeds that of CMOS devices on the same process. Other figures of merit of relevance to RF front-end design are presented, including the maximum stable gain and noise figure. An accurate representation of the device in SPICE has been developed using the commercially available TOM3 model. Using the SOI MESFET model, a source degenerated low noise RF amplifier targeting operation near 1GHz has been designed. The amplifier was fabricated on a PCB board and operates at 940MHz with a minimum NF of 3.8dB and RF gain of 9.9dB while only consuming 5mW of DC power.

Keywords

Silicon on insulator technology; MESFET; TOM3; source degenerated; low-noise amplifier

I. Introduction

CMOS has become the prevailing low cost technology for radio frequency (RF) integrated circuits due to its dominance in the digital market. However, as digital CMOS scales, the continual reduction in supply voltage will limit the applications of RF CMOS technology due to the low breakdown voltages of the CMOS transistors. Even when the supply voltage, V_d , is less than the breakdown voltage, it is still possible for the source-drain voltage of individual transistors to exceed breakdown due to the large back-emf from inductor components in circuits such as DC-DC converters and RF amplifiers. Here results are presented from metal-semiconductor field-effect-transistors (MESFETs) fabricated using a 0.35 μ m SOI CMOS technology [1,2] with no changes to the CMOS process flow. The Si-MESFETs demonstrate high breakdown voltage combined with good RF characteristics [3-5]. Various figures-of-merit including cut-off frequency (f_T), maximum oscillator frequency (f_{max}), maximum stable gain (MSG), and noise figure (NF) are presented.

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The SOI MESFETs show good depletion mode behavior with threshold voltages close to -0.5V and the drain current following a good square-law behavior above threshold. The parameters for a TOM3 MESFET model [6] have been extracted and have been presented elsewhere [3]. Here, simulation results compared to the measured figures-of-merit are presented. Using the SOI MESFET model, a source degenerated low noise RF amplifier targeting operation near 1GHz has been designed using the simulation tool Agilent Advanced Design Systems [7]. A silicon MESFET was then bonded out to a PCB board and used to demonstrate an LNA operating at 940MHz with a minimum NF of 3.8dB and RF gain of 9.9dB while only consuming 5mW of DC power. The SOI MESFETs show higher breakdown voltages than MOSFETs fabricated on the same CMOS process enabling the RF amplifier to be used at higher operating voltages. Before describing the RF amplifier design and measurements, a summary of the SOI MESFET fabrication and model is presented. More detail can be found in references [3,8].

MESFET Fabrication using A SOI CMOS Process

SOI CMOS has emerged as a successful technology for handset RF power applications. The buried oxide reduces the capacitive coupling to the substrate, which improves power efficiency. The SOI layer provides good isolation that aids in developing efficient integrated designs [9,10]. Also, the highly resistive SOI substrates are useful in forming the low loss passive components on chip.

The prime motivation to fabricate an SOI MESFET was its compatibility with well-established SOI CMOS technologies. Other silicon-based MESFETs have been demonstrated using CMOS compatible process steps, but none of them used a standard CMOS process flow [11-14]. The key step in the MESFET fabrication is the use of the self-aligned silicide (salicide) process to form the Schottky gate [8]. The silicide is patterned using a silicide block step that defines the regions of the Schottky gate. This is done using the same salicide process that is used to form the low resistance source, drain and poly-silicon gate contacts. A cross-section of the SOI MESFET is shown in Fig. 1. The oxide spacers are the PECVD oxide that remains above the MESFET active channel after the silicide block process is complete.

Unlike SOI CMOS, the gates of the MESFET are not self-aligned. The width of the PECVD SiO_2 layer determines the distance of the gate from the source and the drain. The drawn distance from the gate to the source and drain regions is the access length, L_a , as shown in Fig. 1. The limitation on the minimum access length is the lateral diffusion and the lithographic design rules. Based on the application, the access length can be varied to achieve optimum performance from the device. The gate length, L_g , is defined as the drawn distance between the edges of the oxide spacer regions.

II. SOI MESFET RF Characterization and Modeling

Previously, a TOM3 SPICE model has been developed which closely matches the performance of SOI MESFETs and is easily compatible with commercial simulators [6]. A quasi-static approach was taken, with the assumption that the voltage dependencies of the nonlinear circuit elements at RF frequencies is the same as in DC conditions and was assumed valid up to 20GHz. RF measurements were performed with an HP8510C vector network analyzer and 8515A S-parameter test set on the active device as well as equal geometry open-circuit and short-circuit geometries for de-embedding. The IC-CAP modeling system [15], a part of the Agilent EEsof high-frequency electronic design automation (EDA) solutions, was used for writing the extraction routines and then optimizing the first order SPICE parameters. Details of the large-signal and small-signal

model can be found elsewhere [3]. For convenience, the small signal circuit model in Fig. 2 which will be used for the development of the 1GHz amplifier design is shown.

SOI MESFETs fabricated using a conventional low voltage CMOS process have higher breakdown voltages than same process MOSFETs offering advantages such as higher operating voltages for linear RF amplifiers. In order to characterize the device for high voltage applications, it is important to determine the safe operating regions of the device and include their effects into the model. The MESFET demonstrates a soft breakdown beyond which the device still possesses reversible electrical characteristics but is entering a region where any voltage spikes can have a detrimental effect. The drain current injection technique [16] was used to determine the breakdown mechanism in the SOI MESFET [5].

The drain current injection technique was applied to MESFETs of different L_a and the measured breakdown voltages are shown in Fig. 3 [4]. As the access length is increased, the breakdown voltage increases with only a small degradation in the RF performance of the device. This is also illustrated in Fig. 3 where the measured peak cutoff frequency f_T is plotted as a function of L_a . It can be seen that the breakdown voltage increased from 12.5 V at L_a of 0.6 μm to 37 V at L_a equal to 2.2 μm , while f_T only fell from 7.3 GHz to 6.4 GHz. Based on the application, a trade-off between high breakdown voltage and high f_T can be made which follows a 15.3V/ μm and -0.5GHz/ μm change in access length. MOSFETs fabricated on the same technology had rated voltage breakdowns of 3.3V defined by the manufacturer.

Fig. 4 shows the measured (lines) and simulated TOM3 model (symbols) f_T of a 100 μm wide SOI MESFET with L_g of 0.6 μm and L_a of 0.6 μm as a function of drain current. The f_T is dependent on the transconductance and the gate capacitance as:

$$f_T = \frac{g_m}{2\pi C_g} \quad (1)$$

In saturation, f_T is voltage-independent. However, the maximum oscillation frequency f_{max} is voltage-dependent and can be described as [17,18]:

$$f_{\text{max}} = \frac{f_T}{2 \sqrt{2\pi f_T R_G C_{gd} + \frac{R_G + R_i + R_S}{R_{DS}}}} \quad (2)$$

where:

$$R_i \equiv \frac{\partial V_g}{\partial I_g} \quad (3)$$

The input resistance R_i is in parallel with the input gate capacitance, so at a specific frequency, the Q of the network can be determined and R_{gs} can be calculated. Fig. 5 shows the f_{max} for two 100 μm wide SOI MESFETs with L_g of 0.6 μm and L_a of 0.6 μm and 1 μm [4]. Devices with longer L_a showed an increase in gate capacitance and decrease in transconductance which resulted in a lower f_{max} . The maximum available gain (MAG) is defined as:

$$MAG = \frac{\text{Power Available from Network}}{\text{Power Available from Source}} = (K - \sqrt{K^2 - 1}) \frac{S_{21}}{S_{12}} \quad (4)$$

where K is Rollet's stability factor. In the case of the de-embedded MESFETs presented here, at 1GHz the device would be unstable with simple 50Ω terminations leading to $K < 1$ and an undefined MAG. Instead, the maximum stable gain (MSG) can be determined by setting K to borderline stability equal to 1 in (4) resulting in:

$$MSG = \frac{S_{21}}{S_{12}} \quad (5)$$

MSG was extracted from the measured S parameters at 1GHz and compared to the simulated MSG from the TOM3 model (Fig. 6).

Several devices were measured using an automated on-wafer probe system capable of determining gain, NF minimum and optimal load impedances for minimum noise. Specifically Maury Microwave automated tuners coupled with an HP 8970B Noise Figure Meter and Cascade Microtech probe station were used. Measurements of a 0.6μm gate length device were made at several operating points to determine trends and establish the direction of future work. No loss de-embedding of the on-wafer structure was performed and the results are shown in Fig. 7. When the MESFET was biased at 2V (~1.6mA drain current), NF's near 2 dB at 1GHz were achieved which are encouraging results for future work.

With performance levels already acceptable for many short-range RF communication applications, there are still improvements that will be incorporated in future Si-MESFET versions. Reduction in gate and source feed resistance is readily achieved through increased vias and contacts while feeding the device's gate from both ends is a well established means of reducing the minimum noise figure. It is estimated that the NF_{min} will improve by 0.5 to 0.75dB through these simple steps, providing very workable micropower devices with under 2.0dB noise figures.

III. SOI MESFET 1GHZ Amplifier Design Methodology

A source degenerated low noise amplifier topology [19-21] was chosen to demonstrate the silicon MESFET as an RF amplifier. This topology is commonly fully integrated on commercial CMOS processes and serves as a demonstration for a future fully integrated MESFET LNA. At this time, only single Si-MESFET devices have been fabricated and a cascoded structure is unavailable. Benefits of a cascoded LNA topology such as increased reverse isolation will be realized in future Si-MESFET circuitries.

For this work, a target frequency of 1GHz with a drain bias of 2V and a gate bias of 0.2V at 25°C was used based on MSG and power consumption measurements. This frequency was chosen as a demonstration to show RF operation while allowing gain overhead for losses associated with board parasitics and source degeneration. Due to board losses and source degeneration, the MSG will be difficult to achieve, so the bias point was chosen to be several dB higher than our design target of 10dB gain. A single die was bonded out to a PCB board and matching networks with discrete circuit elements were soldered on using a Finetech Rework Station. For the initial design, the input was first matched to 50Ω using the small signal model and then an output match for maximum small signal gain was determined using simulated S Parameters. Initial values for the input matching network were

found using an approach similar to [20]; where an inductance Z_{LS} was added in series to ground at the drain to bring the real part of the input impedance up to 50Ω and another inductance Z_{LG} was added in series at the gate to remove the negative reactance of the gate capacitance. Table 1 shows the extracted small signal parameters at 1GHz for the MESFET model shown in Fig. 2 used for hand calculations.

For a first hand calculation approach, the gate resistance, Miller feedback capacitance and parasitics were neglected resulting in the impedance at the gate Z_{gs} determined by the small signal model gate capacitance C_{gs} (Fig. 2) and the impedance Z_{LS} determined by the added inductance at the source. Looking into the input of the amplifier (Fig. 8A), the input impedance can be determined as:

$$Z_{in \text{ MESFET}} = Z_{LS} + Z_{gs} + g_m Z_{gs} Z_{LS} \quad (6)$$

The real part of the input impedance is therefore:

$$\Re(Z_{in \text{ MESFET}}) = g_m Z_{gs} Z_{LS} \quad (7)$$

where the inductor is used to tune the input to 50Ω . The gate of a MESFET is a Schottky junction with minimal capacitance to resonate with the added input gate inductor. In order to keep the value of the inductor low, a capacitive short Z_{CG} to ground of 400fF was added at the gate which appears in parallel with $Z_{in \text{ MESFET}}$. An additional 100fF was added to C_{gs} to model the parasitics of the pad needed to bond the die out. Once Z_{LS} was adjusted to tune the real part of the input to 50Ω , the inductance Z_{LG} was added in series with the input to tune the imaginary part of the input impedance to zero ohms. The initial estimate for the impedance looking into the circuit can then be calculated as:

$$Z_{in} = Z_{LG} + (Z_{CG} \parallel Z_{in \text{ MESFET}}) \quad (8)$$

resulting in initial values for L_S and L_G of 6.5nH and 43nH respectively. On the final PCB board, C_G , L_S and L_G are comprised mainly of parasitics from the pad capacitances, stray capacitance and bondwire impedance.

The TOM3 MESFET model and calculated circuit elements were then simulated in Agilent Advanced Design Systems to determine the S Parameters of the final circuit. The output network was first simulated with a coupling capacitor and a large inductance in parallel with a de-Qing resistance R_Q of 800Ω to the drain bias. R_Q was used to model the series resistance of the inductor at resonance. After checking the input network for an acceptable return loss at 1GHz, the output was conjugately matched to 50Ω for maximum available small signal gain using the simulated S Parameter S_{22} . An L-match network with an inductor L_M to ground was designed so that the drain of the MESFET could be biased directly through the matching network. Matching capacitor C_M also acts as an RF coupling capacitor.

After initial matching networks were determined, microstrip transmission lines and bondwire models of 1nH/mm and $0.13\Omega/\text{mm}$ were used to simulate the design on an actual PCB board. Additionally, the gate was biased with a resistor of $2\text{k}\Omega$ and 240pF bypass capacitors, C_B , were added at the input of each bias supply to provide RF ground. Circuit elements were modeled with measured S Parameters supplied from respective manufacturers and the board was tuned to operate at 1GHz. Fig. 8B shows the final circuit schematic after tuning.

IV. SOI MESFET 1GHZ Amplifier Measurement Results

After simulation, the board was populated and a MESFET die with gate length of $0.6\mu\text{m}$ and L_a of $0.6\mu\text{m}$ from the same process run as those characterized above was bonded out directly to the traces on a FR4 PCB board. Fig. 9 shows a micrograph of the final board, where the LNA circuit occupies an area of $1.75\text{cm} \times 1.5\text{cm}$ shown by the boxed region. The source inductance L_S was completely achieved with a bondwire which results in a higher Q than surface mount components. S parameter measurements were performed with an HP8510C vector network analyzer with all measurements at 25°C . Initially, S11 and S22 were off in frequency so the inductor L_M was increased resulting in the final measured S parameters shown in Fig. 10. Minima in both S11 and S22 were then around 940MHz, but S11 increased to almost -7dB which although acceptable, is a higher return loss than the targeted S11 < -10dB. One reason for the higher return loss is that the inductance of L_S was lower than expected, resulting in a lower real part looking into the input of the device. As L_S is decreased, a higher power gain, S21, can be achieved because less of the RF signal is dropped across the source impedance. However, increased gain occurs at the expense of input mismatch and the actual output power must be monitored for a maxima.

The TOM3 model simulation results showed a good fit to the S parameter measurements and are shown in Fig. 10 as dotted lines. Initially, simulation results did not match as closely and a more complete model for the SOI parasitic pad impedance (C_{pad} , Fig. 2) had to be incorporated into the circuit simulation for a better fit [22,23]. Fig. 8C shows the model that was fit empirically to the extracted pad capacitance of the die which includes a stray pad capacitance C_{PD} (225fF) in series with the SOI substrate capacitance C_{sub} (50fF) and resistance R_{sub} (2k Ω).

The Rollet stability K-factor was measured and simulated and is shown in Fig. 11. The amplifier shows unconditional stability with $K > 1$ and $\Delta < 1$ across an expanded frequency range beyond intended operation at 1GHz. The power gain, S21, has been measured and simulated as a function of gate bias at 940MHz and is shown in Fig. 12. A peak gain of 9.9dB at a drain bias of 2V and gate bias of 0.3V was achieved. At higher gate biases, the gain rolled off due to the decrease in small signal transconductance at higher drain currents. The -3dB bandwidth of the amplifier was approximately 180MHz (0.85 to 1.03GHz).

A minimum noise figure (NF) of 3.8dB at 940MHz with gate bias of 0.2V was measured and is shown in Fig. 13. The minimum noise figure for a similar die at 1GHz with no external circuitry was measured to be 2.2dB (Fig. 7). The additional off chip tuning elements and transmission lines increase the NF and it is reasonable to expect that a lower noise figure can be achieved if the LNA circuit is more fully integrated into a CMOS process.

The DC power consumption has been measured and shows a close fit to simulated data (Fig. 14). The LNA consumes only 5mW at a power gain of almost 10dB.

The amplifier was also biased at a drain voltage of 6V which is considerably higher than the voltage rating of the MOSFETs on the same process. The amplifiers showed an increase in power gain to 10.3dB at a gate bias of 0.3V, but the power consumption increased ~3X and the NF increased ~0.5dB across different gate biases. Both results are expected due to the increase in bias and channel current. The reason for only a small increase in gain was that the load impedance seen by the amplifier was not changed resulting in a load line with the same slope as that at lower drain bias. The load line was shifted to higher drain bias but still operates within the saturation region which is mainly flat across this bias range. However, operation at a drain bias of 6V demonstrates the MESFETs higher voltage capability.

V. Conclusion

A silicon MESFET has been demonstrated in a commercial CMOS process with no changes to the process flow. An industry standard TOM3 model showed a good fit to measured RF metrics and can be used for the design of high frequency circuit applications. Using the model, an RF low noise amplifier operating at 940MHz was designed and fabricated on a PCB board using a bonded out MESFET. The LNA consumed only 5mW of DC power to achieve a gain of almost 10dB.

The amplifier design topology presented here is commonly used for integrated MOSFET LNAs and future work includes the complete integration of an optimized MESFET LNA to decrease the NF. A slightly larger device would allow for an increase in the gain at lower drain bias currents. At the cost of slightly reduced gain, taking advantage of the depletion mode MESFET and biasing the gate at 0V would eliminate the need for on chip biasing circuitry and reduce the LNA footprint. Silicon MESFETs have recently been demonstrated on a fully depleted SOI CMOS technology [24] and should work on future highly scaled technologies with different silicides such as NiSi.

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Fig. 1. Cross-section of a SOI MESFET showing the oxide spacer function used to define the CoSi_2 regions. Unless noted, drawn dimensions of the multi-fingered DUT are $L_g = 0.6\mu\text{m}$, $L_a = 0.6\mu\text{m}$ and $W = 100\mu\text{m}$ ($5\mu\text{m} \times 20$).

Fig. 2. Small-signal model of a SOI MESFET, previously described in [3].

Fig. 3.
The breakdown voltage and peak cut-off frequency as a function of access length L_a for a 100 μm wide, 0.6 μm gate length SOI MESFET.

Fig. 4. Cut-off frequency as a function of drain current for $V_{DS} = 2V$ (solid) and $8V$ (dashed) for the $100\mu m$ wide SOI MESFET with $L_g=0.6\mu m$ and $L_a=0.6\mu m$. Simulations of f_T using the TOM3 model are shown as closed circles (2V) and open circles (8V).

Fig. 5. Maximum oscillation frequency as a function of drain current for $V_{DS} = 2V$ and $8V$ for two $100\mu m$ wide SOI MESFETs with $L_g = 0.6\mu m$ and $L_a = 0.6\mu m$ (solid lines) and $2.2\mu m$ (dashed lines).

Fig. 6. Measured (symbols) and simulated (lines) of the maximum stable gain (MSG) at 1GHz for the 100 μ m wide SOI MESFET with $L_g=0.6\mu$ m and $L_a=0.6\mu$ m.

Fig. 7. Measured minimum NF (dB) as a function of frequency and gate bias for a MESFET with $L_g=0.6\mu\text{m}$ and $L_a=0.6\mu\text{m}$ at drain biases of 2V (solid lines) and 6V (dashed lines). Closed symbols are for $V_g=0.0V$ and open symbols for $V_g=0.3V$.

Fig. 8. Source degenerated LNA circuit used for the silicon MESFET RF amplifier demonstration board. A) shows the impedances used to tune the board and B) shows the final circuit schematic. Bondwire L_S is used to tune the real part of the input impedance to 50Ω . C) shows the model used to fit extracted data for the die bond pad parasitics.

Fig. 9. Micrograph of final LNA on a FR4 PCB. Inset on top left shows zoomed in view of the die with bond wire connections. The boxed region shows the $1.75\text{cm} \times 1.5\text{cm}$ area required to implement LNA circuit.

Fig. 10. Measured (solid lines) and simulated (dashed lines) S parameters for the 1GHz Silicon MESFET LNA fabricated on a PCB board and biased at $V_d=2V$ and $V_g=0.2V$.

Fig. 11. Measured (solid lines) and simulated (dashed lines) Rollet stability factor K and S parameter determinant Δ , for the MESFET LNA biased at $V_d=2V$ and $V_g=0.2V$.

Fig. 12. Power Gain, S21, measured (solid line) and simulated (closed symbols) of the amplifier as a function of gate bias at an operating frequency of 940MHz. A peak gain of 9.9dB at $V_g=0.3V$ was achieved.

Fig. 13. Measured minimum noise figure of the amplifier as a function of gate bias at an operating frequency of 940MHz. Symbols show measurement points.

Fig. 14. Power consumption of the silicon MESFET LNA as a function of gate bias. Solid line shows measured results while symbols are simulated data using the TOM3 MESFET model.

Table 1
Extracted MESFET small signal model parameters for a drain bias of 2V at 1GHz.

1GHz Extracted Silicon MESFET Small-Signal Model Parameters, Vd=2V									
Vg	Rg	Rs	Rd	Rgs	Rds	Cgs	Cgd	Cds	gm
0.0V	1.505 Ω	43.7 Ω	40.89 Ω	104.3 Ω	5.536 kΩ	135.7fF	24.29fF	46.7fF	5.694mS
0.2V	1.505 Ω	43.7 Ω	40.89 Ω	85.13 Ω	3.873 kΩ	167.7fF	24.86fF	51.83fF	8.056mS