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High-Speed Digital Scan Converter for High-Frequency Ultrasound Sector Scanners

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Abstract

This paper presents a high-speed digital scan converter (DSC) capable of providing more than 400 images per second, which is necessary to examine the activities of the mouse heart whose rate is 5–10 beats per second. To achieve the desired high-speed performance in cost-effective manner, the DSC developed adopts a linear interpolation algorithm in which two nearest samples to each object pixel of a monitor are selected and only angular interpolation is performed. Through computer simulation with the Field II program, its accuracy was investigated by comparing it to that of bilinear interpolation known as the best algorithm in terms of accuracy and processing speed. The simulation results show that the linear interpolation algorithm is capable of providing an acceptable image quality, which means that the difference of the root mean square error (RMSE) values of the linear and bilinear interpolation algorithms is below 1 %, if the sample rate of the envelope samples is at least four times higher than the Nyquist rate for the baseband component of echo signals. The designed DSC was implemented with a single FPGA (Stratix EP1S60F1020C6, Altera Corporation, San Jose, CA) on a DSC board that is a part of a high-speed ultrasound imaging system developed. The temporal and spatial resolutions of the implemented DSC were evaluated by examining its maximum processing time with a time stamp indicating when an image is completely formed and wire phantom testing, respectively. The experimental results show that the implemented DSC is capable of providing images at the rate of 400 images per second with negligible processing error.

Keywords

Digital Scan Conversion; Linear Interpolation; High Frame Rate; Ultrasound Sector Scanner; High Frequency Ultrasound Imaging

1. Introduction

High frequency ultrasound transducers have made it possible to open up new applications including ophthalmic, dermatologic, intravascular, small animal, and molecular imaging [1–4] because of their fine spatial resolution on the order of several tens of micrometers. Among these applications, especially, the cardiac imaging of a mouse requires a fine temporal resolution as well. This is so because the heart rate of a mouse is 5–10 beats per second and thus the frame rate should be at least on the order of 150 to 300 per second or more in order to adequately examine the activities of the mouse heart such as valve movement [5,6]. For the purpose of the mouse heart imaging, therefore, high-speed data acquisition is a pivotal element

and it can be realized by using array transducers with electronic translation. Xu et al. reported an analog beamforming system for 35-MHz linear arrays, which is capable of producing images at up to 100 frames per second [4]. And they claimed that the system can provide much faster frame rate than the current one if microcontroller speed and data transfer rate from the beamformer to a personal computer (PC) are improved. However, the width of images produced in the system with the linear array transducer is too narrow to efficiently examine mouse heart activities. High frequency convex arrays could be a possible solution to the problem because its fabrication is relatively easy compared to phased arrays that requires a fine pitch of less than a half wavelength in order to remove grating lobe artifacts. Kim et al. proposed a design of 20-MHz convex arrays for ophthalmic imaging to increase the field of view in azimuthal direction and stressed that the center frequency of the convex arrays can be increased to around 40 MHz which is the limitation in the current array fabrication technology [7]. Once the convex arrays are available, it might be the best tool examining the mouse heart activities. Without these arrays, however, a high-speed mechanical sector scanner with a single element transducer can be used as an interim tool for the examination of mouse cardiac activities, which is currently capable of providing a frame rate of up to 130 frames per second with a view angle of 22 degrees [8].

Besides the high-speed data acquisition, it is another challenge to develop high-speed signal processing functions to support high frame rate imaging of more than 300 frames per second. This is so because these functions must be capable of providing very fast computational speed and wide bandwidth of data transfer between each functional block. Among the functions, the development of a high-speed digital scan converter (DSC) is crucial to map the acquired echo samples onto the pixels of a monitor because location mismatch between the samples and the pixels is especially serious in the sector scanning.

The simplest way to map echo samples onto pixels is to assign echo samples to the nearest pixels [9]. However, the echo samples are typically more abundant in the axial direction but less in the lateral direction. When the samples are mapped onto pixels, pixels located in between two scanlines may not be assigned with any samples, causing the Moiré artifact [9]. This phenomenon is obvious in sector scanning because pixels located far from a transducer have a less possibility to be assigned with a sample. In sector scanning, therefore, the scan conversion mainly involves data interpolation requiring coordinate transformation of a pixel from Cartesian coordinates to polar coordinates or vice versa. Various data interpolation algorithms were proposed, and their performances were examined [10–15]. Among these algorithms, bilinear interpolation is known as the best algorithm in terms of accuracy and processing speed. However, hardware implementation of this algorithm may be very costly because the bilinear interpolation involves complex operations such as square root and arctangent computations in order to convert pixel positions in a Cartesian coordinate into a polar coordinate, and vice versa [12]. In addition, the interpolation algorithm involves at least four data-fetch operations that require complicated buffer management logic circuits. This high cost for the implementation of the bilinear interpolation is particularly true when the operating speed of DSC is pushed higher and higher because electronic components become more expensive and more sophisticated design is required to meet its timing constraints.

This paper reports a recently developed high-speed DSC that is capable of providing high-frequency B-mode images at a rate of up to 400 images per second of which an image size is 256 by 256 pixels. For the sake of simple implementation, this DSC employs a linear interpolation algorithm that is a simplified version of the bilinear interpolation algorithm, thus allowing a high speed operation in simple and cost effective manner. In the paper, the accuracy of the linear interpolation is examined with the Field II simulation program [16], and it is shown that the linear interpolation algorithm is capable of providing comparable image quality to the bilinear interpolation if a sampling rate of envelope samples is at least four times higher than

the Nyquist rate for the baseband component of echo signals. Experimental results, in addition, verified that the DSC developed provides satisfactory performance for high-speed, high-frequency ultrasound imaging.

2. Linear Interpolation

Bilinear interpolation algorithm is two-dimensional interpolation: the first order Lagrange interpolation [17], called linear interpolation, along radial and angular directions. Therefore, the value of a pixel P in Fig. 1 can be obtained by the following calculations.

$$\begin{aligned} I_i &= \frac{S_1 \times R_2 + S_3 \times R_1}{R_1 + R_2} \\ I_{i+1} &= \frac{S_2 \times R_2 + S_4 \times R_1}{R_1 + R_2} \end{aligned} \quad (1)$$

$$A_p = \frac{I_i \times \alpha + I_{i+1} \times \beta}{\alpha + \beta}, \quad (2)$$

where S_1 to S_4 are the values of samples surrounding the object pixel P , α and β are angular differences between P and two scanlines SL_i and SL_{i+1} , and R_1 and R_2 are radial differences between P and two samples located on SL_i and SL_{i+1} , respectively. I_i and I_{i+1} are intermediate values on two scanlines SL_i and SL_{i+1} , respectively.

Linear interpolation is a simplified version of the bilinear interpolation. Unlike the bilinear interpolation, linear interpolation involves only an angular interpolation given by

$$A_p = \frac{S_1 \times \alpha + S_2 \times \beta}{\alpha + \beta}, \quad (3)$$

where S_1 and S_2 are selected because they are the nearest samples to P along radial direction. Although linear interpolation is easily implemented and reduces the complexity of buffer management logic to fetch stored samples for data interpolation, its accuracy is inferior to bilinear interpolation if the sampling rate in the radial direction is low. If the sample rate along radial direction, i.e., of envelope data is increased, the accuracy of linear interpolation would be improved. Richard and Arthur [13] verified this fact with various B-mode images that if being performed with envelope data over-sampled by a factor of 2 or more, linear interpolation can provide superior image quality to bilinear interpolation with the original data that are sampled to match pixel-to-pixel spacing. This result sheds light on the relationship between the number of samples along radial direction and the improvement of the accuracy of linear interpolation. It, however, does not yield any clues as to the relative accuracy of these two algorithms because the accuracy of the bilinear interpolation can be improved with the over-sampled envelope data as well. Intuitively, bilinear interpolation would have superior or equal accuracy to the linear interpolation if the same number of envelope samples is involved in each processing. In order to determine a suitable sampling rate that makes linear interpolation provide an acceptable image quality, it is necessary to quantitatively compare the accuracy of linear and bilinear interpolation in the situation where the same number of envelope samples is used for the processing.

A comparison of accuracy of these two algorithms was undertaken by using the Field II simulation program [16]. In the simulation, a 40-MHz single element transducer model was used. Its focal depth was 8 mm, F-number was 2.5, and the spectrum had a bandwidth of 40 MHz. Five targets, 1.4 mm apart in the lateral direction along a depth of 8 mm, were scanned by means of the mechanical sector scanning in which the viewing angle was 50 degrees and 181 number of scanlines were obtained. Echo signals were acquired at a sampling rate of 800 MHz and Hilbert transformation was carried out to extract the exact envelope information from

the echo signals. After the ideal envelope detection, the information was logarithmically compressed to a 72 dB dynamic range so that it can be used for each interpolation algorithm.

Once the locations of pixels are transformed from a Cartesian coordinate to a polar coordinate, each pixel has a unique angle and radius. In order to obtain a pixel value without the error caused by both radial and angular interpolations, a transducer can be rotated by the angle of a pixel in a polar coordinate and an envelope sample corresponding to the radius of the pixel among the samples generated at an extremely high sampling rate like 2 GHz can be selected. By repeating the procedure for the entire number of pixels, we can obtain an error-free image. In the simulation, a standard image used for the comparison was created by this manner.

In common ultrasound imaging systems, baseband echo samples obtained by quadrature demodulation are decimated along with the bandwidth of the samples. This is possible because the sampling rate of the systems for digitizing radio-frequency echo signals is much higher than the bandwidth of their baseband counterpart. Decimation can be increased until the new sampling rate satisfies the Nyquist rate for the baseband signals. By doing so, the square root function used to obtain envelope information from the baseband complex signals is given enough time to compute the envelope data and a small amount of memory is needed to store the results. For displaying images on a monitor, the space between two adjacent pixels is also determined so that it can satisfy the Nyquist rate for the envelope signals to avoid the Moiré artifact once an image depth for displaying is chosen. As a result, the simulation was performed with the two pixel-to-pixel spaces of $37\ \mu\text{m}$ and $18.5\ \mu\text{m}$ corresponding to one and two times the Nyquist rate for the baseband signals, respectively. DSC with linear and bilinear interpolation was performed with various factors of decimation, i.e., various sampling rates under the each pixel-to-pixel space. The accuracy of each interpolation algorithm along with a sampling rate was evaluated by computing the normalized root mean square error (RMSE) between pixel values obtained by the each algorithm and exact pixel values. Table 1 shows the normalized RMSE values along with each pixel-to-pixel space.

As indicated above, Table 1 shows that bilinear interpolation is always capable of providing the superior accuracy to linear interpolation even though sampling rate increases. However, the differences between the accuracy of these two algorithms decrease with sampling rate and become below 1 % as the sampling rate approaches to $8f_{\text{max}}$ that is four times higher than the Nyquist rate for the baseband component of the echo signals. The symbol f_{max} is the highest frequency component of the bandwidth of the baseband echo signals. With a high sampling rate, therefore, linear interpolation is capable of providing similar image quality as bilinear interpolation.

Fig. 2 shows point target images with a 72 dB dynamic range obtained by the Field II simulation when the sampling rate is 40 MHz ($2f_{\text{max}}$) and the pixel-to-pixel space is $18.5\ \mu\text{m}$. The images in top, middle, and bottom panels were respectively obtained by the exact solution, DSC with bilinear interpolation, and DSC with linear interpolation. This figure shows that the error from linear interpolation makes the image of the point targets, located in $-2.8\ \text{mm}$ and $-1.4\ \text{mm}$, more blocky whereas bilinear counterpart makes it more blurry. However, the point target image located in the center scanline, i.e., $0\ \text{mm}$ in the lateral direction shows almost similar quality in both cases. As a result, it appears that interpolation error more affects the image of targets located away from the center scanline than these in vicinity of the center scanline. This is easily seen from Fig. 3 illustrating lateral beam profiles of the three point targets located at $0\ \text{mm}$ (top panel), $-1.4\ \text{mm}$ (middle panel), and $-2.8\ \text{mm}$ (bottom panel). The error imposed on the lateral beam profile in the top panel appears to be restricted to below $-60\ \text{dB}$ level for both linear and bilinear interpolations, whereas in the middle and bottom panels it appears that the error exists for the entire profile in both cases. In case of linear interpolation, especially, the off-center lateral beam profiles look like stairs due to the lack of envelope samples, which

make the image appear blocky. However, this problem is alleviated as the sampling rate increases as illustrated in Fig. 4 and Fig. 5 which show point target images obtained with a sampling rate of 100 MHz ($5f_{\max}$) and their lateral beam profiles, respectively.

A sampling rate of 100 MHz is still considered slow for linear interpolation to provide an acceptable image quality, meaning that the difference of the RMSE values of linear and bilinear interpolation should be below 1 %. At this sampling rate, however, the image obtained with linear interpolation (bottom panel in Fig. 4) appears to be much smoother than the previous one. In addition, its lateral beam profiles shown in Fig. 5 become closer to these obtained with bilinear interpolation.

The results suggest that to use linear interpolation to implement DSC operating at a very high speed with the acceptable image quality, the sampling rate of envelope samples should be at least four times higher than the Nyquist rate for the baseband component of echo signals. This requirement can be achieved by either radial interpolation with decimated envelope samples [13] or a very high-speed envelope detector capable of generating envelope samples at the same rate of the sampling clock of a system [18].

3. Implementation of DSC

Fig. 6 illustrates the functional block diagram of the designed DSC with the linear interpolation algorithm. The logarithmic compressed envelope data are sent to one of three line buffers; each line buffer is capable of storing data corresponding to a scanline. Once the two line buffers finish storing the data, scan conversion starts for pixels within a sector scan slice formed by two corresponding scanlines to the line buffers while the other is storing the current envelope data. The pixel address generator (PAG) provides the line buffer read address generator (LBAG) and the fractional angle generator with the indices of pixels within a sector scan slice identified by a left scanline number (LEFT_SL). In Fig. 7, for example, the sector scan slice formed by scanlines SL_i and SL_{i+1} is identified by SL_i located on the left side of the slice. In order to achieve the desired operating speed, LBAG and the fractional angle generator responsible for coordinate transformation are implemented by a look-up table (LUT) method that uses the symmetry property of a sector scan image to reduce the size of LUT.

2.1. Pixel address generator

The generation of pixel addresses corresponding to a given sector scan slice can be also realized by a LUT method. Each pixel belongs to only one among sector scan slices, and the number of pixels within a given sector slice is determined by several factors: number of scanlines, viewing angle of imaging plane, imaging depth, and number of pixels in an image. Once these factors are determined, we can determine which pixels belong to which sector scan slices, so that the space of LUT can be divided by the number of the slices constituting an imaging plane and the each space contains the addresses of pixels within the corresponding slice. With LEFT_SL values indicating each slice, therefore, PAG sends the addresses of pixels within the current sector scan slice to LBAG, the fractional angle generator, and a display memory block.

However, the direct realization of the LUT method requires a large size of memory, i.e., $(N-1) \times M \times \log_2(K_x \times K_y)$ bits, where N is the number of scanlines, M is the maximum number of pixels within a given sector scan slice, and $K_x \times K_y$ is the image size. For the case of a 512 by 512 image and 200 scanlines, for example, the memory size should be 4.7 Mbits where M is obtained by the calculation $(512 \times 512 \div 200)$.

In order to reduce the memory size, the digital scan converter is designed to perform the function of encoding the pixel addresses. Each pixel within a given sector scan slice, called an

effective pixel group, is vertically subdivided into G_0 to G_7 indicated by dotted rectangles in Fig. 7 as an example. Each subgroup has a leading pixel represented by dotted circles. It should be noted that a pixel address in a subgroup can be calculated by a leading pixel address and the object pixel position number in the subgroup. For instance, the address of the object pixel P in subgroup G_4 is obtained by adding its position number of 6 to the Y -axis component of the leading pixel address $X4Y0$, so that the address becomes $X4Y6$. Therefore, both LEFT_SL values and subgroup numbers in each effective pixel group can play the role of indices of LUT. Each entry of the LUT standing for the indices contains a leading pixel address and the number of a subgroup member. The memory size for this LUT strategy is therefore

$$\text{Memory Size (bits)} = (N - 1) \times \frac{K_x}{2} \times \log_2(K_x \times K_y \times K_y). \quad (4)$$

Under the previous condition, the memory size for LUT is reduced from 4.7 Mbits to 1.4 Mbits. Fig. 8 shows an example describing the contents of LUT and its output value for the sector scan slices in Fig. 7. The number of LUT indices is eight because there are eight subgroups. Each entry corresponding to the indices contains a leading pixel address and the number of a subgroup member. For the second index representing subgroup G_1 , its entry contains the leading pixel address $X1Y6$ and four that is the number of G_1 member.

2.2. Coordinate transformer and interpolator

In order to perform coordinate transformation, each pixel constituting an image is assigned a unique address in a Cartesian coordinate as shown in Fig. 9, which is an example of pixel addressing of 256-by-256 sized image. Eight most significant bits correspond to a location in X -axis whereas the other bits a location in Y -axis. For example, hexadecimal 0x8000 in Fig. 9 is composed of 0x80 for a X -axis location and 0x00 for a Y -axis location. The reference column indicates the center in X -axis. An interesting feature in this addressing is that X -axis components of two different pixels equally distant from the reference column are two's complement to each other. In Fig. 9, for example, X -axis components of 0x7F00 and 0x8100 are two's complement, i.e. $0x100 - 0x7F = 0x81$. By using this feature, the size of LUT for coordinate transformation can be reduced to approximately half.

A pixel address provided by PAG is sent to LBRAG and the fractional angle generator to perform coordinate transformation and linear interpolation. The two functional blocks can be straightforwardly implemented by a LUT method. The indices of LUTs belonging to the two functional blocks are the addresses of pixels located on both the reference column and its left side in Fig. 9. The right side pixel addresses are converted into two's complement forms to obtain their corresponding values from the entries for their equal distance pixel addresses on the left of the image plane. Entry values of the LUTs are computed in PC and loaded into the LUTs.

LBRAG plays a role in providing the line buffers with the sample address corresponding to a given pixel address to make the line buffers send the samples to the calculation block. Entries of LUT in LBRAG can be calculated by

$$\text{Sample Address} = \text{round} \left(\frac{\Delta d \cdot \sqrt{(X_j - X_C)^2 + Y_j^2}}{\Delta_{\text{sample}}} \right), \quad (5)$$

where X_j and Y_j represent a X -axis and Y -axis address components of the j -th pixel and X_C is a X -axis address component of reference column corresponding to origin in the Cartesian coordinate. In Eq. (5), Δd is a distance between two successive pixels in horizontal or vertical

directions, Δ_{sample} is a sample interval, and $round(\bullet)$ is a function producing the nearest integer value. Note that the two sample values S_1 and S_2 in Eq. (3) are located at the same address of two different line buffers.

The fractional angle generator has a LUT in which entries are β values in Eq. (3). If the angle of i -th scanline is θ_{SL_i} and the angular difference between SL_i and SL_{i+1} is predetermined value $\Delta\theta$, β can be obtained by

$$\beta = \theta_{SL_i} - \tan^{-1} \left(\frac{X_j - X_c}{Y_j} \right). \quad (6)$$

And α can be simply calculated by

$$\alpha = \Delta\theta - \beta. \quad (7)$$

Therefore, the fractional angle generator consists of LUT containing precomputed β and a subtractor to calculate α .

4. Experimental Results

In order to evaluate the performances of the designed DSC, it was implemented in a single FPGA (Stratix EP1S60F1020C6, Altera Corporation, San Jose, CA) on a DSC board operating at 100 MHz that is a part of a high-speed ultrasound imaging system developed. Echo signals are digitized by a 12-bit analog-to-digital converter (AD9430, Analog Devices Inc., Norwood, MA) at 200 MHz and sent to the DSC board via a low voltage differential signaling (LVDS) bus. The DSC board contains a high-speed envelope detector capable of generating logarithmic-compressed envelope samples at a sampling rate of 200 MHz [18], so that the designed DSC involving linear interpolation is capable of providing acceptable image quality. In addition, the board has a 64-bit, 33-MHz PCI bus controller to transfer pixel data to a display module in a personal computer (PC), which was implemented by software programs written in C++. The display module is responsible for displaying images on a monitor and storing the images in a hard disk of PC. At present, the display module can store one thousand successive images with time stamps indicating when an image data is completely stored in PC memory. In these experiments, a mechanical sector scanner capable of scanning at the rate of up to 130 frames per second was used [8]. The scanner mechanically translates a 40-MHz light-weight single element transducer of which the focal depth is 8 mm and the f-number is 2.5 [19].

The maximum processing speed of the implemented DSC was evaluated by using four-cycle 25-MHz sinusoidal burst signals at the pulse repetition frequency (PRF) of 80 KHz, which were generated by a function generator (33250A, Agilent Technologies Inc., Palo Alto, CA) and fed into the input port of the system. The system treated the burst signals as echo signals. Scan conversion with the signals was performed under the condition where the number of scanlines was 200 and the maximum view angle was 15 degrees. Scan converted images were sent to the display module and stored in a hard disk of PC with a time stamp. The time stamp recorded in a file showed that the maximum frame rate was 400 images per second. This is an obtainable maximum rate with 100-MHz operation clock and 256 by 256 image size. On the other hand, the display rate of the images was 95 images per second due to the limited capability of a monitor. This display rate was obtained by an experiment in which PRF was increased while displaying one out of two images. The maximum PRF without missing an image was 38.5 KHz corresponding to about 190 images per second ($38.5 \times 10^3 \div 200$); thus the maximum display rate was one half of 190 images per second.

The spatial resolution of the implemented DSC was evaluated by wire phantom testing. Fig. 10 shows a wire phantom image consisting of five 20 μm diameter tungsten wires (California Fine Wire Co., CA) separated by distance intervals along vertical and horizontal directions of 1.5 mm and 0.65 mm, respectively. The total scanlines were 108, the scanning angle was 12.8 degrees, and a logarithmic compression with a 60 dB dynamic range was performed. The scan conversion was performed with 2048 samples, so that imaging depth was 7.88 mm. Since the scan conversion started from 4 mm depth, the maximum image depth is 11.88 mm and the third wire image in the vicinity of the focal depth of the transducer, 8 mm, has the best spatial resolution: the -6dB axial and lateral resolution of 48 μm and 103 μm , respectively.

The accuracy of these spatial resolutions was evaluated with the -6dB axial and lateral resolutions computed from RF data which are 45 μm and 110 μm , respectively. In the case of the axial resolution, the implemented DSC degrades it by 3 μm due to interpolation error, but the difference is negligible. On the other hand, the lateral resolution of the DSC is better than the one computed from RF data by 7 μm . This can happen because the DSC performed interpolation along the lateral direction. For the lateral resolution, a -6dB lateral position was determined by averaging two lateral positions located at right before and after -6dB value. After finding the other of -6dB lateral position in the same way, the -6dB lateral resolution was determined by computing the difference between these two -6dB lateral positions. Therefore, the -6dB lateral resolution of the implemented DSC can be narrower than that computed with RF data when no interpolation is performed along the both lateral and axial directions. From these results, consequently, it is seen that the system is capable of achieving accurate results because of its negligible signal processing error.

5. Conclusion

In this paper, a high-speed digital scan converter for high frequency ultrasound sector scanners has been described. It employs a linear interpolation algorithm in which two nearest samples to each object image pixel are selected and an angular interpolation is performed. Since the linear interpolation carries out only angular interpolation unlike bilinear interpolation, coordinate transformation providing interpolation coefficients can be simply implemented compared to the bilinear counterpart. In addition, the linear interpolation involves two data-fetch operations instead of four in the case of the bilinear counterpart, which reduces the complexity of the buffer management logic. These advantages of the linear interpolation enabled us to implement a high-speed DSC in a simple and cost effective manner. In terms of accuracy, however, it is obvious that the linear interpolation is inferior to bilinear one because it does not perform the interpolation along radial direction. If the sampling rate along radial direction, i.e., the envelope sample rate is increased, the accuracy of the linear interpolation would be improved. Through computer simulation with the Field II program, therefore, it has been shown that the linear interpolation algorithm is capable of providing an acceptable image quality if the sampling rate of envelope samples is at least four times higher than the Nyquist rate for the baseband component of echo signals.

The designed high-speed DSC was implemented in a single FPGA on a DSC board that is a part of a high-speed ultrasound imaging system developed. The performances of the implemented DSC were evaluated by experiments in terms of temporal resolution and spatial resolution. The temporal resolution of the DSC was 400 images per second that is applicable to cardiac imaging of the mouse where the heart rate is 5–10 beats per second. And the spatial resolutions of the DSC were 48 μm and 103 μm in axial and lateral directions, respectively. These values are comparable to those computed from RF data which are 45 μm and 110 μm , respectively. As a result, the cost-effective high-speed DSC with acceptable performances would serve as a viable alternative for examining the activities of the mouse heart like valve movement with high-performance high-frequency array transducers.

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Fig. 1.
Conceptual representation of bilinear and linear interpolation.

Fig. 2.

Point target images obtained when a sampling rate is 40 MHz ($2f_{\max}$) and the pixel-to-pixel space is $18.5\mu\text{m}$. The images in top, middle, and bottom panels were obtained by the exact solution, DSC with bilinear interpolation, and DSC with linear interpolation, respectively.

Fig. 3.

Lateral beam profiles of three point targets shown in Fig. 2. Top panel is for a point target at 0 mm in lateral direction and 8 mm in axial direction, middle panel is for it at -1.4 mm and 8 mm, and bottom panel is for it at -2.8 mm and 8 mm.

Fig. 4.

Point target images obtained when a sampling rate is 100 MHz ($5f_{\max}$) and the pixel-to-pixel space is $18.5\mu\text{m}$. The images in top, middle, and bottom panels were obtained by the exact solution, DSC with bilinear interpolation, and DSC with linear interpolation, respectively.

Fig. 5.

Lateral beam profiles of three point targets shown in Fig. 4. Top panel is for a point target at 0 mm in lateral direction and 8 mm in axial direction, middle panel is for it at -1.4 mm and 8 mm, and bottom panel is for it at -2.8 mm and 8 mm.

Fig. 6.
Functional block diagram of designed digital scan converter with linear interpolation.

Fig. 7.

Description of grouping pixels and linear interpolation within two adjacent scanlines SL_i and SL_{i+1} indicated by bold dashed lines. A multiplication sign represents an image pixel. A dotted rectangle represents one of subgroups of the pixel group within the two scanlines. A dotted circle designates a leading pixel in each subgroup. Filled circles on the scanlines represent acquired samples. The multiplication sign in a diamond is an object pixel to linear interpolation. α and β are angular differences between P and SL_i and SL_{i+1} .

Fig. 8.

An example to describe the contents of LUT and its output value. Left scanline number SL_i and a subgroup number constitute an index of LUT. For the sector scan slice in Fig. 7, the number of indices is eight because there are eight subgroups. Each entry corresponding to the indices contains a leading pixel address and the number of a subgroup member. In case of the second index representing subgroup G_1 , its entry contains the leading pixel address X1Y6 and number four. Its outputs are generated by increasing a leading pixel address by one as many as the number of a subgroup member minus one.

_CNT is an upward counter, and DOWN_CNT is a downward counter.

Fig. 9.
Configuration of pixel addressing of 256 by 256 sized image. The reference column indicates the center in X-axis.

Fig. 10. Wire phantom image consisting of five $20\ \mu\text{m}$ diameter tungsten wires of which distance intervals along vertical and horizontal direction are $1.5\ \text{mm}$ and $0.65\ \text{mm}$, respectively.

Table 1

Comparison of accuracy of the linear interpolation and the bilinear interpolation algorithms by computer simulation using Field II program; the accuracy of each algorithm was evaluated with the normalized RMSE between pixel values obtained by each interpolation algorithm and exact pixel values. In this table, f_s is a sampling frequency and $f_{\max}$ is the highest frequency of baseband echo signals of 20 MHz in the simulation.

(a) A pixel-to-pixel space of $2f_{\max}$						
f_s	$2f_{\max}$	$4f_{\max}$	$5f_{\max}$	$8f_{\max}$	$10f_{\max}$	$20f_{\max}$
algorithm	The normalized RMSE					
Bilinear Interpolation	8.56 %	7.40 %	7.30 %	7.21 %	7.13 %	7.12 %
Linear Interpolation	12.19 %	9.46 %	9.00 %	7.86 %	7.72 %	7.40 %
Differences	3.63 %	2.06 %	1.70 %	0.65 %	0.59 %	0.28 %
(b) A pixel-to-pixel space of $4f_{\max}$						
f_s	$2f_{\max}$	$4f_{\max}$	$5f_{\max}$	$8f_{\max}$	$10f_{\max}$	$20f_{\max}$
algorithm	The normalized RMSE					
Bilinear Interpolation	8.77 %	7.08 %	6.68 %	6.38 %	6.36 %	6.28 %
Linear Interpolation	12.79 %	9.21 %	8.89 %	7.12 %	6.63 %	6.55 %
Differences	4.02 %	2.13 %	2.21 %	0.74 %	0.27 %	0.27 %