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A high-precision voltage source for EIT

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Abstract

Electrical impedance tomography (EIT) utilizes electrodes placed on the surface of a body to determine the complex conductivity distribution within the body. EIT can be performed by applying currents through the electrodes and measuring the electrode voltages or by applying electrode voltages and measuring the currents. Techniques have also been developed for applying the desired currents using voltage sources. This paper describes a voltage source for use in applied-voltage EIT that includes the capability of measuring both the applied voltage and applied current. A calibration circuit and calibration algorithm are described which enables all voltage sources in an EIT system to be calibrated to a common standard. The calibration minimizes the impact of stray shunt impedance, passive component variability and active component non-ideality. Simulation data obtained using PSpice are used to demonstrate the effectiveness of the circuits and calibration algorithm.

Keywords

EIT; electrical impedance tomography; voltage source; instrumentation; calibration

1. Introduction

Electrical impedance tomography (EIT) is an imaging modality which displays the spatial distribution of the complex conductivity distribution inside a body. An excitation is applied to electrodes on the body surface, resulting in an electromagnetic (EM) field appearing within the volume. If the excitation consists of one or more currents, the voltages that appear at some or all of the electrodes are measured. If the excitation consists of voltages, then the currents at the electrodes are measured. The inverse problem describing the current-voltage relationship is then solved to determine the complex conductivity distribution that must have been present to produce the measured data set. The ill-posedness of this inverse problem manifests itself through the small changes in surface current or voltage that sometimes result from large changes in the interior impedance distribution. High-precision electronics are needed to apply the excitations and measure the data that correspond to these changes.

For an electrical impedance tomograph with finite measurement precision, distinguishability is defined as the ability to detect an inhomogeneity in a homogeneous background, and is maximized for all conductivities and geometries when currents are applied to the surface electrodes and the resulting voltages are measured (Isaacson 1986). Furthermore, distinguishability is maximized when multiple, independent current sources are used to apply

spatial patterns of currents to the electrodes. Applying current patterns whose eigenvalues match the natural response (modes) of the body being interrogated maximizes the signal-to-noise ratio (SNR) of the resulting data set and therefore minimizes the amount of regularization necessary for the subsequent reconstruction.

Taken together, these two observations suggest that multiple, high-precision current sources are required to maximize the distinguishability and SNR of an impedance tomography data set. While such current sources have been developed for this application (Cook *et al* 1994, Ross *et al* 2003, Cherepenin *et al* 2001, Hartov *et al* 2000), they tend to have limited bandwidth, apply only sinusoidal excitations, and require a large number of high-precision components. The result is an electronics package with a large system footprint, and high component, power and cooling costs.

In contrast, precision voltage sources are generally easier and less costly to implement (Zhu *et al* 1993, Hartov *et al* 2000). However, as mentioned above, applying voltages and measuring currents produces a less optimal EIT system. In an attempt to gain the hardware simplicity of a voltage source along with the optimality of applied currents, we have developed algorithms for utilizing multiple voltage sources to apply a desired current pattern (Choi *et al* 2003). This algorithm takes into account the interaction between the sources which results in the current at any given electrode being a function of the voltages on all the electrodes.

When using a voltage source in EIT, it is necessary to know both the applied voltage and the resulting current with high precision. If it is desired to have the applied voltage remain unchanged for a wide range of load impedances, then it is necessary to have a voltage source with low output impedance. In the case where voltages are being applied to produce specific currents, the applied voltage will be adjusted, generally in an iterative way, to compensate for changes in the load impedance. Consequently, low output impedance is less important than having the ability to precisely measure the actual applied voltage and current.

Below, we describe a voltage source circuit, calibration circuit and calibration procedure for use in EIT (Ross 2003). The source incorporates direct measurement of the applied voltage and measurement of the applied current. Both the calibration procedure and the subsequent application of the source are discussed. The calibration procedure results in a set of calibration factors and parameters that allow the suppression of errors due to stray shunt impedance, passive element values and non-ideal properties of active devices. Since all voltage sources in an EIT system will be calibrated using a single calibration circuit, the approach results in nearly identical performance of all voltage sources.

2. System description

Figure 1 is a block diagram of an applied-voltage EIT system with L electrodes. Each electrode is connected to a circuit that includes a voltage source for generating the applied voltage as well as an ammeter to measure the applied current and a voltmeter to directly measure the applied voltage. A switching network enables a single calibration circuit to be connected to any of the voltage source/ammeter/voltmeter circuits to allow the whole system to be calibrated to a single reference.

Though not shown in figure 1, the voltage sources (with ammeters and voltmeters), switches and calibration circuit each interface to a digital controller which sets the system configuration and collects digital measurements of voltage and current. A series of calibration steps, to be described below, are performed to collect calibration data for each source. Typically, the electrodes are not in contact with a body to be imaged during these calibration steps. The controller utilizes the calibration data to determine actual applied currents and voltages from measurements that are made when collecting data for an EIT image.

3. Circuit topology

Figure 2 shows a common configuration for implementing a voltage source with an integrated current measurement capability. The circuit consists of an operational amplifier unity-gain buffer with a current-sensing resistor, R_{sense} , included in the feedback loop. First consider the case where the shunt impedance, Z_{shunt} , is infinite and the operational amplifier is ideal, having infinite gain, infinite input resistance and zero input capacitance. Under these conditions, the voltage, V_0 , that is applied to the load resistance, R_{Load} , equals the input voltage, V_i . Also, the current delivered to the load, I_{actual} , equals the current through R_{sense} , denoted as I_{sense} . This load current can be determined by measuring V_{sense} and evaluating $I_{\text{sense}} = V_{\text{sense}}/R_{\text{sense}}$.

If the operational amplifier has finite gain, $V_0 \neq V_i$ and it is necessary to directly measure V_0 in a high-precision application. The presence of Z_{shunt} creates a larger problem because it causes I_{sense} to be different from I_{actual} . Z_{shunt} models the capacitance and resistance between the output of the voltage source and ground. Stray capacitance and resistance is introduced by wiring, printed-circuit board traces and the input impedance of the active devices connected to this node, including the impedance between the inverting op amp input and ground in figure 2. Also, the addition of other circuits, such as a voltmeter, connected to the output will insert additional capacitance and finite shunt resistance which can be grouped in Z_{shunt} . In all cases, the presence of finite impedance to ground will result in some of I_{sense} flowing to ground through Z_{shunt} rather than into R_{Load} . The error current is denoted by

$$I_{\text{error}} = I_{\text{sense}} - I_{\text{actual}} = \frac{V_0}{Z_{\text{shunt}}} \quad 1$$

Rearranging, we find that

$$I_{\text{actual}} = I_{\text{sense}} - \frac{V_0}{Z_{\text{shunt}}} \quad 2$$

meaning that knowledge of Z_{shunt} , V_0 and I_{sense} enables the computation of the actual load current value. The voltage source and calibration circuit described below will be able to directly measure Z_{shunt} in order to enable I_{actual} to be determined with high precision.

Figure 3 shows how the voltage source has been augmented to enable calibration. In addition to a number of switches, a buffer amplifier (Buffer) has been added to allow measurement of the output voltage and an instrumentation amplifier (IA) has been added for determining the current flowing in R_{sense} . A calibration circuit has also been added that can measure either current or voltage. In a complete system, there is only one calibration circuit and individual voltage sources can be connected to this calibration circuit, one at a time. It is assumed that the calibration circuit is itself calibrated to a standard, i.e. the current or voltage values that it reports are the true values. However, since all voltage sources are calibrated using a single calibration circuit, errors in the calibration circuit will only impact the overall *accuracy* of the system and not its *precision*.

As is evident in figure 3, the shunt impedance Z_{shunt} includes any stray capacitance along with input capacitance and resistance for the instrumentation amplifier, buffer amplifier and the voltage source itself. Also included is the switch capacitance to ground. The capacitance of solid-state switches tends to be large and vary significantly with switch position and applied voltage. Since switch positions will change between calibration settings and operation setting, low-capacitance reed relays are used in place of solid-state switches. Reed relays present capacitance that varies little with switch position. Additionally, it is assumed that the 'on' resistance of the switches is negligible.

4. Calibration steps

There are several steps for calibrating the voltage source. During the calibration process, the gains of the buffer amplifier and the instrumentation amplifier are measured along with the precise values of R_{sense} and Z_{shunt} . It is assumed that phase-sensitive voltmeters are used to measure the complex voltages V_{vm} , V_{im} , V_{vc} and V_{ic} . Consequently, all gains, voltages, currents and impedance values are assumed to be complex. For example, R_{sense} , though physically a resistance, is represented as a complex impedance, enabling the calibration system to account for any parallel capacitance in the actual implementation. The four steps in the calibration algorithm are explained below.

4.1. Step 1

Figure 4 shows the switch settings for step one of the calibration process in which the complex gain of the buffer amplifier and the complex common-mode gain of the IA are measured relative to the gain of the calibration circuit. In this configuration, switches S_1 , S_2 , S_3 and S_{C2} are closed and all other switches are open. With S_1 closed, R_{sense} is shorted; with S_2 closed, the voltage source op amp (A1) is configured as a unity gain buffer. S_3 and S_{C2} connect the voltage source op amp output, which is also the input to the buffer amplifier and both inputs to the instrumentation amplifier, to the calibration circuit voltmeter.

An input voltage, V_i , is applied and the voltages V_{vc} , V_{vm} and V_{im} are measured. From these measurements, the following gains can be determined:

$$G_{\text{Buffer}} = \frac{V_{\text{vm}}}{V_{\text{vc}}} \quad G_{\text{IA-CM}} = \frac{V_{\text{im}}}{V_{\text{vc}}} \quad 3$$

where G_{Buffer} is the gain of the buffer amplifier and $G_{\text{IA-CM}}$ is the common-mode gain of the IA. In general, the output of an IA is determined by

$$V_{\text{im}} = G_{\text{IA-DM}}(V_+ - V_-) + G_{\text{IA-CM}}\left(\frac{V_+ + V_-}{2}\right) \quad 4$$

where $G_{\text{IA-DM}}$ is the differential gain, $V_+ - V_-$ is the differential input voltage and $\frac{V_+ + V_-}{2}$ is the common-mode input voltage. We are able to determine common-mode gain here because the two inputs to the IA are at the same voltage (connected by S_1), meaning that the differential input voltage is zero.

4.2. Step 2

In the second calibration step, we determine the complex differential gain of the IA, $G_{\text{IA-DM}}$. Figure 5 shows the switch arrangement for this step. As can be observed, switches S_2 , S_3 , S_4 and S_{C2} are closed and all other switches are open. Opening S_1 and closing S_4 produces a voltage drop across R_{sense} when an input voltage, V_i , is applied which appears as a differential input voltage to the IA. The input voltage at the non-inverting input is measured by the calibration circuit and equals

$$V_+ = V_{\text{vc}} \quad 5$$

while the voltage at the non-inverting input is

$$V_- = \frac{V_{\text{vm}}}{G_{\text{Buffer}}} \quad 6$$

The differential input voltage, then, is

$$V_{\text{DM}} = V_+ - V_- = V_{\text{vc}} - \frac{V_{\text{vm}}}{G_{\text{Buffer}}} \quad 7$$

and the common-mode input voltage is

$$V_{CM} = \frac{V_+ + V_-}{2} = \frac{1}{2} \left(V_{vc} + \frac{V_{vm}}{G_{Buffer}} \right) \quad 8$$

Using (4), we can solve for

$$G_{IA-DM} = \frac{V_{im} - G_{IA-CM} V_{CM}}{V_{DM}} \quad 9$$

and, using this result in combination with (7) and (8), we can compute G_{IA-DM} .

4.3. Step 3

Figure 6 shows the configuration for the third step in the calibration process. This step, along with the next step, are used to collect measurements that will be used to determine the values of R_{sense} and Z_{shunt} . Here, switches S_2 , S_5 and S_{C1} are closed and all other switches are open. Operational amplifier AC1 in the calibration circuit is configured as a *current-to-voltage converter* (I - V converter) which, for an ideal operational amplifier, produces an output voltage that equals $-R$ times the input current (current in S_{C1}). Additionally, with an ideal operational amplifier and negative feedback the voltage at the inverting operational amplifier input terminal is forced to equal the voltage at the non-inverting input terminal which is at ground potential. This ‘virtual ground’ in the arrangement of figure 6 results in both ends of Z_{shunt} ideally being at ground potential. When implemented with a real operational amplifier, the circuit will result in a small voltage appearing across Z_{shunt} . Our calibration algorithm will account for this voltage in determining values for R_{sense} and Z_{shunt} .

In this step, the voltages V_{ic} , V_{vm} and V_{im} are recorded. For clarity, these quantities will be denoted as V_{ic_3} , V_{vm_3} and V_{im_3} . In addition, the differential voltage across R_{sense} is computed using

$$V_{DM_3} = \frac{V_{im_3} - G_{IA-CM} \left(\frac{V_{vm_3}}{G_{Buffer}} \right)}{\left(G_{IA-DM} + \frac{G_{IA-CM}}{2} \right)}. \quad 10$$

Since the current through R_{sense} equals the current in Z_{shunt} plus the current in the I - V converter, we can write

$$\frac{V_{DM_3}}{R_{sense}} = -\frac{V_{ic_3}}{R_f} + \frac{V_{vm_3}}{G_{Buffer} Z_{shunt}}. \quad 11$$

4.4. Step 4

Figure 7 shows the switch configuration for the last step in the calibration. This configuration is also employed when using the voltage source after calibration. Here, only S_1 is closed; all other switches are open. A voltage V_i is applied and both V_{im} and V_{vm} are measured and denoted as V_{im_4} and V_{vm_4} . Likewise, the differential voltage across R_{sense} is computed using

$$V_{DM_4} = \frac{V_{im_4} - G_{IA-CM} \left(\frac{V_{vm_4}}{G_{Buffer}} \right)}{\left(G_{IA-DM} + \frac{G_{IA-CM}}{2} \right)}. \quad 12$$

The current through R_{sense} flows in Z_{shunt} , resulting

$$\frac{V_{DM_4}}{R_{sense}} = \frac{V_{vm_4}}{G_{Buffer} Z_{shunt}}. \quad 13$$

4.5. Computation of R_{sense} and Z_{shunt}

In a high-precision application, the deviation of the value of R_{sense} from its nominal value and its variation with aging and temperature will significantly degrade performance. Additionally, R_{sense} may include a capacitive component due to the circuit wiring. To account for this possibility, R_{sense} is assumed to be a complex impedance. Using the results from steps 3 and 4, along with the calibration constants from steps 1 and 2, we can estimate the values of both R_{sense} and Z_{shunt} . Substituting (13) into (11) gives

$$\frac{V_{\text{DM}_3}}{R_{\text{sense}}} = -\frac{V_{\text{ic}_3}}{R_f} + \frac{V_{\text{vm}_3}}{V_{\text{vm}_4}} \frac{V_{\text{DM}_4}}{R_{\text{sense}}} \quad 14$$

which can be solved for R_{sense} producing

$$R_{\text{sense}} = \left(\frac{R_f}{V_{\text{ic}_3}} \right) \left(\frac{V_{\text{vm}_3}}{V_{\text{vm}_4}} V_{\text{DM}_4} - V_{\text{DM}_3} \right). \quad 15$$

Finally, Z_{shunt} can be computed using (13) rearranged as

$$Z_{\text{shunt}} = \frac{V_{\text{vm}_4} R_{\text{sense}}}{G_{\text{Buffer}} V_{\text{DM}_4}}. \quad 16$$

These values of R_{sense} and Z_{shunt} are stored and used to determine the current being delivered to the load in an actual voltage source application.

5. Voltage source operation

In operation, the goal is to have precise measurements of the voltage applied to a load and the current delivered to this load. Figure 8 shows the configuration, with the delivered current denoted as I_{actual} and the applied voltage denoted as V_0 . The voltage at the load, V_0 is determined by

$$V_0 = V_{\text{vm}} / G_{\text{Buffer}}. \quad 17$$

The current being delivered to the load, I_{actual} is found using (2) with V_0 given by (17),

$$I_{\text{actual}} = I_{\text{sense}} - \frac{V_0}{Z_{\text{shunt}}} \quad 18$$

$$= \frac{V_{\text{im}} - G_{\text{IA-CM}} \left(\frac{V_{\text{vm}}}{G_{\text{Buffer}}} \right)}{\left(G_{\text{IA-DA}} + \frac{G_{\text{IA-CM}}}{2} \right) R_{\text{sense}}} - \frac{V_{\text{vm}}}{G_{\text{Buffer}} Z_{\text{shunt}}}. \quad 19$$

6. Circuit simulation

The circuit topology shown in figure 8 was implemented in PSpice to provide data to demonstrate the behavior of the calibration algorithm. A model for an Analog Devices AD8610 operational amplifier was used to implement the voltage source, the I - V converter, and the voltage buffers. The AD8610 was configured as a voltage follower to implement the voltage buffers. A model for a Burr-Brown (Texas Instruments) PGA207 high-speed programmable gain instrumentation amplifier was used for the instrumentation amplifier. This IA was configured for unity differential gain and the model provides a common-mode rejection ratio (CMRR) of approximately 100 dB at dc with a 20 dB/decade slope above approximately 4 kHz. The I - V converter used a feedback resistance-of 1 k Ω . A 50 pF capacitor was added in parallel with R_f to improve stability. The switches, assumed to be reed relays, were modeled as shown in figure 9. The model is based on the specifications for the Coto Technology 9401

surface mount relay. These relays present 1.1 pF of capacitance between each open contact to the coil and 0.2 pF across open contacts. Contact resistance has a maximum value of 0.15ω .

The performance of the calibration algorithm was evaluated by collecting values for V_{vm} , V_{im} , V_{ic} and V_{vc} as needed for each of the four calibration steps defined above (with $R_{Load} = \infty$). Additionally, values for V_{vm} and V_{im} were collected with R_{Load} present. From these data, an estimate of R_{Load} was produced and compared to the actual R_{Load} . All measured voltages are complex and the estimate of R_{Load} is a complex impedance which can be viewed as the parallel combination of a resistance and capacitance, where the capacitance can be positive or negative and, for the simulation, ideally equals zero. Separate estimates for R_{Load} were generated for various instances of the voltage source having different values of Z_{shunt} and/or R_{sense} . The calibration circuit was not changed at any time in order to accurately model the case where multiple voltage sources, each having somewhat different properties due to component variation and differences in physical layout, are calibrated using a single calibration circuit.

The parameters for the three test cases are shown in table 1. The shunt impedance, Z_{shunt} , is modeled as the parallel combination of R_{shunt} and C_{shunt} . Case 1 is a reference case, having a R_{sense} with the nominal value of 1 k and a significant capacitive component to Z_{shunt} . Case 2 is used to illustrate the ability of the calibration algorithm to compensate for the variation in the true value of R_{sense} from the nominal value. Case 3 has a substantially different value for Z_{shunt} and is used to illustrate the ability to compensate for differences in shunt impedance.

6.1. No calibration

Figure 10 shows the error in the estimated load impedance when the three voltage sources, i.e. the three cases in table 1, are operated without calibration. R_{sense} is assumed to be equal to its nominal value of 1 k, the IA is assumed to have unity differential gain and zero common-mode gain, the voltage buffer is assumed to have unity gain, and Z_{shunt} is assumed to be infinite. The load impedance is a pure resistance of value $1 k\omega$.

Figure 10(a) shows error in the estimated load resistance. At low frequencies, the errors for Cases 1 and 3 are small (approximately -0.08ω and -1ω , respectively) due to the fact that R_{sense} is equal to the assumed value of 1 k ω and the primary source of error is R_{shunt} (10 M ω and 1 M ω , respectively) being in parallel with the load. The error for case 2 is approximately -90ω since R_{sense} is actually 1.1 k ω . At high frequencies, the error increases for all cases due to gain roll-off in the IA and voltage buffer as well as the presence of C_{shunt} . None of the sources is able to provide good estimates of the load resistance at 1 MHz.

Figure 10(b) shows the error in estimated load capacitance. Since the actual load capacitance is zero, the error reflects the actual measured load capacitance. The errors are large and vary with both R_{sense} and C_{shunt} . Note that the capacitance that is observed is *smaller* than C_{shunt} as a result of the limited bandwidth of the IA and voltage buffer.

6.2. Full calibration

Here, we consider the performance with *full calibration*, meaning that the calibration circuit itself has been calibrated. Using PSpice, we found the complex transimpedance and complex gain of the I-V converter and voltage buffer, respectively, in the calibration circuit. The transimpedance measurement is made with the 50 pF compensating capacitor in parallel with R_f in the I-V converter. The values of transimpedance and complex gain were then used to correct the measured values of V_{ic} and V_{vc} to give accurate representations of the voltage and current seen by the calibration circuit.

Figure 11 shows the estimated load resistance and capacitance with full calibration. Now, there is only a small error in the estimate of the load resistance at low frequencies ($<0.5 \text{ m}\omega$) and a few ohms of error at high frequencies. It is important to note that the error at high frequencies is nearly the same for all three cases. The errors in the estimate of the load capacitance are generally less than 0.2 pF, though they are somewhat higher at low frequencies.

The performance of the algorithm is limited somewhat by the imperfect virtual ground presented by the I - V converter. The analysis leading to (15) takes into account the current through Z_{shunt} that results from having a nonzero voltage across it, it does not account for current that flows through the input and stray capacitance between the input of the I - V converter and ground. Consequently, the I - V converter will provide a low value for the current.

6.3. Relative calibration

In practice, the calibration circuit may not be perfectly calibrated. A feature of the calibration algorithm is that all voltage sources are calibrated using the same calibration circuit, so while errors in calibration circuit calibration will impact the *accuracy* of the voltage sources, it should not impact their *precision*. To illustrate this point, the voltage sources were calibrated using a completely uncalibrated calibration circuit. In the calibration algorithm, the I - V converter is assumed to have a frequency independent transresistance of R_f , i.e. the 50 pF compensation capacitor is not considered, and the voltage buffer is assumed to have a gain of unity.

Figure 12 shows the result with an uncalibrated calibration circuit. The absolute error in the estimate of the load resistance is small at low frequencies since R_f actually equals the assumed value of $1 \text{ k}\omega$. At high frequencies, the absolute error is much larger due to the uncalibrated frequency response of the calibration circuit. The spread in the error in the estimate of the load resistance, however, is very small at low frequencies ($\approx 0.5 \text{ m}\omega$) and somewhat larger ($\approx 0.5\omega$) at high frequencies. The estimate of the load capacitance shows a bias of approximately -50 pF. This bias is due to the fact that the I - V converter uses a 50 pF capacitance in parallel with $R_f = 1 \text{ k}\omega$ but, in the calculations, the transimpedance of the I - V converter is assumed to be frequency independent. The calibration algorithm attributes this RC time constant (with a sign inversion) to the load resistance. Varying the load resistance results in a change in the estimated load capacitance which maintains this same RC time constant. The spread of the estimated capacitance values is less than 0.1 pF across the frequency range shown.

Generally, the calibration circuit would be calibrated, though imperfectly, resulting in smaller errors in accuracy than those observed in figure 12. However as figure 12(b) shows, even with large errors in accuracy, the relative precision of the voltage sources which are all calibrated using the single calibration circuit remains high.

7. Discussion and conclusions

The results obtained using data from PSpice demonstrate the ability of the calibration system to determine the calibration parameters needed for high-precision voltage source performance. If the calibration circuit is properly calculated, the calibrated voltage sources will also be highly accurate. If the calibration circuit is imperfectly calibrated, the accuracy of the calibrated voltage sources is also imperfect but all sources maintain a high relative precision, since all sources are inaccurate in the same way. In an EIT system, this relative precision of the sources is much more important than the accuracy of the sources. If, for instance, the measured currents at each voltage source are scaled by a single common scaling factor, i.e. the system has high relative precision but does not have high accuracy, the impedance values in the resulting EIT image would also be scaled but the image itself would not be distorted. If, on the other hand, the measured currents at each voltage source are scaled by different scaling factors,

representing the case of low accuracy and low relative precision, the image itself would be distorted.

One limitation of the calibration system described here is that it is not capable of fully compensating for the cables that connect remote electrodes to the EIT system, even when the calibration process is performed with these cables attached. In particular, the series impedance due to coupling capacitors (used to dc-isolate the electrodes from the EIT system for patient safety) and the series resistance and inductance of the cables are not estimated. However, the shunt capacitance presented by the cable is accounted for by the algorithm. In practice, a separate calibration process, using precision load impedances, is used to estimate these additional parameters. Since it requires the application of several precision load impedances at the electrode end of the cables, this second calibration process cannot be easily automated.

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Figure 1.
Block diagram of an applied-voltage EIT system.

Figure 2.
Voltage source with current measurement capability.

Figure 3.
Voltage source designed to allow precision voltage and current measurements.

Figure 4.
Switch setting for calibration step one.

Figure 5.
Switch settings for calibration step 2.

Figure 6.
Switch settings for calibration step 3.

Figure 7.
Switch settings for calibration step 4.

Figure 8.
Configuration for applying the voltage source.

Figure 9.
Reed relay model. $R_s = 0.15\omega$ when the switch is 'on' and $1\text{ G}\omega$ when the switch is 'off'.

Figure 10.
Error in load impedance estimation without calibration: (a) resistance error and (b) capacitance error.

Figure 11.
Error in load impedance estimation with full calibration: (a) resistance error and (b) capacitance error.

Figure 12.
Error in load impedance estimation with relative calibration: (a) resistance error and (b) capacitance error.

Table 1

Parameters for the three test cases.

	R_{sense} (k Ω)	R_{shunt} (M Ω)	C_{shunt} (pF)
Case 1	1	10	150
Case 2	1.1	10	150
Case 3	1	1	300