ANOTHER SOLID STATE TIMER¹JOHN W. TAPP AND FOGLE C. CLARK²

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Solid state timers offer a number of advantages over synchronous motor driven timers or capacitor timed relays. They are inexpensive. The timed interval can be made independent of both the duration of the initiating pulse and the load resistance, and a wide range of intervals can be obtained with small components. A timer circuit in which the timed interval is initiated by application of +24 v dc and the load is energized at the end of the timed interval has been described by Saslow and Markowitz (1964). For convenient use with operant equipment in which all switching is performed on -24 v dc, this paper describes a solid state timer in which the timed interval is initiated by -24 v dc and which produces -24 v dc as an output for the duration of the timed interval. This timer will drive loads of varying resistance without appreciable effect on the duration of timed intervals. Since both input and output are -24 v dc, the circuit can be built into a small plastic box with color-coded leads and patched into a program where needed. In this application, an external relay whose contacts transfer for the timed interval is used as a load. Alternatively, the timer, together with a self-contained output relay can be wired onto a clip-on programming panel. In this case, the addition of a tap switch and several timing capacitors provides for the selection of various intervals on the front panel. The circuit may also be wired directly onto the feeder control relay in an experimental cage, providing a fixed duration magazine cycle following each

operate pulse to the feeder circuit. The total cost of parts for the circuit, less output relay, is under \$5.50 for a single time interval, and only slightly more for selection of a number of intervals.

Fig. 1. Solid state timer circuit. X_1 — (PNP) 2N414; X_2 — (NPN) 2N1102 (use heat sink); C — timing capacitor, 5% tolerance, values for various intervals indicated in text; R_1 — 15 K trimpot; R_2 — 27 K; R_3 — 15 K; R_4 — 3.9 K; R_5 and R_6 — 150 ohms; D_1 and D_2 — 200 ma silicon diodes.

The circuit is shown in Fig. 1 and functions as follows: when ground (-24 v dc) is placed on the junction of R_1 and C, the capacitor charges instantaneously and the base of transistor X_1 is forward biased so that X_1 conducts. When ground is removed from the operate terminal, C discharges through R_1 , R_2 , and the base to emitter resistance of X_1 . When C has discharged to a point insufficient to maintain the forward bias on X_1 , the transistor cuts off completing the timing cycle. The diode, D_1 , prevents discharge of C through any other circuits which may be patched to the operate terminal.

The second stage circuit isolates the timing circuit from the output load, preventing loading from affecting the timing cycle. In addition, the use of an NPN transistor (X_2) in the second stage allows the output load to be operated by application of -24 v dc (ground). When X_1 is conducting, its collector is at a voltage determined by R_3 , R_4 , and the base

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to emitter resistance of X_2 (10 v with the indicated circuit values). This voltage, applied through R_4 , forward biases X_2 , which conducts. X_2 operates the load relay (RY), which remains operated until the end of the timing cycle. When X_1 is not conducting, its collector is at ground, X_2 is cut off, and the load is de-energized. The diode, D_2 , in the collector circuit of X_2 prevents damage to the transistor from inductive loads.

Resistors R_5 and R_6 form a voltage divider which provides + 12 v dc for transistor X_1 . Operation of this stage from 12 v increases the life of X_1 and allows the use of smaller capacitors with lower working voltages.

The following values of the capacitor C will give the indicated time intervals:

1.5 mfd	—	0.5 sec
3.5 mfd	—	1.1 sec
5 mfd	—	1.5 sec
10 mfd	—	3.0 sec
25 mfd	—	7.5 sec
50 mfd	—	15 sec
100 mfd	—	30 sec
150 mfd	—	45 sec
200 mfd	—	60 sec

These times are accurate within $\pm 3\%$ for the shortest two intervals and $\pm 2\%$ for the remaining intervals. The given times are for closure of the normally open contacts of a Clare Type J 500 ohm relay with three sets

of springs. Use of a different 24 v relay affects the timed interval only insofar as operate and release characteristics of the relay are concerned and, in general, does not influence timing error. The trimpot, R_1 , in the first stage timer circuit is provided to adjust the timer precisely and to compensate for changes produced by the use of different output relays. The relationship between the values of C and duration of the timed interval is linear provided close tolerance capacitors are used.

One precaution should be observed in employing this circuit. The onset of the timed interval is simultaneous with the application of an external operate pulse. The capacitor C does not begin to discharge until this pulse is removed. Hence, input operate pulses should be short with respect to the interval being timed, and should be of uniform duration if stability of the timed intervals is to remain within the limits indicated above. For most applications this is unimportant and an ordinary relay pulse former output will suffice for initiating the interval. An electronic or electro-mechanical pulse former could, of course, be added to the unit at slight additional cost.

REFERENCE

- Saslow, M. G. and Markowitz, H. An inexpensive and simple solid state timer. *J. exp. Anal. Behav.*, 1964, 7, 150.