TECHNICAL NOTE

AN ELECTROMECHANICAL ANALYZER USING
HISTOGRAM TECHNIQUES

In behavioral studies it is often necessary to classify events and store the number of events occurring in each classification. The classification requirements may be either functions of amplitude (*i.e.*, intensity, force, peaks, *etc.*) or time (*i.e.*, duration, interval, *etc.*). The following describes an analyzer capable of classifying events according to their duration, interval, or time of occurrence, and storing and displaying the number of such events in each classification.

The analyzer consists of input shapers, functional logic control circuits, a clock divider, flip-flop counters, diode logic converters and electromechanical counters. Figure 1 is a simplified block diagram indicating the basic blocks required. A 60-cycle signal from the power supply is used as a reference frequency for all time derivations. The 60-cycle signal is gated to the input of a series of divider circuits which produce selectable clock times of 0.1, 0.2, 0.4, 1, 2, 4, and 10 sec. The time selected will determine the bin width for each classification. Thus, if 0.2 sec is selected, the first classification will be from 0 to 0.2 sec, the second from 0.2 to 0.4 sec, the third from 0.4 to 0.6 sec and so on.

The output of the clock divider (which determines the bin width) is counted by the address generator in a binary fashion. The number of stages used in the address generator will determine the total number of

bins. In this case, five binary stages are employed, thus permitting 32 successive classifications (0-31). The unit constructed and used here contained only 31 classification as a matter of convenience and choice. The five-line binary code of the address generator is decoded by the diode logic converter to 31 lines. A sixth line into the logic converter connects the count input to all 31 gates.

The logic converter is made up of 31 "AND" gates, each having six inputs. As the address generator counts the selected clock frequency, each AND gate is enabled sequentially. The first AND gate is enabled from 0 to 0.2 sec, the second AND gate is enabled from 0.2 to 0.4 sec, *etc.* If an input event occurs, it completes the enabled AND gate and produces a level change at the output of the AND gate. Each AND gate is connected to a driver and then to an electromechanical

Fig. 1. Simplified block diagram.

counter. The level change at the output of the AND gate triggers the driver, which causes one count to be registered by the counter.

If the clock and count input are selectively controlled, the type of analysis can be selected. The function control block serves this purpose. One mode of operation is interval analysis. In this mode the first input event causes the clock divider and address generator to reset momentarily and then to begin counting from zero as described above. Each AND gate is then successively enabled for the period of time selected (for instance 0.2 sec). The second input event completes the enabled AND gate and a count is registered in the corresponding channel. The channel in which a count is registered is thus a measure of the elapsed time, in 0.2-sec increments, since the first input event occurred. The second input event also causes the clock divider and address generator to be reset momentarily, and a new counting and enabling sequence is again initiated.

Another useful mode of operation is duration analysis. In order to classify each input event according to duration, the clock is turned on only during the event. The inhibit line thus inhibits the gate connected at the input of the clock divider during all other times. The leading edge of each input event is used to reset the clock divider and address generator momentarily as described above. As the count progresses from zero, each AND gate is again enabled as before. However, the clock divider is inhibited upon completion of the input event causing the address generator to stop. Thus, only one AND gate (which corresponds to duration of the input event) is held in the enabled state. The trailing edge of the input event is used to generate a count pulse which then completes the AND gate, and one count is recorded in the corresponding channel. The next input event begins the complete cycle again by (1) resetting the clock divider and address generator, and, (2) completing the gate at the input to the clock divider for the duration of the input event.

A third useful mode of operation is simple time analysis. In this mode, input events are classified according to their time relationship with respect to an initial reference, usually a stimulus. The time reference is connected to the start input which causes the address generator and clock divider to be reset momentarily, starting the count from zero, as described above. The start input simultaneously opens the gate at the input of the clock divider to begin the counting sequences. Once again the AND gates are sequentially enabled. If an input event occurs, it is counted and stored in the channel corresponding to the AND gate enabled at that time. However, no reset is generated and the AND gates continue to be sequentially enabled. If another input event occurs it is counted and stored in the corresponding succeeding channel. In this way all channels are sequentially enabled, and if an input event occurs at any point along the scanning sequence, it is counted and stored in the channel enabled at the time of its occurrence. The scanning continues until the last channel is enabled or until a new start signal is received which begins a new sequencing cycle.

In all modes one of the AND gates in the logic converter is used as a signal to inhibit the clock gate.

Usually the last AND gate (32nd) is selected for this purpose which provides a means for obtaining an overflow channel. Thus, if the enabling sequence, as described above, should continue to the last channel before another input or start signal occurs (which would reset the clock divider and address generator) the clock is inhibited. This holds the last AND gate enabled and the next count signal will be stored in the last channel. In this way 31 channels are obtained according to the above descriptions, plus a 32nd channel of overflow events.

One other counter is provided which accumulates the total number of inputs classified. Although this same number can be obtained by adding the total accumulations of all counters, it is convenient and simple to totalize inputs as the analysis proceeds. Furthermore, the accumulated total provides a method of checking the resultant histogram to make certain that all inputs were indeed classified and stored in only one bin.

The input event is converted to a standard 50-msec pulse by the delay multivibrator (DM), although the electromechanical counters will operate from a 25-msec pulse. Thus, if the clock causes the divider to advance one step during the 50-msec input-event time, the event may be recorded in the adjacent bin. There is little chance of missing a count completely since the resolution required for counting is only 50 microseconds. It would be necessary for the clock divide to advance exactly at the center (± 25 microseconds) of the 50-msec pulse to be missed.

It is also remotely possible that a second event may be missed if it occurs during (or immediately after) reset. However, input rates are limited to 20 per sec by the maximum counting rate of the electromechanical counters, and the reset pulse is very short (only 50 microseconds) by comparison.

Figure 2 is a detailed logic diagram indicating all of the necessary logic elements, interconnections, and controls. The complete logic assembly is contained in two card cages mounted behind the control panel 8 $\frac{1}{2}$ in. high. The counters are also mounted on an 8 $\frac{1}{2}$ -in. panel. The logic cards employed require plus and minus 12 v regulated while the counters and indicator lights require 6 v (unregulated). The power supplies are housed behind a 5 $\frac{1}{2}$ -in. panel. It is estimated that the entire analyzer could be assembled in two weeks by one technician.

As indicated in Fig. 2, all inputs are buffered by a reed relay since it was found that direct electrical connections to the Schmitt triggers greatly increased the chances of false triggering. A relay is also provided as an output from the clock. This provides a means for synchronizing other equipment that may be used in programming.

Several analyzers have been in use for more than a year. One application has been in conjunction with another similar histogram analyzer where duration and force of lever presses have been classified simultaneously. The resultant data indicated force-duration histograms for the same time interval. Other applications have included interresponse time analysis and stimulus-response time analysis. The latter analysis is provided by starting the analysis (in the time histogram mode) by triggering the start input with each stimulus.

Fig. 2. Complete detailed logic.

Each response is then recorded as one count in the bin corresponding to the time elapsed since the previous stimulus. Each stimulus resets the start and the process is repeated. Another application is to record responses per-unit-time. This is accomplished in a similar manner (time mode) by selecting the bin width to be large (perhaps 10 sec or 1 min). Thus, the number of responses per bin is accumulated, for each bin, as the address generator sweeps from 0 to 31.

The estimated cost of this unit is \$3000, which includes labor. Relay logic would be cheaper, costing between \$1500 to \$2000. However, speed, reliability, and size would be sacrificed. As an example, the reset time of a relay is in milliseconds where this analyzer resets in microseconds. Other units, such as the Lehigh Valley, 1567 Response Time accumulator and the Grason-Stadler Multi-Class Time analyzer were higher priced, but have been discontinued by the manufacturer. However, Lehigh Valley has a new modular

system priced at approximately \$3900 for a single mode (time). There is also the Nuclear-Chicago 7100 which costs \$9800 and includes 400 bins, but their equipment is designed for high speed analyses and does not lend itself to behavioral data.

Although emphasis was placed on economy and versatility, similar design approaches may be used for larger and faster units. The maximum input rate is determined by the maximum counting rate of the electromechanical counters. Counters capable of 40 counts per sec are available although 10 counts per sec is sufficient for most applications. All other modules are standard digital logic cards available from many different companies.

VINCENT CAGGIANO
LEE FALLON
Walter Reed Army
Institute of Research