TECHNICAL NOTE

*A METHOD OF INTERFACING A SMALL COMPUTER
WITH PSYCHOLOGICAL EXPERIMENTS¹*

The increasing use of computers in behavioral research (Uttal, 1968; Borko, 1962; Weiss, Laties, Siegel, and Goldstein, 1966) raises the problem of how to accomplish an interaction between the computer and the experimental environment. Two of the commonly faced problems are: (a) how to convert switch or relay closures into precisely defined electrical pulses; and (b) how to convert the pulses originating in the computer into outputs capable of energizing lamps, relays, solenoids, or other external devices.

The interface described in this report is similar to the one described by Ciofalo, Tedford, Goldberg, and Dodge (1968), but is unique in that it employs a mixture of BRS-Foringer digital logic computers (Digibits)² and standard Digital Equipment Corporation modules (Flip Chips) as the intermediate logic between the computer circuitry and the experimental environment. The BRS-Foringer modules were employed for two reasons. First, a large number of these logic cards was available in our laboratory, and secondly, use of the logic cards as buffer storage devices and timers relieved the computer of some of its tasks (see below).

The computer system in the authors' laboratory currently consists of a PDP-8/I computer with 4096 words (12 bits per word) of memory, an AX08 Laboratory Peripheral (DEC), and the interface described below. The PDP-8/I is connected to each of two physiological psychology research laboratories by composite cables consisting of 15 fifty-foot lengths of RG62 coaxial cable (Belden). These cables are connected to the computer through a 16-pin connector (Amphenol) and to the BRS-Foringer modules by connections on the rear of a Mac-Panel receiver.

The interface for each laboratory permits 10 digital inputs to the computer and provides five separate output pulses compatible with the Digibit Logic. A simplified schematic diagram of the interface is presented in Fig. 1. Each switch in the environment sets an appropriate bit (flip-flop) in an input register external to the computer. In the computer program a single instruction transfers, in parallel, the input register into the 12-bit accumulator of the PDP-8/I. Which switches

are closed, if any, is determined by a subroutine that tests the accumulator and provides a program branch to service routines for each input. Also, each bit of the input register may be cleared individually. The accumulator is loaded with a word having the appropriate bit set to logic one, and when the clear instruction is issued, the corresponding bit in the input register is set to logic zero, leaving the other bits unaffected.

The accumulator is also used to control the interface outputs. BRS-Foringer relay driver cards are controlled by flip-flops in a second external register, the output register. If one wants to turn on a particular external device wired to a relay driver, the accumulator of the PDP-8/I is loaded with a word that has the appropriate bit set to logic one. A single output command is issued and the corresponding flip-flop in the external register and the relay driver are turned on. In a similar manner, to turn the device off, the accumulator is loaded with a word having a zero in the same bit and issuing a different output command. This resets the flip-flop and turns the relay driver off.

More specifically, the Digibit modules are used to shape environmental switch closures into a brief (25 microsecond) pulse. The initial phase of the input interface converts the Digibit pulse (-12 to 0 v) into a Flip Chip pulse of 0 to -3 v. This is accomplished by a W511 module that limits the excursion from 12 v to 3 v and also inverts the polarity of the input pulse. To maintain logic polarity, the R107 module inverts the W511 output into a positive going -3 to 0 v pulse which sets one bit of a R203 flip-flop register. The R203 output is gated through a R123 input buss gate into the input mixer (IM) which feeds the accumulator of the PDP-8/I. Gating is accomplished by a W103 device selector. The W103 examines bits 3 to 8 of the computer's memory buffer register (BMB) whenever the operation code is 6. If bits 3 to 8 match the unique code that the W103 is prepared to accept, any one, or any combination, of three input/output pulses (IOP) is delivered to associated device. Which of the three pulses is delivered, is determined by bits 9 to 11 of the memory buffer register. For example, when the instruction 6412 is issued, IOP 2 on device 41 is delivered. This pulse enables the R123 gate (see Fig. 1), thereby transferring the contents of the input register through the input mixer into the accumulator. Similarly, when the command 6411 is given, the W103 sends a pulse to clear the input register through a gate on each flip-flop. This gate is enabled only if a corresponding bit in the accumulator is set to logic one. The contents of the accumulator are continuously available on the buffered accumulator (BAC) lines of the input/output (I/O) buss.

A second W103 device selector controls output gating. Instruction 6401 sets to logic one any bit in the output

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²Modules of other manufacturers were unavailable for testing, but published specifications indicate that Lehigh Valley solid state modules may be used in place of the Digibits. Grason-Stadler modules may also be used, but a slight modification of the interface would be required.

Fig. 1. Block diagram of the computer interface showing one of the 10 inputs and one of the five outputs.

register whose gate is enabled by a logic one level from a corresponding bit in the accumulator (see Fig. 1). When the instruction 6402 is issued, any bit in the output register whose corresponding bit in the accumulator is set to logic zero, will also be set to logic zero. The complementary output of each flip-flop in the output register drives a W600 negative output converter clamped at -12 v. The complementary output of the R202 is used because the W600 not only boosts the signal from 3 to 12 v but also inverts it. The W600 output can be used to drive any of the Digibit modules.

This interface has been in use in our laboratory for approximately 2 yr and has proven quite reliable. Thus far, only two disadvantages have been noted. First, since the standard 25-microsecond Digibit pulse is quite long compared to the 1.5-microsecond cycle time of the PDP-8/I, the input register cannot be cleared immediately after being read into the computer. Accordingly, software provision must be made to wait at least 25 microseconds before attempting to clear the buffer. Secondly, since Digibits are designed to accept rates of 40 KHz, consecutive pulses from the computer must be software retarded not to exceed this rate.

However, the relatively slow speed of the Digibits is not a problem in most psychological experiments, and these disadvantages are, in our opinion, outweighed by several factors. For example, the Digibits may be used to: (1) handle fixed time intervals such as the 50-msec pulses required to operate feeders; (2) serve as secondary buffers if devices must be held on or off for more than several seconds; (3) multiply the output capability of

the interface by decoding serial pulses on one output line into unique codes capable of energizing several different devices; and (4) program the initial phases of behavioral training, thereby freeing the computer for other uses. With the Digibit portion of the interface handling most of the time-consuming behavioral functions, the computer is free to sample several channels of analog inputs, store and process physiological and behavioral data, or generate oscilloscope displays of experimental results.

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