A Study on Electrical Reliability Criterion on Through Silicon Via Packaging

Ben-Je Lwo
Department of Mechanical and Aerospace Engineering,
Chung-Cheng Institute of Technology,
National Defense University,
Tao-Yuan 335, Taiwan
e-mail: lwob@ndu.edu.tw

Kuo-Hao Tseng
Department of Mechanical and Aerospace Engineering,
Chung-Cheng Institute of Technology,
National Defense University,
Tao-Yuan 335, Taiwan

Kun-Fu Tseng
Department of Multimedia and Game Science,
Asia-Pacific Institute of Creativity,
Miao-Li 351, Taiwan

Three-dimensional (3D) structure with through silicon via (TSV) technology is emerging as a key issue in microelectronic packaging industry, and electrical reliability has become one of the main technical subjects for the TSV designs. However, criteria used for TSV reliability tests have not been consistent in the literature, so that the criterion itself becomes a technical argument. To this end, this paper first performed several different reliability tests on the testing packaging with TSV chains, then statistically analyzed the experimental data with different failure criteria on resistance increasing, and finally constructed the Weibull failure curves with parameter extractions. After comparing the results, it is suggested that using different criteria may lead to the same failure mode on Weibull analyses, and 65% of failed devices are recommended as a suitable termination for reliability tests.
[DOI: 10.1115/1.4032932]

Keywords: TSV (through silicon via), reliability criterion, 3D packaging

1 Introduction

Through silicon via is a key technology for the 2.5*D* and 3*D* electronic packaging since it has a number of the advantages, including shorter electrical connections, reduced form factor, higher density, lower power consumption, and the capability of heterogeneous integrations. Despite these improvements, an accurate and efficient reliability analysis methodology on TSV structures is needed before the new technology can be widely applied.

A testing sample is recorded as a failure once the criterion condition is met during the reliability tests. Although various criterions may lead to wide variation in results, packaging reliability tests with different criterions were found from the literatures and the industrial standards. For example, the failure criterions for direct current electrical reliability measurement used in a single conference included relative resistance change at 5% [1], 10% [2–6], 15% [7,8], 20% [3,9–11], or a resistance threshold [12]. After reviewing typical TSV reliability paper, it was interesting to note that a large variety of criterions were used in the literatures [13–21]. A survey on industrial standards also indicated different failure criterions for electrical reliability tests. For example, IPC 9701A takes 20% nominal resistance increase as the criterion [22], but many of the JEDCE standards state that a sample is fail if parameter limits are exceeded or functionality cannot be demonstrated [23–29]. Furthermore, different criterions such as 5% [30], 10% [31], and 20% [31–33] of resistance change or a specific resistance value [31,33] are also found in JEDEC standards. Different requirements from the industrial standards and experimental time consideration are believed to be the reasons why a variety of criterions were employed in the literature.

It is observed from the aforementioned literature survey that many different criterions were used for packaging reliability tests, but the 10% and 20% were the most popular ones. Reasons for using a specific criterion were hardly found in the literatures, except the 10% of relative resistance change used by Frank et al. [15] since they claimed that circuits are generally designed to work with a maximum 10% on resistor-capacitor delay. Furthermore, Pan explained why 20% resistance increase is a reasonable criterion for their experiments according to the control chart theory by considering size and material properties of their test samples [34]. To study the effects of criterion itself on TSV structures, several reliability tests on packaging with TSV chains were performed, and the experimental data were statistically analyzed through different but commonly used criterions on resistance increase. Comparisons of the analysis results will be discussed next after Weibull parameter extractions. According to the experimental data, this paper finally investigates a suitable duration for a reliability test.

2 The Experiments and the Weibull Reliability Model

The test samples (which is 2.9 mm × 2.9 mm flip chip TSV packaging with 300 μm leadless solder balls) for our experiments are the daisy chain (via chain) of the TSV structures with 14 vias, as the sketch presented in Fig. 1. The via diameter for the TSV is 60 μm and the total resistance for a via chain is about 7 Ω. To construct current paths through the TSV chain, test chips for current bias tests were mounted on a self-design, FR-4 printed circuit board (PCB) as shown in Fig. 2. For nonbias testing samples, preconditionings process to simulate PCB mounting was performed so that both bias and nonbias samples are comparable. To resolve a low resistance change on test samples, four-point-probe methodology with an Agilent 4156 C Precision Semiconductor Parameter Analyzer was used [32]. To avoid thermal effect, resistances were measured at room temperature (25 °C).

Figure 3 is the flowchart for the experimental procedure. In this study, the initial resistances of the test samples after PCB mounting or preconditioning were first measured as the baseline for the followed experiments, and the reliability tests include the temperature humidity cycling test (THCT), biasing thermal aging test (BTAT), and biasing thermal cycling test (BTCT). Table 1 lists the specifications of the tests.

In this study, the commonly used 5%, 10%, 15%, and 20% resistance increase were employed as the failure criterions to perform reliability analyses after the experiments. Weibull

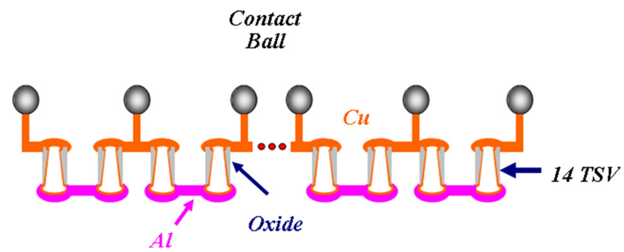

Fig. 1 The via chain structure [4]

Contributed by the Electronic and Photonic Packaging Division of ASME for publication in the Journal of Electronic Packaging. Manuscript received August 16, 2015; final manuscript received February 25, 2016; published online March 23, 2016. Assoc. Editor: Seungbae Park.

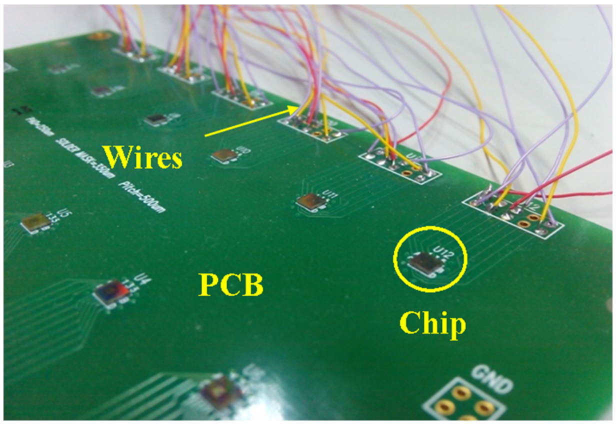

Fig. 2 Setup for the biasing tests

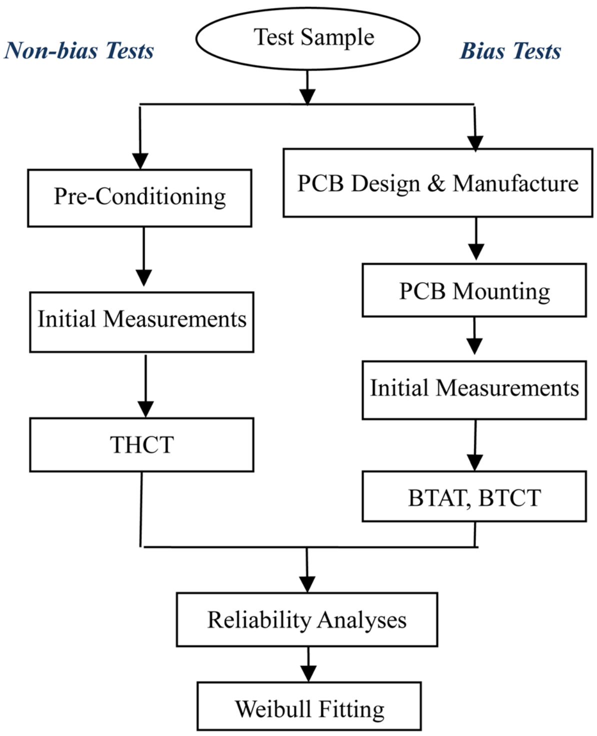

Fig. 3 The experimental flowchart

parameters were next extracted from the reliability data according to the two-parameter Weibull distribution function

$$F(t) = 1 - \exp\left[-\left(\frac{t}{\eta}\right)^{\beta}\right] \quad (1)$$

where $F(t)$, β, and η are, respectively, the cumulative failure rate, the shape parameter, and the scale parameter (or characteristic lifetime parameter since it is the time for 63.2% sample fail). In

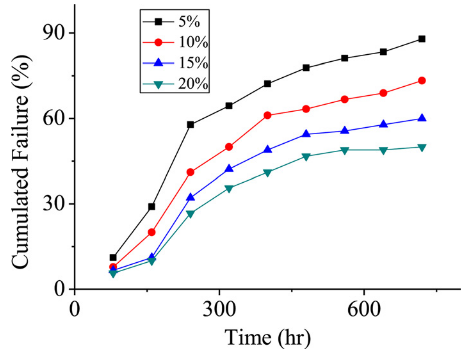

Fig. 4 Reliability test results for THCT

addition, $\beta < 1$ and $\beta > 1$ indicate that the failure rate decreases (i.e., "infant mortality") and increases (i.e., "aging" or "wear out") with time, respectively. The WEIBULL++ software (version 6) was used for parameter extractions through data fitting, and the strength of the fittings was checked through the correlation coefficients (ρ) calculated from fitting.

3 Results and Discussion

3.1 The THCT. Resistances increasing with time were monitored from testing samples during the experimental process (not show) due to the formation and growth of defects. However, individual sample behaviors were found so that each sample reaches a criterion at a different time. After the experiments, the relationships between time and the cumulative failure rate, which is defined as the number of the failed devices over the total device number after preconditioning, were plotted. Figure 4 illustrates the reliability experimental results for the test based on different relative resistance change as the failure criteria. From Fig. 4, it is observed that the failure rates increased with time, but the increasing rates reduced with the criteria.

Figure 4 basically shows increasing failure at a decreasing rate as time increases, and Fig. 5 plots the extracted Weibull parameters, respectively, for the 5%, 10%, 15%, and 20% criterions according to the data in Fig. 4. All of the correlation coefficients (ρ) for the fitting were larger than 0.97, so that the fitting results are good enough. From Fig. 5, it is observed that the shape parameter (β) distributions are extremely close with 2.5% maximum differences, and all of the values indicate wear-out failure modes. It is noted from Fig. 5 that the scale parameter (η) for the experiments is approximately linearly rising with the percentage of the criterions.

3.2 The BTAT. Similar as the THCT results, sample resistances for BTAT were increasing but with individual behaviors. Furthermore, resistances of the testing samples increased more rapidly at the first 5% but the increment became slower afterward. Consequently, the 5% curve increases much faster than the others. Figure 6 plots the results for the tests. Similar to Fig. 4, Fig. 6 shows smooth curves with increasing cumulative failures. Note that the cumulative failures for the 15% and 20% curves are the same between 120 hrs and 150 hrs because resistances of the failed

Table 1 Specifications of the reliability tests

Test	Condition	Number of samples	R.S.I. (hr)	Standard
THCT	8-hr cycle, 30–85 °C temp. range, 95% RH	90	80	JESD22-A100C [23]
BTAT	125 °C storages temperature	53	10	JESD22-A108C [28]
BTCT	2-hr cycle with 0–100 °C temperature range	43	20	JESD22-A104D [26]
Biasing	2×10^4 A/cm^2 of current density	53 + 43		JEP 154 [31]

Note: RH—relative humidity and R.S.I.—resistance scan interval.

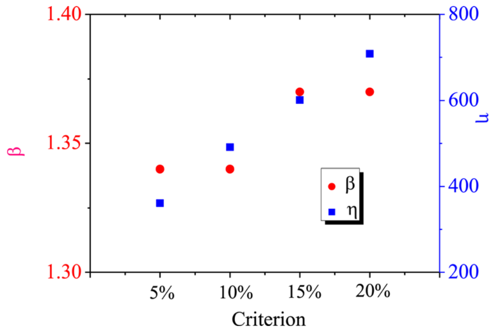

Fig. 5 Extracted Weibull parameters from the results in Fig. 4

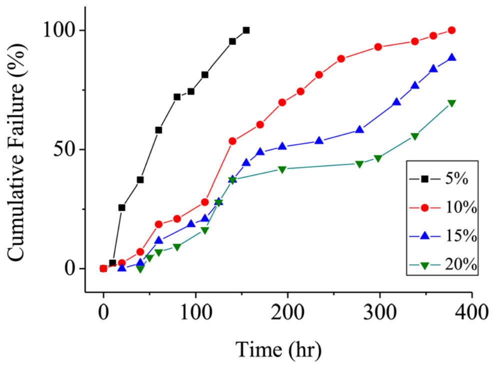

Fig. 6 Reliability test results for BTATs

samples increased more than 20% during the time period. This phenomenon might imply the appearance of the second physical failure model.

Figure 7 plots the extracted Weibull parameters from different failure criterions, and all of the correlation coefficients (ρ) for the fitting are larger than 0.95. It is observed that the shape parameters (β) imply wear-out failure modes, and the data distribution is close (in the range of $1.66 \pm 8\%$). Similar to Fig. 5, it is interesting to note that the scale parameters (η) for the experiment are also a linearly rising profile.

3.3 The BTCT. Figures 8 and 9 are the results for the BTCT, and an abrupt increase at the beginning of fail (120 hrs) is observed in Fig. 8, especially for the 5% and 10% curves. However, the 20% curve has a totally different shape from the others since the failure rate increased slowly at a later lifetime. This is because the sample resistances reached 5% and 10% in a relative short period (respectively, at 120 and 140 hrs), but it took a longer time for the resistance to reach the 20% criterion. It is also interesting to note that the biasing samples (BTAT and BTCT) have shorter failure times than the nonbias THCT samples due to electromigration effect. Consequently, it is concluded that current bias is a strong factor for TSV unreliability.

Excluding the extremely large shape parameter for the 5% result which was derived from three-point fitting only, data in Fig. 9 imply wear-out failure modes, and the scale parameter (η) for the experiments is also approximately linearly rising. The correlation coefficients (ρ) for the fitting are larger than 0.94, except the 0.84 from the 10% criterion.

To sum up, it is found that different criteria may lead to different shape parameters if there is an abrupt increase in accumulation of failure. In addition, the linear η versus criterions for the three experiments in this section is believed due to the average effect from the samples. That is, although each sample has its individual life-resistance record, the average behavior of a group of samples reveals a roughly linear relationship between η and the criteria.

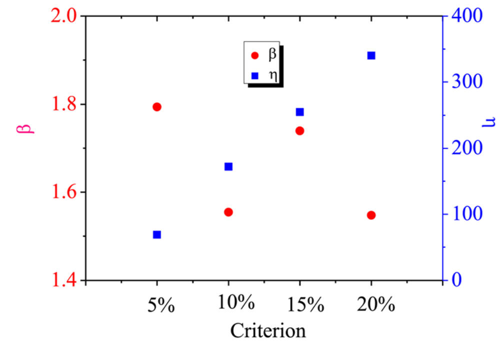

Fig. 7 Extracted Weibull parameters from the results in Fig. 6

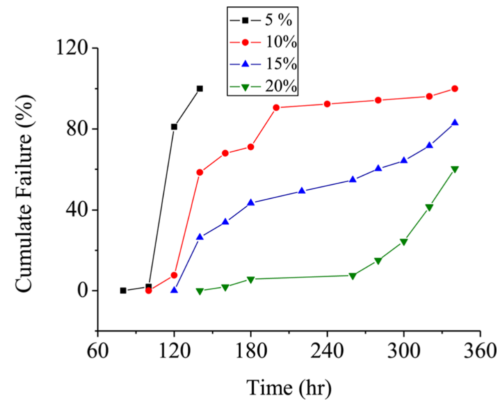

Fig. 8 Reliability test results for BTCTs

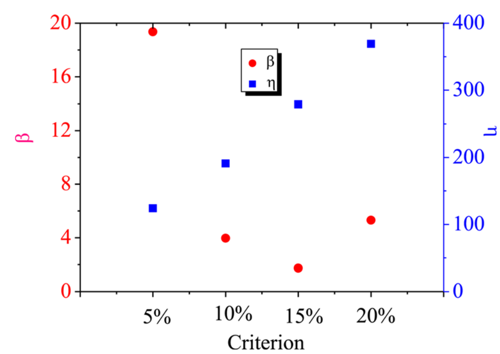

Fig. 9 Extracted Weibull parameters from the results in Fig. 8

Furthermore, different slopes of the linear fitting lines on η may imply different acceleration factors for the environmental conditions, and the intercepts of the η curves may be explained as the time of the dominate failure mode initiation.

3.4 Weibull Parameters From Different Percentages of Failed Devices. A reliability test is generally a time-consuming procedure so that the efficiency can be improved if a suitable terminating time for the experimental process has been chosen. To this end, JEP 154 standard recommended that each leg of the test should be continued until at least 65% of the test devices have failed [31], and testing 63% of failure is preferred in IPC-9701A standard, although 50% is acceptable [22]. Consequently, it is interesting to found the differences on the extracted Weibull parameters if the aforementioned experiments on TSV were terminated in an earlier time.

Tables 2 and 3, respectively, compare the extracted β and η parameters with the results in Secs. 3.1–3.3 (rows marked as "Previous") if the experimental processes stopped when 65% of

Table 2 Extracted β parameters at different failed devices

Test		THCT		BTAT				BTCT		
Criterion (%)		5	10	5	10	15	20	5	10	15
Previous β		1.34	1.34	1.79	1.55	1.74	1.55*	19.3	3.97	1.75
65% of failed devices	β value	1.59	1.39	2.09	1.46	1.82	1.55*	26.3	11.4	1.57
	Difference (%)	18.7	3.7	16.6	−5.8	4.6	0*	36.3	187	−10.3
50% of failed devices	β value	1.83	1.60	2.56	1.42	2.0	1.68	26.3	16.1	1.61
	Difference (%)	36.6	19.4	43	−8.4	14.9	8.4	36.3	306	8.0
Note								◆	◆	

Note: THCT—thermal humidity cycle test; BTAT—bias thermal aging test; BTCT—bias thermal cycle test; ◆—short of fitting point; and *—parameter from the same dataset.

Table 3 Extracted η parameters at different failed devices

Test		THCT		BTAT				BTCT		
Criterion (%)		5	10	5	10	15	20	5	10	15
Previous η		362	492	69	172	255	340*	124	191	280
65% of failed devices	η value	311	473	59	186	230	340*	118	150	291
	Difference (%)	−14.1	−3.9	−14.5	8.1	−9.8	0*	−4.8	−21.5	3.9
50% of failed devices	η value	272	400	46	196	214	298	118	141	286
	Difference (%)	−24.9	−18.7	−33.3	14.0	−16.1	−12.4	−4.8	−26	2.1
Note								◆	◆	

Note: THCT—thermal humidity cycle test; BTAT—bias thermal aging test; BTCT—bias thermal cycle test; ◆—short of fitting point; and *—parameter from the same dataset.

devices and 50% of devices were failed, respectively. Note that the previous parameters are extracted from the dataset with at least 80% of devices were failed, except the 20% criterion from BTAT. Due to rapidly increasing failure rates at the beginning of fail, BTCT data in columns mark with "◆"were not reliable because the parameters were derived from only two or three point fitting. After comparing data in the tables, it is found that parameters derived from larger failed percentage lead to better results, but the differences between β parameters are mostly limited so that similar conclusions may be proposed on the Weibull failure modes. However, linearity profiles on η were missing as the terminal failure percentages are reducing. This is because the average effect deteriorates as the failure data were obtained from fewer samples, which are relatively weak.

In summary, it is recommended that 50% of failed device is the minimum requirement to terminate a reliability test on TSV packaging, and the 65% of failed device requirement by the standards is a reasonable demand for the reliability tests.

4 Conclusion

According to the experimental data through reliability tests on TSV chains, different failure criterions on relative resistance change were employed to statistically investigate the sample behaviors through the extracted Weibull parameters. The following conclusions are found based on the parameter analyses:

(1) Although different failure criterions were used, the extracted shape parameters for a reliability test are not far, so that the same Weibull failure mode will be conducted if the failure curve does not increase abruptly.
(2) The extracted scale parameters are approximately linearly increasing profiles with the percentage of the failure criterions.
(3) A reliability test shall not terminate if less than 50% of the devices has been failed, and 65% of failed devices are recommended to be a suitable duration for a reliability test.

Acknowledgment

The authors would like to thank Ministry of Science and Technology of Taiwan, R.O.C. for financial supports under Grant NSC 104-2221-E-606-016. Experimental data prepared by Mr. Chung-Yen Ni at the Semiconductor Lab., National Defense University, is greatly appreciated.

References

[1] Kuo, K. H., Lee, J., Chien, F. L., Lee, R., Mao, C., and Lau, J., 2014, "Electromigration Performance of Cu Pillar Bump for Flip Chip Packaging With Bump on Trace by Using Thermal Compression Bonding," 64th Electronic Components and Technology Conference (ECTC), Orlando, FL, May 27–30, pp. 56–60.

[2] Baba, S., Koide, M., Watanabe, M., Fukuzono, K., Yamamoto, T., Sakuyama, S., Shimizu, K., Okamoto, K., and Mizutani, D., 2014, "Development of Second-Level Connection Method for Large-Size CPU Package," 64th Electronic Components and Technology Conference (ECTC), Orlando, FL, May 27–30, pp. 68–73.

[3] Wu, F. J., Ho, L. H., Kuo, C. M., Tu, C. J., Ni, C. H., Chang, S. C., Wu, C. Y., Lin, K. A., Wu, W. H., and Wu, Y. S., 2014, "Six-Die Stacking: Three-Dimensional Interconnects Using Au and Pillar Bumps," 64th Electronic Components and Technology Conference (ECTC), Orlando, FL, May 27–30, pp. 316–323.

[4] Lwo, B. J., Lin, M. S., and Huang, K. H., 2014, "TSV Reliability Model Under Various Stress Tests," 64th Electronic Components and Technology Conference (ECTC), Orlando, FL, May 27–30, pp. 620–624.

[5] Demir, K., Armutlulu, A., Tong, J., Pucha, R., Sundaram, V., and Tummala, R., 2014, "First Demonstration of Reliable Copper-Plated 30 μm Diameter Through-Package-Vias in Ultra-Thin Bare Glass Interposers," 64th Electronic Components and Technology Conference (ECTC), Orlando, FL, May 27–30, pp. 1098–1102.

[6] Hau-Riege, C., Keser, B., Alvarado, R., Syed, A., Yau, Y. T., Bezuk, S., and Caffey, K., 2014, "The Impact of Different Under Bump Metallurgies and Redistribution Layers on the Electromigration of Solder Balls for Wafer-Level Packaging," 64th Electronic Components and Technology Conference (ECTC), Orlando, FL, May 27–30, pp. 1173–1178.

[7] Islam, N., Kim, G., and Kim, K., 2014, "Electromigration for Advanced Cu Interconnect and the Challenges With Reduced Pitch Bumps," 64th Electronic Components and Technology Conference (ECTC), Orlando, FL, May 27–30, pp. 50–55.

[8] Huang, Y. W., Zhan, C. J., Juang, J. Y., Lin, Y. M., Huang, S. Y., Chen, S. M., Fan, C. W., Cheng, R. S., Chao, S. H., Hsieh, W. L., Chen, C., and Lau, J. H., 2014, "Effect of Joint Shape Controlled by Thermocompression Bonding on the Reliability Performance of 60 μm-Pitch Solder Micro Bump Interconnections,"

64th Electronic Components and Technology Conference (ECTC), Orlando, FL, May 27–30, pp. 1908–1914.
[9] Na, D. J., Aung, K. O., Choi, W. K., Kida, T., Ochiai, T., Hashimoto, T., Kimura, M., Kata, K., Yoon, S. W., and Yong, A. C. B., 2014, "TSV MEOL (Mid End of Line) and Packaging Technology of Mobile 3D-IC Stacking," 64th Electronic Components and Technology Conference (ECTC), Orlando, FL, May 27–30, pp. 596–600.
[10] Arfaei, B., Mutuku, F., Sweatman, K., Lee, N. C., Cotts, E., and Coyle, R., 2014, "Dependence of Solder Joint Reliability on Solder Volume, Composition and Printed Circuit Board Surface Finish," 64th Electronic Components and Technology Conference (ECTC), Orlando, FL, May 27–30, pp. 655–665.
[11] Hutzler, A., Tokarski, A., Kraft, S., Zischler, S., and Schletz, A., 2014, "Increasing the Lifetime of Electronic Packaging by Higher Temperatures: Solders vs. Silver Sintering," 64th Electronic Components and Technology Conference (ECTC), Orlando, FL, May 27–30, pp. 1700–1706.
[12] Garnier, A., Jouve, A., Franiatte, R., and Cheramy, S., 2014, "Underfilling Techniques Comparison in 3D CtW Stacking Approach," 64th Electronic Components and Technology Conference (ECTC), Orlando, FL, May 27–30, pp. 906–912.
[13] Tsuchiya, H., and Yokogawa, S., 2006, "Electromigration Lifetimes and Void Growth at Low Cumulative Failure Probability," Microelectron. Reliab., **46**(9), pp. 1415–1420.
[14] Frank, T., Chappaz, C., Leduc, P., Arnaud, L., Moreau, S., Thuaire, A., El Farhane, R., and Anghel, L., 2010, "Reliability Approach of High Density Through Silicon Via (TSV)," 12th Electronics Packaging Technology Conference (EPTC), Singapore, Dec. 8–10, pp. 321–324.
[15] Frank, T., Moreau, S., Chappaz, C., Leduc, P., Arnaud, L., Thuaire, A., Chery, E., Lorut, F., Anghel, L., and Poupon, G., 2013, "Reliability of TSV Interconnects: Electromigration, Thermal Cycling, and Impact on Above Metal Level Dielectric," Microelectron. Reliab., **53**(1), pp. 17–29.
[16] Kuo, K. H., Lee, J., Chen, S., Chien, F. L., Lee, R., and Lau, J., 2012, "Electromigration Performance of Printed Sn0.7Cu Bumps With Immersion Tin Surface Finishing for Flip Chip Applications," 62nd Electronic Components and Technology Conference (ECTC), San Diego, CA, May 29–June 1, pp. 698–702.
[17] Dixit, P., Viljanen, H., Salonen, J., Suni, T., Molarius, J., and Monnoyer, P., 2013, "Fabrication, Electrical Characterization and Reliability Study on Partially Electroplated Tapered Copper Through-Silicon Vias," 8th International Microsystems, Packaging, Assembly and Circuit Technology Conference (IMPACT), Taipei, Taiwan, Oct. 22–25, pp. 190–193.
[18] You, H. Y., Hwang, Y., Pyun, J. W., Ryu, Y. G., and Kim, H. S., 2012, "Chip Package Interaction in Micro Bump and TSV Structure," 62nd Electronic Components and Technology Conference (ECTC), San Diego, CA, May 29–June 1, pp. 315–318.
[19] Suriya, M., Lee, D., Lee, J. C. B., Kim, J., Deai, H., and Yeung, J., 2013, "The Reliability Performance of Copper Wire Bonding BGA Package by Way of HAST Methodology," 8th International Microsystems, Packaging, Assembly and Circuit Technology Conference (IMPACT), Taipei, Taiwan, Oct. 22–25, pp. 180–185.
[20] Lall, P., and Lowe, R., 2014, "Comparison of Prognostic Health Management Algorithms for Assessment of Electronic Interconnect Reliability Under Vibration," ASME J. Electron. Packag., **136**(4), p. 041013.
[21] Xi, J., Zhai, X., Wang, J., Yang, D., Ru, M., Xiao, F., Zhang, L., and Lai, C. M., 2015, "Reliability Assessment of Wafer Level Packages With Novel FeNi Under Bump Metallization," ASME J. Electron. Packag., **137**(3), p. 031016.
[22] IPC, 2006, "Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments," Association Connecting Electronics Industries, Bannockburn, IL, Standard No. IPC-9701A.
[23] JEDEC, 2007, "Cycled Temperature-Humidity-Bias Life Test," JEDEC Solid State Technology Association, Arlington, VA, Standard No. JESD 22-A101C.
[24] JEDEC, 2009, "Steady State Temperature Humidity Bias Life Test," JEDEC Solid State Technology Association, Arlington, VA, Standard No. JESD 22-A100C.
[25] JEDEC, 2010, "High Temperature Storage Life," JEDEC Solid State Technology Association, Arlington, VA, Standard No. JESD 22-A103D.
[26] JEDEC, 2009, "Temperature Cycling," JEDEC Solid State Technology Association, Arlington, VA, Standard No. JESD 22-A104D.
[27] JEDEC, 2004, "Power and Temperature Cycling," JEDEC Solid State Technology Association, Arlington, VA, Standard No. JESD 22-A105C.
[28] JEDEC, 2005, "Temperature, Bias, and Operation Life," JEDEC Solid State Technology Association, Arlington, VA, Standard No. JESD 22-A108C.
[29] JEDEC, 2009, "Highly Accelerated Temperature and Humidity Stress Test (HAST)," JEDEC Solid State Technology Association, Arlington, VA, Standard No. JESD 22-A110C.
[30] JEDEC, 2000, "Constant Temperature Aging to Characterize Aluminum Interconnect Metallization for Stress-Induced Voiding," JEDEC Solid State Technology Association, Arlington, VA, Standard No. JEP 139.
[31] JEDEC, 2008, "Guideline for Characterizing Solder Bump Electromigration Under Constant Current and Temperature Stress," JEDEC Solid State Technology Association, Arlington, VA, Standard No. JEP 154.
[32] JEDEC, 2005, "Stress Test Driven Qualification of and Failure Mechanism Associated With Assembled Solid State Surface Mounted Components," JEDEC Solid State Technology Association, Arlington, VA, Standard No. JEP 150.
[33] JEDEC, 2009, "3D Chip Stack With TSVS: Identifying, Evaluating and Understanding Reliability Interaction," JEDEC Solid State Technology Association, Arlington, VA, Standard No. JEP 158.
[34] Pan, J., 2014, "A Control-Chart-Based Method for Solder Joint Crack Detection," J. Microelectron. Electron. Packag., **11**(3), pp. 94–103.