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Implantable Radio Frequency Identification Sensors: Wireless Power and Communication

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Abstract

There are significant technical challenges in the development of a fully implantable wirelessly powered neural interface. Challenges include wireless transmission of sufficient power to the implanted device to ensure reliable operation for decades without replacement, minimizing tissue heating, and adequate reliable communications bandwidth. Overcoming these challenges is essential for the development of implantable closed loop system for the treatment of disorders ranging from epilepsy, incontinence, stroke and spinal cord injury. We discuss the development of the wireless power, communication and control for a Radio-Frequency Identification Sensor (RFIDS) system with targeted power range for a 700mV, 30 to 40uA load attained at −2dBm.

Index Terms

RFID; RFID Sensor; CMOS; Neural Interface

I. INTRODUCTION

This paper describes the wireless power, control and communication for an implantable neural interface powered via a far-field radiofrequency source. There are significant tradeoffs that must be made when designing implantable sensors. Given the sensitivity of inductive coupling to alignment, and depth, it is not a good candidate for powering or communicating with multiple devices implanted in the body. The development of far-field power and communication is essential to the development of distributed implantable RFID Sensor networks (RFIDS).

II. Micro NEURAL Controller

A. State Machine

As shown in Figure 1 the RFIDS has five operating modes including three working modes: Power-Up & Sync Mode (0), Standby Mode (1), Time-Stamp Mode (2), Streaming Mode (3) and Snippet Mode (4). In the Power-Up & Sync Mode (0), the RFID harvests energy and synchronizes its clock with the radio frequency (RF) signal from the external base station via the phase locked loop (PLL).

Upon synchronization the sensor enters into the Standby Mode (state 1, Figure 1). The Standby Mode (1) is a power-saving mode where all circuits are powered down except the state control and command/receive functions.

Time-Stamp Mode (2) allows real-time applications by observing and transmitting the time of neural spike occurrences. A threshold circuit is programmed by the user to record a spike occurrence when the neural activity crosses the threshold storing an occurrence in memory. When polled the neural interface transmits the interval between spikes and threshold levels exceeded (positive and/or negative). The timestamp data is recorded from up to 40 sensors simultaneously.

In Streaming Mode (3), 8 bit waveforms sampled at 15.6Ksps are recorded/transmitted from up to 4 sensors simultaneously (queried sequentially by the base station). The controller turns off the thresholder to save power in this mode.

In Snippet Mode (4), the sensor stores 1.5 ms of data following a threshold crossing. The chip stores 8 samples pre threshold and 24 samples post threshold. The waveform shapes are recorded/transmitted from up to 20 sensors.

A block level diagram of the Neural Interface is shown in Figure 2. The neural signal is bandpass filtered and amplified and then passed to a thresholder circuit and the analog to digital converter (ADC). From there the data are stored in the FIFO. The data is then formed into packets for transmission back to the base station when polled using the unique ID on each sensor. Upon request from the base station, the controller enters states in which outbound packets are formed from the FIFO and transmitted (Figure 3). Table I and Table II show the packet formats for each communication protocol. Each inbound command generates a response from each sensor consisting of a data packet or a null data packet if no data were recorded. Variable length packet formats (Figure 3 and Table II) are used to minimize power and bandwidth during operation. While forming a packet, the preset header, the start of packet (SOP) delimiter, and the hard programmed tag address are loaded to the packet format register directly. Neural data in the FIFO and CNT extension information in Time-Stamp Mode as well as Error Detection/Correction Code are loaded and computed in real time. The packet stream is Manchester Encoded, spread in spectrum and transmitted to the base station.

B. FIFO

In this effort, an 8×32 FIFO (First-in First-out) is used as a memory buffer for storing neural data. A dual-ported 8T SRAM memory, Figure 4, with a read buffer has been adopted to enable fast Non-Destructive Reads (NDR). With a working power supply of 400mV, the FIFO shares a 15.6 KHz clock frequency with the ADC for writing and a 400 KHz clock frequency for read. As in shown in Figure 2, neural spike times and digitized samples from the ADC are written to the 8 bit by 32 word FIFO. This information is stored until the RFIDS is polled for transmission. After the contents in the FIFO are fully cleared, the write and read pointer are reset to the top of the FIFO, readying the sensor for the next cycle. The FIFO area is 71.7 μm × 211.7 μm.

III. PLL

As result of technology advancement, market demands for greater portability and implantation, several low power phase-locked loops (PLL) have been presented by multiple authors in recent years. Gundel and Carr presented a low power PLL for biomedical wireless applications consuming 20 μW at 3.3 V, with clock frequency of 100 kHz [1], fabricated in a 0.6 μm CMOS process. Popplewell et al proposed a PLL for self-powered RFID

applications with an output frequency of 5.2 GHz with a power consumption of 1.1 mW at 1.2V [2], fabricated in a 130 nm CMOS process. Other authors have proposed low voltage PLLs for different applications, which are tabulated in Table III.

Our PLL has a power consumption of 2.7 μW with an output frequency of 3.2 MHz using a 0.7 V power supply. Table III indicates that Popplewell's PLL is the lowest power, but this is the result of using an LC crossed-coupled VCO.

The PLL of Figure 5 is a standard charge pump PLL consisting of a standard phase-frequency detector (PFD), a buffer, a charge pump, a transmission gate switch, a passive loop filter, and a standard current starved voltage-controlled ring oscillator (VCO) with a divide-by-4 divider. The five stage current starved ring oscillator requiring 7 legs of bias current consuming more than 50% of total PLL power. The loop is synchronized during both power/packet reception, and a switch is used to break and hold the loop while the outgoing packet is being transmitted. The charge pump must hold the VCO to minimize drift during the packet transmission period.

The charge pump is a current steering topology proposed by Maneatis [6] which has the advantage of being suitable for low voltage applications due to the presents of only two saturated transistors drops to the ground. The buffer ahead of the charge pump converts the "up" and "dn" generated by the PFD to complementary "up" and "dn". The schematic of the buffer is given in Figure 6, along with the schematic of the charge pump from Maneatis [6]. The charge injection problem inherent to charge pumps is significantly reduced as a result of the NFET steering switches operating in weak inversion and their reduced inversion layer charge.

The PLL is designed with a damping ratio of 0.7. The worst case simulated settling time is 12 μs when the VCO control voltage is pulled down from VDD (greatest distance from the settling voltage) to the nominal settling voltage. The area consumed by the PLL is 170 μm × 95 μm.

IV. RF-DC

This section describes the RF-Front end for each ARFID sensor. Figure 7 shows the block diagram of the front end with all significant building blocks. The RF to DC front end consists of the antenna, matching network, RF-DC converter, band-gap reference and a low drop out regulator (LDO) which powers the signal conditioning circuitry. The load modulator alters the antenna impedance to achieve backscatter transmission of outbound data to the base station at 3.2Msps. The design of the antenna is beyond the scope of this work and hence shall not be discussed. However, through the use of 2D and 3D electromagnetic simulation [7] it has been determined that safe levels of power near the brain surface is approximately 200uW [8] from which we expect to harvest 50uW.

A. Matching network

The matching network including the antenna is designed to maximize the power transfer between the antenna and the input to the rectifier. The power match is typically either a shunt or series LC network avoiding power dissipated in the network. The choice between shunt LC match versus series LC match depends on the following criteria:

1. Available input power
2. Impedance of the antenna
3. Input impedance of the RF-DC converter.

Efficient harvesting is a function of all three. The RF-DC converter is required to produce an adequate amount of DC voltage to power the signal conditioning circuitry while maintaining high efficiency. The shunt LC network is a good candidate if the input voltage is high and the impedance of the antenna and the RF-DC converter are closely matched [9]. Efficiency can be maximized by minimizing the losses in the RF-DC converter which translates to having a fewer number of stages (fewer series diodes losses) and operating the diodes as high on the I–V curve as practical without the diode going ohmic (i.e. operate the diode at as high a switched current density as possible). It is desirable that the voltage levels at the input to the rectifier be high relative to diode turn on voltage without damaging the diode. This often results in the series LC matched networks being the better candidate as the result of providing a voltage boost of Q when antenna impedances are low. The input impedance of the RF-DC converter is given as follows [10–11] (the equations have been modified to include only positive half wave rectification)

$$R_{in}=\frac{\widehat{v_{in}}}{4NI_{OUT}} \quad (1)$$

$$C_{in}=\frac{2N}{T}\int_0^T CD\left[\overline{VD}+\widehat{vin}.\sin\omega t\right]dt \quad (2)$$

Where N is the number of stages and I_{out} is the target load current. The network was designed to match the impedances resulting in L and C values of 9.49 nH and 382 fF respectively with an antenna impedance of ~50 ohm.

B. RF-DC converter

A single stage RF-DC converter is shown in Figure 8. Two methods of implementing the RF-DC converter are:

1. Using a MOS devices in a switch based arrangement.
2. Using either a schottky diode (preferred due higher fT) or MOS diodes for rectification.

In a biological environment, the RF-DC converter is required to generate a DC voltage from the RFIDS antenna which has very low input power available. Lower power levels are a result of absorption of RF power by biological tissue as well as limits on specific absorption rates (SAR) in humans [12–15]. The permissible level is 1.6W/kg of tissue in order to avoid raising the temperature by greater than 1°C [16]. A clock cannot be implemented on chip due as a result of the power cost at high frequencies. These two disadvantages make the Dickson architecture or its modified version using MOS transistors [17–18] infeasible for use in 1.0–2.4 GHz high frequency RFIDS.

Sarpeshkar and Mandal proposed a MOS switch based design for the RF-DC converter [17]. Three factors influence the choice of a MOS or schottky diode switch; 1) the MOS threshold voltage, 2) the available switching voltage, and 3) switch current density per sheet capacitance a figure of merit being (A/fF-um^2). Typically schottky diode and MOS switches provides an order of magnitude increase in current for every 60/120mV increase in turn on voltage respectively;

$$V_{REF}=nV_T N\ln(k)+\frac{N}{L}VD_1 \quad (3)$$

where n ≈ 1 for Schottky diodes and SOS-CMOS and n ≈ 2 for bulk CMOS. For Schottky diodes the log linear range is limited to 400 to 500mV while for CMOS switches the range is limited by threshold voltage. However MOS switches have a distinct advantage in that the "on resistance" can be further reduced as the overdrive voltage exceeds the threshold voltages reducing the I_D V_{drop} (includes and $I_D V_D$ and $I_D 2RS$) switch losses of all "diodes". As a result MOS switches have the potential to further reduce the switch on resistance when signal levels are large relative to the threshold voltage and CMOS f_T is adequate to support the desired current bandwidth. Where the combination of the available input power and antenna impedance translates to a large signal input to the rectifier, MOS switch stages can be cascaded to obtain even higher DC voltages with high efficiency. High performance low voltage transistors are not available in the 180nm CMOS process from MOSIS. For the selected process CMOS devices are less efficient than available Schottky diode devices.

Curty and Declereq in [10] and our group in [11] show that a low threshold MOS diode available in a 0.5 um SOI process can be a more efficient rectification device for given switching requirements. Successful results were obtained in [11] and we were able to harvest power levels as low as −5 dBm while supporting up to 100uA load currents.

The schottky diode outperforms the MOS diode when it has a steeper I–V slope and lower sheet capacitance. Barnett and Lazar [9] have generated DC voltages of 1.3V using up to 16 Schottky diodes. The work presented here uses a single stage schottky RF-DC converter and a series LC matching network. The diodes are 5um × 5um. The blocking Cs were selected at 24pF while the diodes which behave as near ideal switches but with added diode capacitance tuned by an 9.489 nH inductor at 2.4GHz. CL was chosen to be 48 pF or as large a practical to minimize power drop out and keep supply voltage ripple well under 5mV. Figure 9 presents measured results for the RF to DC harvester verses load currents, ± 1 sigma errors bars are indicate for 10 die. The targeted power range for a 30 to 40uA is attained at −2dBm.

C. Voltage Reference and Linear regulator

The low drop out (LDO) regulator consists of a voltage reference and an error amp with a PMOS pass transistor. Figure 10 shows the schematic of the voltage reference and the LDO. Figure 11 shows the chip layout with the various blocks noted. In operation, a current proportional to temperature (I_{PTAT}) is generated across R_{PTAT} and is added with a current (I_{CTAT}) that is complementary to temperature. This temperature independent current is mirrored across R_{REF} to get the required temperature independent voltage $V_{REF.}$ Schottky diodes are used to achieve lower voltages for lower power operation. Choosing a current value in the permissible log linear range equal to 1μA, the value of Vref for 400mV was found to be equal to 6.7KΩ. The reference voltage for the circuit can be expressed as [19]

$$V_{REF} = nV_T N \ln(k) + \frac{N}{L} VD_1 \quad (4)$$

In the above equation n = 1.6273, VT = 26mV, K= 8, L= 8.8 and N = 3.8. A PMOS input stage was chosen for the error amp to allow operation under low common mode constraints. Compensation between the first stage and the output has been achieved via indirect compensation. Indirect compensation feeds back current directly into a low impedance node in the first stage, thus eliminating the need for extra legs of current [19]. The NMOS current mirror has been split into two series transistors in order to realize the low impedance node for the indirect compensation. Table IV summarizes the performance of the low drop out regulator.

V. Conclusion

Our results demonstrate that up to 100uW of power is available for on chip circuit operation with losses. The RFIDS utilizes 25uW of power for signal conditioning, spike detection, and analog to digital conversion. From circuit simulations; control, and communication circuits consume ~5 to 10uW of power (peak power during 10uS of transmission). As a result, we need to receive ~35uW of power after all losses for implantable RFIDS to be viable. This has been partially mitigated by the addition of a 48pF LDO decoupling capacitor. Based on our previous work, these power levels are possible with far-field RF at 1.0–2.4GHz range (our sim paper).

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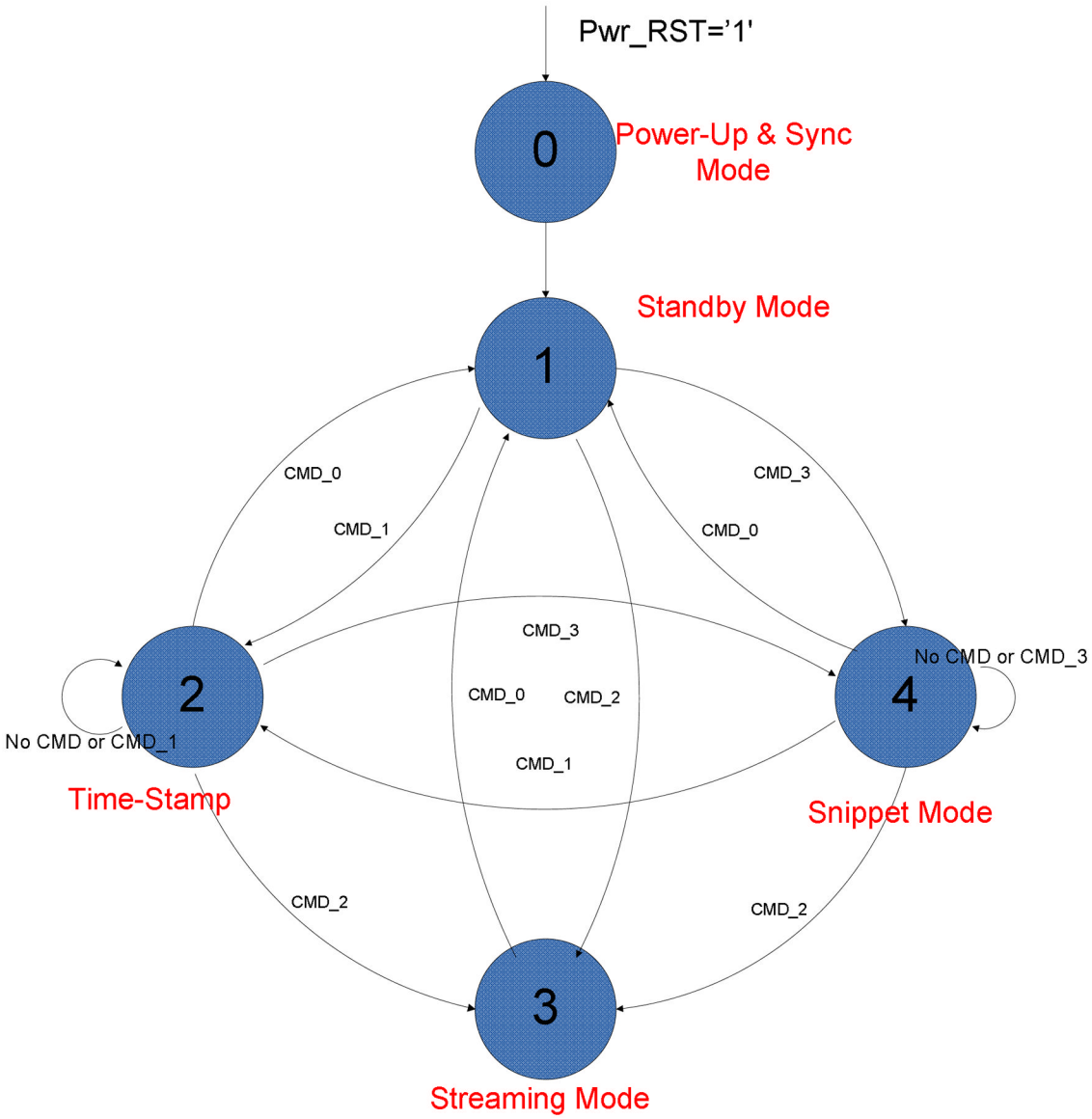

Figure 1.
Simplified controller state diagram

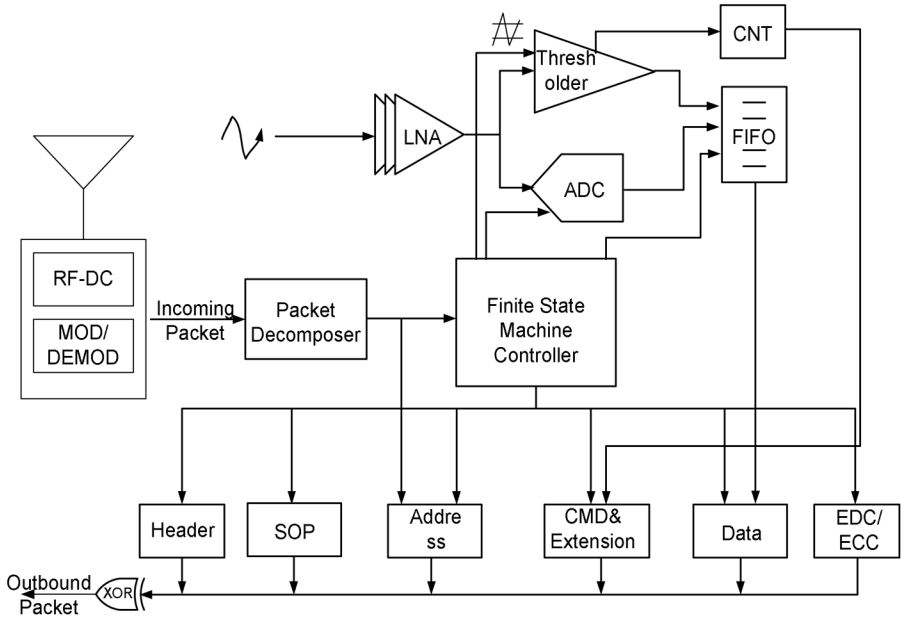

Figure 2.
Controller Block Diagram

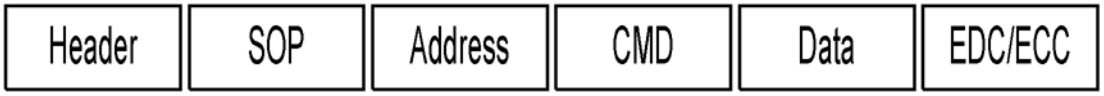

Figure 3.
General Packet Format.

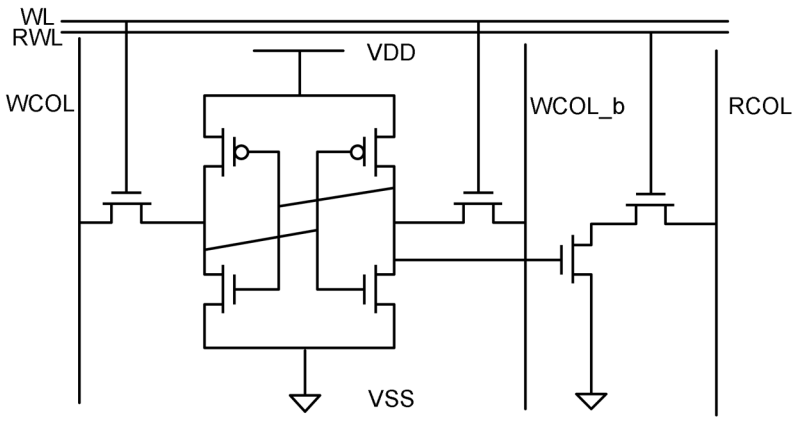

Figure 4.
8T Dual Port SRAM Cell Schematic

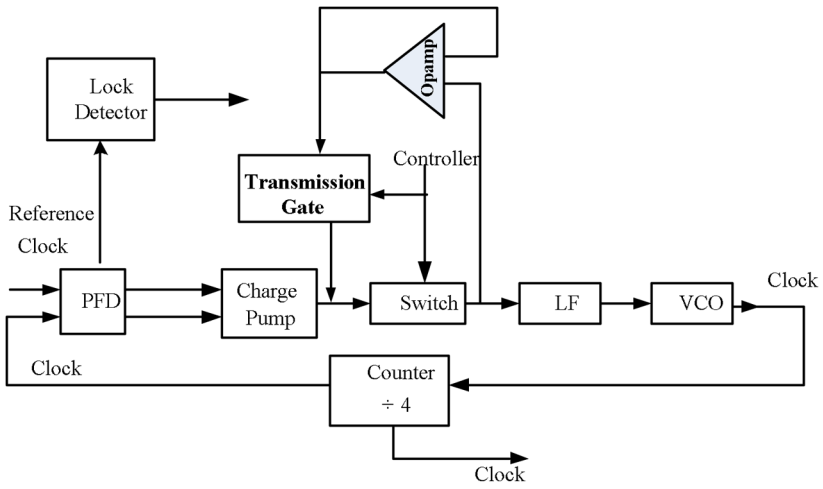

Figure 5.
PLL Block Diagram

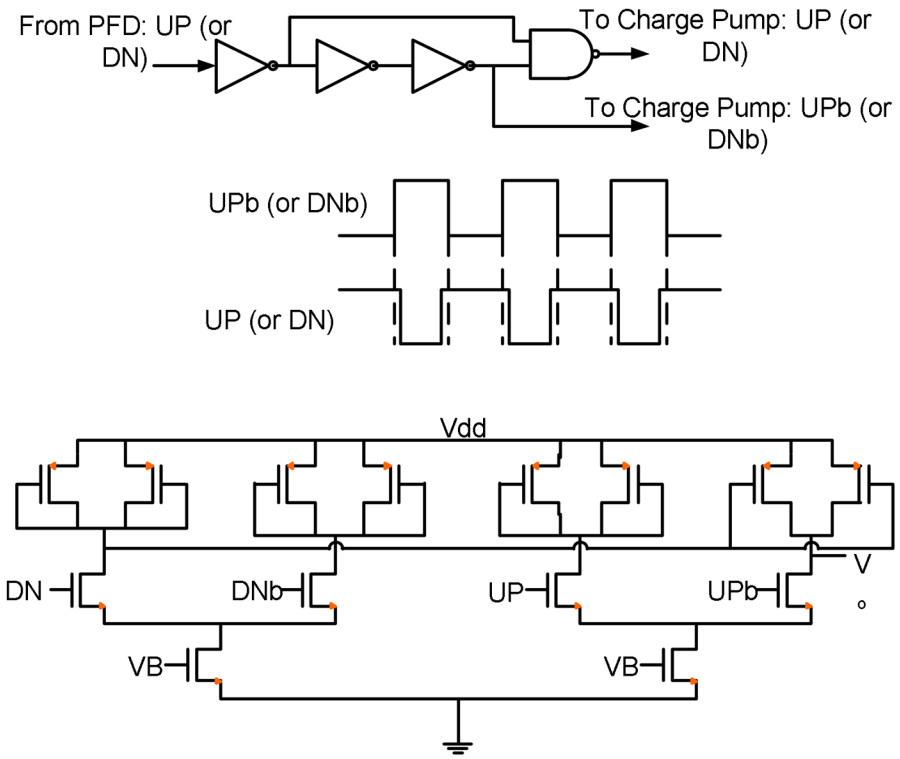

Figure 6.
The buffer (top) and the charge pump (bottom).

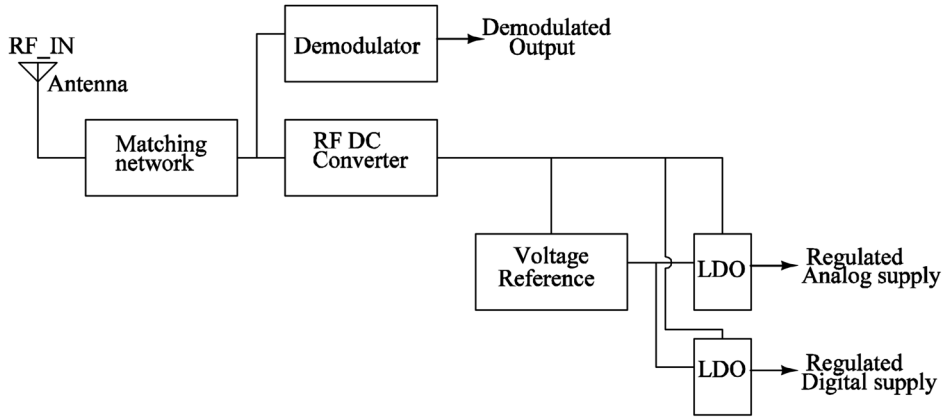

Figure 7.
Block diagram of the RF- Front End

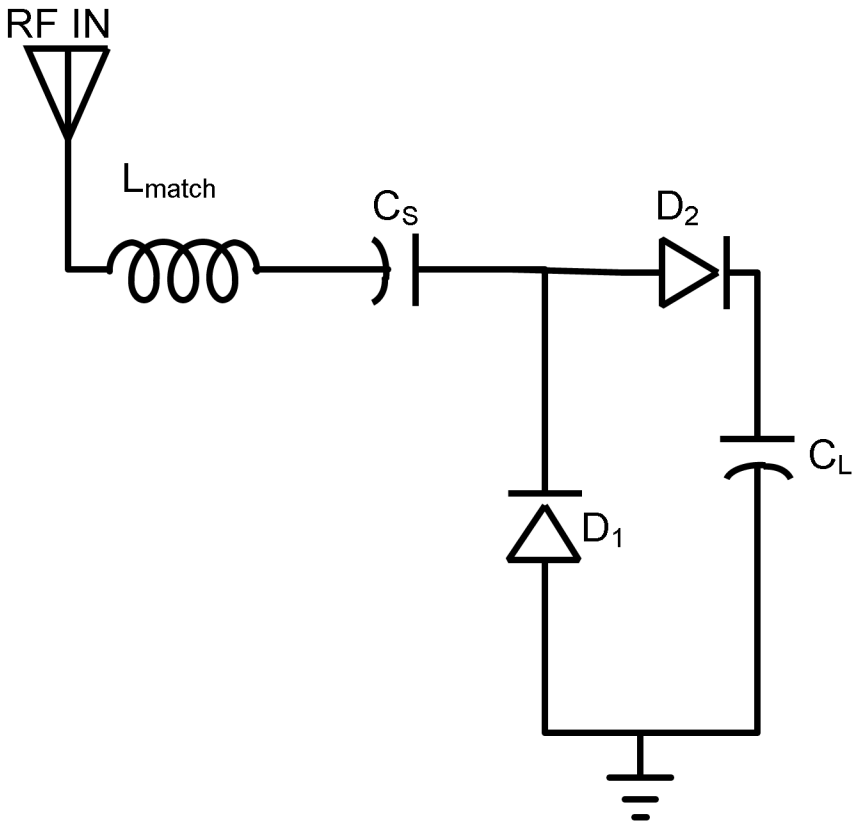

Figure 8.
Single State RF-DC converter

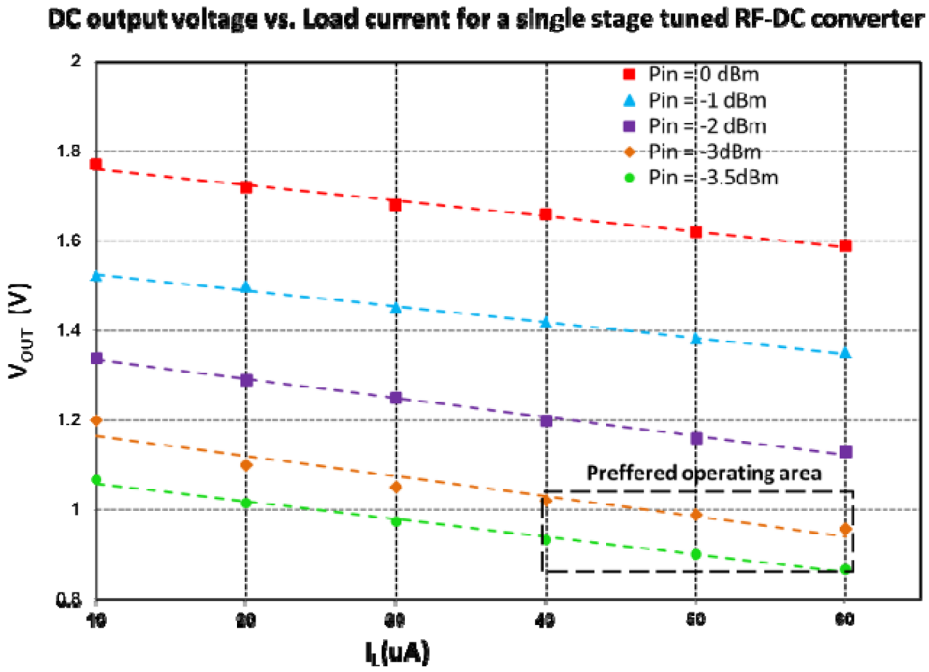

Figure 9.
Performance of the single stage RF-DC converter

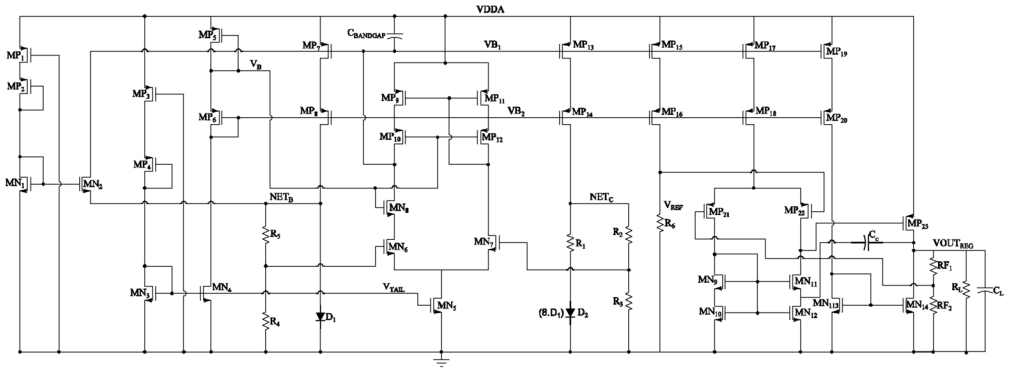

Figure 10.
Schematic of the voltage reference and LDO

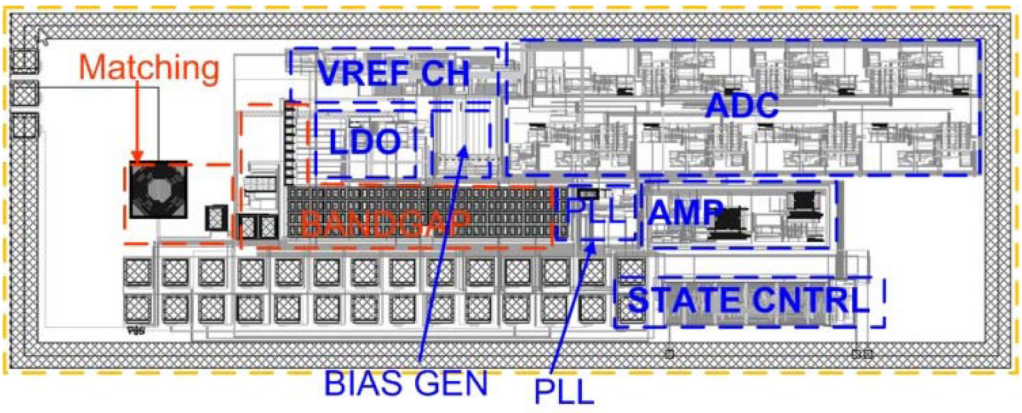

Figure 11.
Layout of the entire chip

Table I

MNI INBOUND PACKET FORMAT

Mode 2 FORMAT (Time-Stamp Mode)		
Name	**Length**	**Functionality**
Header	2	Synchronization
SOP	1	Start of Packet
Address	1	Probe ID
CMD	1	Denote previous Working Mode and content in the Data section
Data	0 – 32	Up to 16 spike detection with 8 bit ± VTH Crossing; 8 bit spike interval counter
CRC	1	Error Detection
Mode 3 Format (Streaming Mode)		
Name	**Length**	**Functionality**
Header	2	Synchronization
SOP	1	Start of Packet
Address	1	Probe ID
CMD	1/2	Denote previous Working Mode
Data	32	8 bps Spike Real Time Record
CRC	1	Error Detection
Mode 4 Format (Snippet Mode)		
Name	**Length**	**Functionality**
Header	2	Synchronization
SOP	1	Start of Packet
Address	1	Probe ID
CMD	1/2	Denote previous Working Mode
Data	1 or 32	8bps Spike Segment Capture
CRC	1	Error Detection

Table II

MNI INBOUND PACKET FORMAT

Name	Length	Functionality
Header	2	Synchronization
SOP	1	Start of Packet
Address	1	Select Probe
CMD	1	Select Working Mode
Data	0 or 1	±Threshold Setting
CRC	1	Error Detection

Table III

MNI INBOUND PACKET FORMAT

Author	Freq. (MHz)	Ch. (nm)	Power/MHz@VDD (uW/MHz)
Gundel & Carr [1]	0.1	600	200@3.3V
Popplewell [2]	5200	130	0.19@1.2V
Hsieh [3]	1900	180	2.37@0.5V
Chao [4]	610	130	2.049@0.5V
Raha [5]	500	90	0.600@0.6V

TABLE IV

VOLTAGE REGULATOR SPECIFICATIONS ACROSS CORNERS: VDD=0.9V

CORNER	TEMP(°C)	VOUT(mV)	POWER(μW)
TT	15	707.9	19.61
	27	707.6	19.57
	50	706	19.47
SS	15	713	21
	27	715	21
	50	716	21.45
FF	15	709	18.07
	27	708	18.01
	50	705.8	17.89