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IEEE Trans Circuits Syst I Regul Pap. Author manuscript; available in PMC 2008 September 11.

Published in final edited form as:
IEEE Trans Circuits Syst I Regul Pap. 2008 ; 55(7): 1863–1872. doi:10.1109/TCSI.2008.918006.

A Charge-Based Low-Power High-SNR Capacitive Sensing Interface Circuit

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Abstract

This paper describes a low-power approach to capacitive sensing that achieves a high signal-to-noise ratio. The circuit is composed of a capacitive feedback charge amplifier and a charge adaptation circuit. Without the adaptation circuit, the charge amplifier only consumes 1 μW to achieve the audio band SNR of 69.34dB. An adaptation scheme using Fowler-Nordheim tunneling and channel hot electron injection mechanisms to stabilize the DC output voltage is demonstrated. This scheme provides a very low frequency pole at 0.2Hz. The measured noise spectrums show that this slow-time scale adaptation does not degrade the circuit performance. The DC path can also be provided by a large feedback resistance without causing extra power consumption. A charge amplifier with a MOS-bipolar pseudo-resistor feedback scheme is interfaced with a capacitive micromachined ultrasonic transducer to demonstrate the feasibility of this approach for ultrasound applications.

Index Terms

Capacitive sensing circuit; charge amplifier; capacitive circuit; channel hot electron injection; Fowler-Nordheim tunneling; floating-gate circuit; MEMS microphone interface circuit

I. Motivations for Capacitive Sensing Circuits

Capacitive transduction is one of the most important and widely used techniques in microsystems to detect the force, pressure, as well as the position, velocity, or acceleration of a moving object. In a typical two-chip hybrid approach as shown in Fig. 1(a), there is a parasitic capacitance at the interconnect resulting from the bonding wires and pads. This parasitic capacitance as well as the static sensor capacitance are usually much larger than the varying capacitance to be sensed. Additionally, there exist some unpredictable and undesired leakage currents at the sensor-electronics interface. Power consumption is another critical issue in many applications. Designing low-power interface circuits that have high sensitivity and a large dynamic range is not a trivial task.

In this paper, we propose a new approach to sensing capacitive changes. As shown in Fig. 1 (b), the circuit is composed of a capacitive feedback charge amplifier and a charge adaptation circuit. The charge amplifier in our approach operates continuously in time and can be viewed as a capacitive circuit. To cope with the charge and leakage currents at the floating node, methods based on floating-gate circuit techniques [1–3] are employed to adapt the charge. We will show that this approach can achieve a high signal-to-noise ratio (SNR).

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In the next section, we introduce some capacitive circuits that lead to a capacitive sensing implementation. The analysis of a capacitive sensing charge amplifier is detailed in section III. In section IV, we demonstrate how to use floating-gate based adaptation techniques to auto-zero the output DC voltage. An experiment conducted on a charge amplifier interfaced with a capacitive ultrasonic micromachined transducer (CMUT), demonstrates the feasibility of this approach for ultrasonic applications. A design procedure is proposed in section V. We compare our work with previous approaches and draw the conclusions in the final section.

II. Capacitive Circuits

Capacitors are natural results in a MOS process, and, therefore, the capacitive circuit approach is a practical and an efficient technique for IC designers. The transfer function expression of the capacitive circuit in Fig. 2(a) is similar to that of a resistive voltage divider. The difference is the extra voltage term, $V_Q = Q/(C_1 + C_2)$, set by the charge at the output floating node. In Fig. 2(b), the close loop gain of a capacitive circuit with a feedback around an amplifier is $-C_1/C_2$. There is also a charge dependent term, $V_Q = Q/C_2$, in the output voltage expression. Traditionally, floating-node approaches have been avoided because the charge on floating nodes is neither predictable nor controllable. However, recent advancements in the floating-gate technology, especially in programming [1] and adapting [2] floating-gate charges, make these floating-node approaches possible. The schematic shown in Fig. 2(c) is a practical capacitive sensing circuit stemming from the circuit in Fig. 2(b). All the parasitic capacitances from the floating node to the ground are modeled by C_w. This paper will show that this new design notion results in a simpler capacitive sensing circuit with better performance.

III. Charge Amplifier for Capacitive Sensing

Although the preliminary analysis has been presented elsewhere [4], [5], the complete analysis of the capacitive sensing charge amplifier will be detailed in this section. The small-signal model of the circuit in Fig. 2(c) is shown in Fig. 3(a). The amplifier is modeled as a first-order system. The topology can be a simple cascode operational transconductance ampli-fier (OTA), which is shown in Fig. 3(b), a folded cascode am-plifier, or a cascode common-source amplifier. If the amplifier has two stages, although similar results can be derived, the dominant pole will depend on the compensation capacitance and the power consumption will be larger.

A. Transfer function

We can express the DC output voltage as

$$V_{out} = -\frac{V_{bias}C_{sensor}+Q}{C_f(1+\rho)}, \tag{1}$$

where $\rho = C_T/(C_f A_v)$, $A_v = G_m R_o$, $C_T = C_{sensor} + C_w + C_f$, and Q is the charge on the floating node. Usually the amplifier gain should be designed high enough ($A_v \gg C_T/C_f$ and ρ≪ 1) so that (1) can be approximated as

$$V_{out} \approx -\frac{V_{bias}C_{sensor}+Q}{C_f} \text{ as } \quad \rho \to 0. \tag{2}$$

The DC level of V_{out} can be set at the mid-rail by either adjusting the non-inverting terminal voltage if the floating-gate charge is fixed, or by adjusting the floating-gate charge according to the output voltage.

The output voltage varies linearly with the sensor capacitance as

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$$\Delta V_{\text{out}} = -\frac{V_{\text{bias}}}{C_{\text{f}}(1+\rho)} \cdot \Delta C_{\text{sensor}}. \tag{3}$$

The circuit can achieve high sensitivity if a large value of V_{bias} and a small value of C_{f} are used. In Fig. 4, we show a music waveform recorded from a version of our capacitive sensing circuit interfaced with an audio MEMS microphone.

If the floating-node voltage is regulated by the feedback and is assumed to be constant, the transfer function can be expressed as

$$\frac{V_{\text{out}}(s)}{C_{\text{sensor}}(s)} = -\frac{V_{\text{bias}}}{C_{\text{f}}(1+\rho)} \cdot \frac{1 - sC_{\text{f}}/\text{G}_{\text{m}}}{1+s\tau}, \tag{4}$$

where τ is the time constant of the circuit and is given as

$$\tau = \frac{1}{\omega_{3dB}} = \frac{C_{\text{eff}}}{\text{G}_{\text{m}}(1+\rho)}, \tag{5}$$

where $C_{\text{eff}}=(C_{\text{o}}C_{\text{T}} - C_{\text{f}}^2)/C_{\text{f}}$ and $C_{\text{o}} = C_{\text{L}} + C_{\text{f}}$. Typically, both C_{sensor} and C_{L} are larger than C_{f}. The zero due to capacitive feedthrough is at a much higher frequency than the amplifier bandwidth. If the amplifier gain is high enough ($A_{\text{v}} \gg C_{\text{T}}/C_{\text{f}}$), the transfer function can be approximated as

$$\frac{V_{\text{out}}(s)}{C_{\text{sensor}}(s)} = -\frac{V_{\text{bias}}}{C_{\text{f}}} \cdot \frac{1 - sC_{\text{f}}/\text{G}_{\text{m}}}{1+sC_{\text{eff}}/\text{G}_{\text{m}}}. \tag{6}$$

B. Noise analysis

We can calculate the output-referred noise power from the small signal model in Fig. 3(c). If V_{fg} and V_{out} are related by a capacitive divider, the small signal model can be further simplified as shown in Fig. 3(d), where $R_{\text{x}} = C_{\text{T}}/(C_{\text{f}}\,\text{G}_{\text{m}})$. The output-referred voltage noise can be expressed as

$$\widehat{V}_{\text{out,total}}^2 = \frac{\tilde{i}_{\text{o}}^2}{4\text{G}_{\text{m}}} \cdot \frac{C_{\text{T}}}{C_{\text{f}}C_{\text{o}}} \cdot \frac{1}{1+\rho} \tag{7}$$

$$= \frac{nqU_{\text{T}}}{2\kappa} \cdot \frac{C_{\text{T}}}{C_{\text{f}}C_{\text{o}}} \cdot \frac{1}{1+\rho}. \tag{8}$$

In (8), the differential pair transistors are assumed operating in the subthreshold region and

$$\tilde{i}_{\text{o}}^2 = \frac{2}{\kappa} nqU_{\text{T}}\text{G}_{\text{m}} \quad (\text{A}^2/\text{Hz}), \tag{9}$$

where κ is the subthreshold slope coefficient of a MOS transistor, n is the effective number of noisy transistors, q is the charge of an electron, U_{T} is the thermal voltage, and G_{m} is the transconductance of a transistor. The result is consistent with that in [6] where the transistors are assumed operating in the above threshold region.

C. Maximum dynamic range analysis

Assuming that the nonlinearity of the circuit comes from the voltage-controlled current source of the transconductance amplifier, we define $\Delta V_{\text{lin,max}}$ as the maximum input linear voltage.

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When the input voltage is smaller than or equal to $\Delta V_{\text{lin,max}}$, the output current is linear to the input voltage with some tolerable distortion. For example, if the OTA shown in Fig. 3(b) is used and the differential pair operates in the subthreshold region, we can have the I-V relation as

$$I_{\text{out}} = I_{\text{b}} \tanh\left(\frac{\kappa V_{\text{d}}}{2U_{\text{T}}}\right) \tag{10}$$

$$\approx I_{\text{b}} \frac{\kappa \Delta V_{\text{fg}}}{2U_{\text{T}}}, \tag{11}$$

where I_{b} is the tail current and V_{d} is the OTA input differential voltage. The hyperbolic-tangent function causes the nonlinearity of the circuit. In Fig. 5 we plot the relation between the total harmonic distortion and the maximum input linear range, $\Delta V_{\text{lin,max}}$, of the differential pair. If $V_{\text{d}} \leq \Delta V_{\text{lin,max}} = 8$ mV, we can approximate

$$\text{G}_{\text{m}} \approx \frac{\kappa \text{I}_{\text{b}}}{2U_{\text{T}}} \tag{12}$$

with −60 dB total harmonic distortion.

The maximum output linear range, $\Delta V_{\text{out,max}}$, can be obtained from the transfer function of V_{fg} to V_{out} as

$$\begin{aligned} |\Delta V_{\text{out, max}}(j\omega)| &= \left|\frac{(j\omega)C_{\text{f}} - \text{G}_{\text{m}}}{(j\omega)C_{\text{o}} + \text{G}_{\text{m}}/\text{A}_{\text{v}}} \Delta V_{\text{fg}}(j\omega)\right| \\ &\leq \left|\frac{(j\omega)C_{\text{f}} - \text{G}_{\text{m}}}{(j\omega)C_{\text{o}} + \text{G}_{\text{m}}/\text{A}_{\text{v}}}\right| |\Delta V_{\text{lin, max}}. \end{aligned} \tag{13}$$

A normalized variable, η, can be defined as $\eta = \omega/\omega_{3dB} = \omega\tau$. We can rewrite (13) as

$$|\Delta V_{\text{out,max}}(\eta)| \leq \frac{C_{\text{T}}}{C_{\text{f}}} \cdot \frac{\Delta V_{\text{lin,max}}}{\sqrt{\eta^2(1+\rho)^2 + \rho^2}}. \tag{14}$$

If the gain of the amplifier and the bandwidth of the circuit are both infinite (i.e. $\rho = 0$ and $\eta = 0$ respectively), from (14), it implies that the maximum output linear range is also infinite. The circuit is completely linear in this ideal scenario, if the limitations from supply rails are not taken into account.

In reality, the amplifier has a high but finite gain ($0 < \rho \ll 1$) and, to save power, the operating frequency is usually close to and within the bandwidth ($\eta \approx 1$). We can approximate (14) as

$$|\Delta V_{\text{out,max}}(\omega)| \leq \frac{\text{G}_{\text{m}}}{C_{\text{o}}} \cdot \frac{\Delta V_{\text{lin,max}}}{\omega}. \tag{15}$$

From (15), we can increase the output linear range by increasing the G_{m} or by decreasing the load capacitance. If the $\Delta V_{\text{out,max}}$ is defined as the maximum output linear range in the worst scenario within the bandwidth, we can have

$$\begin{aligned} \Delta V_{\text{out,max}} &\equiv \inf_{0<\omega\leq\omega_{3dB}} \frac{\text{G}_{\text{m}}}{C_{\text{o}}} \cdot \frac{\Delta V_{\text{lin, max}}}{\omega} \\ &= \frac{\text{G}_{\text{m}}}{C_{\text{o}}} \cdot \frac{\Delta V_{\text{lin, max}}}{\omega_{3dB}} \\ &= \frac{C_{\text{T}}}{C_{\text{f}}} \cdot \Delta V_{\text{lin, max}}, \end{aligned} \tag{16}$$

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which is the lower bound of the maximum output linear range.

D. SNR analysis

The lower bound of the circuit SNR can be obtained from (16) and (8) and can be expressed as

$$SNR \geq C_{\text{eff}} \cdot \frac{2\kappa \Delta V_{\text{lin,max}}{}^2}{nqU_{\text{T}}}. \tag{17}$$

We can also express the SNR as a function of the frequency,

$$SNR(\omega) \approx \frac{2\kappa(1+\rho)G_{\text{m}}^2 \Delta V_{\text{lin,max}}{}^2}{C_{\text{eff}} nqU_{\text{T}} \omega^2}. \tag{18}$$

For a given signal frequency, the SNR can be increased by increasing G_m or decreasing C_{eff}.

E. Setup and measurement results

A version of the capacitive sensing circuit was fabricated in a 0.5 μm double-poly CMOS process. A MEMS microphone sensor fabricated in the Sandia National Laboratory's silicon based SwIFT-Lite process [7] is used to test the circuit. The typical value of the sensor capacitance is in the range of pico farads. The measurement setup and the micrographs are shown in Fig. 6. An ultra-thin card type speaker is used as the acoustic signal source. A tunneling junction and an indirect injection transistor are integrated on the chip as parts of the floating-node charge adaptation circuit. To measure the characteristics without any charge adaptation circuit, both tunneling and drain voltages are tied to 3.3V. The floating-node voltage can settle slowly to an equilibrium value, which is very sensitive to the environmental electromagnetic interference. To avoid the perturbation of the floating-node voltage, the chip and the sensor are placed inside a shielding metal box. In this setup, we can carefully adjust the non-inverting terminal voltage to set the output DC level at the mid-rail.

The spectrum of a output waveform with 1V magnitude at 1kHz with -38dB total harmonic distortion is shown in Fig. 7. The distortion comes from the offset, the cascoded output stage of the amplifier, as well as the nonlinearity of the speaker and the MEMS sensor. In the same plot, we also show the noise spectrum of the sensing circuit without the MEMS sensor. The output noise depends on the input capacitance as analyzed in (8). To have a better idea of the circuit noise performance when it is interfaced with a MEMS sensor, we replace the sensor with a 2 pF linear capacitor. By varying the tail current of the OTA, three noise spectrums that have power consumption of 1 μW, 0.23 μW, and 0.13 μW are measured and plotted in Fig. 8. As expected from (5) and (8), increasing G_m results in a higher bandwidth with the cost of more power consumption, but the total output thermal noise is independent of G_m. If the sensing circuit is followed by a low-pass filter that limits the noise bandwidth inside the audio band (i.e. 20Hz to 20kHz with uniform weighting), the resulting output noise can be reduced by burning more power.

The integrated total output noise over the entire bandwidth is 570 μV_{rms}. The integrated thermal noise is 520 μV_{rms}, which is slightly higher than 370 μV_{rms}, estimated from (8). When the power consumption is 1 μW, the 1/f corner is around 2kHz, and the integrated flicker noise in that range is 225 μV_{rms}. The integrated total output noise in the audio band is 341 μV_{rms}. The corresponding minimum detectable capacitance variation in the audio band is 83 aF, which can be derived from (6) using the parameters listed in TABLE I. The capacitance sensitivity in the audio band is $0.59\ \text{aF}/\sqrt{\text{Hz}}$ and the minimum detectable displacement is

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$20.76 \times 10^{-4}\ \mathring{A} / \sqrt{\text{Hz}}$. The SNR of the circuit is 64.88dB over the entire bandwidth and is 69.34dB in the audio band with the power consumption of 1 μW.

IV. Capacitive Sensing with Charge Adaptation

In the previous section, we have shown that using capacitive feedback charge amplifier to sense capacitance change can achieve high SNR with low power consumption. The performance will be compared with other works in section VI. Although we can set the output DC level by adjusting the voltage at the non-inverting terminal, it is not stable. Without the shielding metal box, the output voltage is prone to being saturated to the supply rails because the floating-node voltage is very sensitive to the electromagnetic interference in the testing environment. In this section, we demonstrate how the floating-gate techniques are employed to stabilize the output DC level.

A. Setup and measurements for audio applications

The schematic used to demonstrate the capacitive sensing circuit with the charge adaptation circuit is shown in Fig. 9. To reduce the leakage current caused by the ESD protection circuits, the sensor is bonded to the chip with electronics via a bare pad. The leakage current at the connection can be integrated directly by the charge amplifier. The measured leakage current ranges between 5 fA and 1 pA depending on the biasing voltage and the supply rails.

A tunneling junction and an injection transistor are integrated on chip to compensate for the leakage current. Fowler-Nordheim tunneling current brings electrons away from the floating gate when there is a high voltage across the MOS-capacitor tunneling junction. On the other hand, when there is a high channel-to-source field across the injection transistor with enough channel current, channel hot electrons will be injected onto the floating gate. For a *p*FET transistor, the injection current can be modeled as:

$$I_{\text{inj}} = I_{\text{inj0}} \left(\frac{I_{\text{s}}}{I_{\text{s0}}} \right)^{\alpha} \exp\left(-\frac{\Delta V_{\text{ds}}}{V_{\text{inj}}} \right), \tag{19}$$

where I_{inj0} is the quiescent injection current, I_{s} is the source current, I_{s0} is the quiescent source current, V_{inj} is a device and bias dependent parameter, and α is very close to 1 [2]. The injection current can be controlled by the transistor drain voltage. One of the many possible ways to control the drain voltage according to the output DC level is shown in Fig. 9. In this adaptation scheme, the tunneling voltage is kept constant and only the injection current varies to compensate for the leakage current. The adaptation scheme can auto-zero the output DC voltage to the mid-rail without affecting circuit performance. The dynamics of these two mechanisms are detailed in [8].

To have enough field to generate the injection current, the supply rail is raised to 6.5V and the externally applied tunneling voltage is 13V. As shown in Fig. 10, the output voltage is adapted to the mid-rail after an upward or a downward step is applied to the sensor bias voltage. The extracted time constants are 5 seconds and 30 seconds respectively. This implies that the effective resistance caused by the adaptation scheme is in the scale of $10^{12}\Omega$. Increasing the tunneling voltage results in a faster adaptation rate because of the larger tunneling current.

The noise spectrums with and without this adaptation scheme are compared in Fig. 11. It is shown that this adaptation scheme does not degrade the noise performance over the frequency band of interest. Introducing the floating-gate adaptation currents makes the low frequency corner slightly higher. The corner frequency is at 0.2Hz and is consistent with the extracted time constants from Fig. 10.

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The power consumption in the charge adaptation circuit in Fig. 9 is in the range of milli-watt because the adaptation circuit is made up of discrete components. If these transistors are also integrated on chip and are designed to be long, the power consumption can be much lower. If the charge adaptation is implemented by using the topology of autozeroing floating-gate amplifier introduced in [2], no extra power is consumed for the charge adaptation.

The externally applied tunneling voltage can be generated on chip using charge pump circuitry. In this case, the tunneling voltage, as well as the tunneling current, can be adjusted by the input voltage or the clock frequency of the charge pump. Consequently, the adaptation time constant can also be tuned on chip. Since the tunneling junction is small and the tunneling current is in the range of pico- or nano-amps, the extra cost of the silicon area and the power consumption of the charge pump circuitry, including the clock generator, diodes, and capacitors, is usually low. In some applications, if the medium of the sensor is leaky and the leakage current is large enough to provide a fast adaptation time constant, the tunneling current is not necessary for charge adaptation. In this case, the tunneling voltage generator circuitry, as well as the tunneling junction, can be avoided altogether.

B. Setup and measurements for Ultrasonic Applications

The charge amplifier approach is also applied to sensing capacitive micromachined ultrasonic transducers (CMUT), which have been recently developed for ultrasound imaging [9], [10]. The measured leakage current of the CMUT device can be up to 500 pA. Since the operating frequency is high, besides the tunneling-injection adaptation scheme, MOS-bipolar pseudo-resistors can be used to provide the DC path to the floating node. Although transistors operating in the weak inversion region can also be used as large floating resistors [11], unlike the MOS-bipolar pseudo-resistors, their gate voltages need to be carefully biased.

A MOS-bipolar pseudo-resistor is a *p*FET transistor with the connection from the gate to the drain and the connection from the bulk to the source. It exhibits a very large resistance (exceeding $10^{12}\Omega$) when the cross voltage is close to zero. Pseudo-resistors have been used in quasi-floating-gate transistor circuits [3] and the neural recording application [12]. To extend the output linearity, we use two pseudo-resistors in series to provide the DC path to the floating node.

The setup for the ultrasonic measurement is illustrated in Figure 12. A piezo transducer is used to generate plane waves at 1MHz using 16V peak 5 cycle tone bursts at its input. The CMUT receiver is biased to 90V DC at one of its terminals. The other terminal is connected to the sensing amplifier. The CMUT and the piezo device are submerged in the oil during the measurement. The capacitance of the CMUT sensor is about 2 pF and the maximum variance is about 1%. The resulting waveforms are also shown in Fig. 13. The initial, highly distorted signal is due to the electromagnetic feedthrough. After 15 microseconds the first acoustic signal arrives from the piezo transducer to the CMUT receiver, which corresponds to a distance of 2.2 cm in the oil, as expected. By changing this distance and the relative alignment of the piezo and CMUT devices, the received signal and multiple echoes change drastically, again as expected from an ultrasound transmission experiment. Some important parameters for the CMUT measurement are listed in TABLE II.

V. Design Procedure

Given the specifications of the minimum detectable capacitance (ΔC_{min}), the bandwidth (ω_{3dB}), and the SNR, we try to optimize the current consumption (I_b), the feedback capacitance (C_f), and the load capacitance (C_L). The known variables include the total capacitance seen from the floating node ($C_T \approx C_{sensor} + C_w$), the bias voltage of the sensing capacitor (V_{bias}), and the maximum input linear voltage of the transconductance amplifier ($\Delta V_{lin,max}$). We also

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assume that the maximum output linear range is not limited by the supply rails but only by the nonlinearity of the OTA.

The design starts from the sensitivity expression

$$\Delta C_{\min}^2 = \tilde{V}_{\text{out,total}}^2 \cdot \left(\frac{C_f}{V_{\text{bias}}}\right)^2 = \frac{nqU_T}{2\kappa V_{\text{bias}}^2} \cdot \frac{C_T C_f}{C_o}, \tag{20}$$

where $\Delta C_{\min}$ is the minimum detectable capacitance. From (20) we can have

$$\frac{C_f}{C_L} \le \frac{\Delta C_{\min}^2}{C_T} \cdot \frac{2\kappa V_{\text{bias}}^2}{nqU_T}. \tag{21}$$

Since only the ratio of C_f to C_L matters, these two capacitances can have reasonable and practical values.

The next step is to determine the current consumption for a given C_f/C_o ratio. Assuming that the differential pair transistors of the OTA operate in the subthreshold region, we can substitute (12) into (5) and (18) and obtain

$$\frac{\kappa}{2U_T} \cdot \frac{I_b}{C_{\text{eff}}} \cdot \omega_{3dB} \tag{22}$$

$$\frac{\kappa^3 \Delta V_{\text{lin,max}}{}^2}{2nqU_T^3\omega^2} \cdot \frac{I_b^2}{C_{\text{eff}}} \ge SNR(\omega). \tag{23}$$

We can estimate the required current as

$$I_b \ge \omega_{3dB} \cdot \frac{2U_T}{\kappa} \cdot \frac{C_o C_T}{C_f} \tag{24}$$

$$I_b \ge \sqrt{SNR \cdot \frac{2nqU_T^3\omega^2}{\kappa^3 \Delta V_{\text{lin,max}}{}^2} \frac{C_o C_T}{C_f}}. \tag{25}$$

The current consumption is usually determined by (24).

VI. Comparison and Conclusion

One common approach to detecting capacitive changes is using the switched-capacitor (SC) circuit with a charge amplifier [13], as shown in Fig. 14(a). Switches are inserted to reset the charge on the connecting node. Correlated double sampling (CDS) [14] techniques are also used [15], [16] to reduce the low-frequency noise and the DC offset. Issues like noise-folding, clock feed-through, and charge sharing need to be taken care of. For applications that require very high sensitivity, lock-in capacitive sensing is one of the most popular techniques [17–19]. As shown in Fig. 14(b), because of the modulation scheme, these circuits consume lots of power, usually in the milli-watt range and are very complicated. In either the SC or lock-in approaches, the sensing circuits process the entire charge on the sensing capacitor, instead of only the minute portion caused by the capacitance change. To cancel the effect of the large static capacitance, differential capacitor structures are necessary.

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The differential capacitor structure is not available in the MEM capacitive microphone sensor. Traditional approaches usually convert the capacitive current into a voltage that is amplified in the following stages. A self-biased JFET buffer shown in Fig. 14(c) is the most commonly used interface circuit for electret condenser microphones (ECMs). However, JFET is not compatible to the CMOS process and the gain is highly sensitive to the parasitic interconnect capacitance. In [20], the current through the JFET is sensed and amplified to improve the power supply rejection ration (PSRR) as shown in Fig. 14(d). Other approaches use diodes [21], [22] or a unity-gain feedback OTA [23] as a large resistor to convert the current to a voltage. The resulting voltage can be amplified directly or can be buffered and amplified in the next stage, as shown in Fig. 14(e)-(h). These approaches usually have much lower power consumption compared with the SC and the lock-in techniques. However, the linearity is usually poor. In this work, we can achieve ultra-low power consumption and a large output dynamic range with high linearity. We compare our work with others in TABLE III.

Although the capacitive feedback charge amplifier is a simple topology, we detailed the noise, the maximum dynamic range, and the SNR analysis in this paper. Because the circuit only amplifies the charge resulting from the capacitance change in the first stage without any I-V conversion or modulation, it consumes ultra low power and achieves high linearity. An auto-zeroing method adopting from floating-gate circuit techniques has been demonstrated to deal with the charge and the leakage current at the floating node without affecting the performance. Pseudo-resistors can also be used to provide the DC path to the floating node. We have demonstrated these techniques in the applications of audio MEMS microphones and ultrasonic transducers.

Acknowledgements

This research is partially funded by the NIH Grants 5R01DC005762 and 1R01HL082811.

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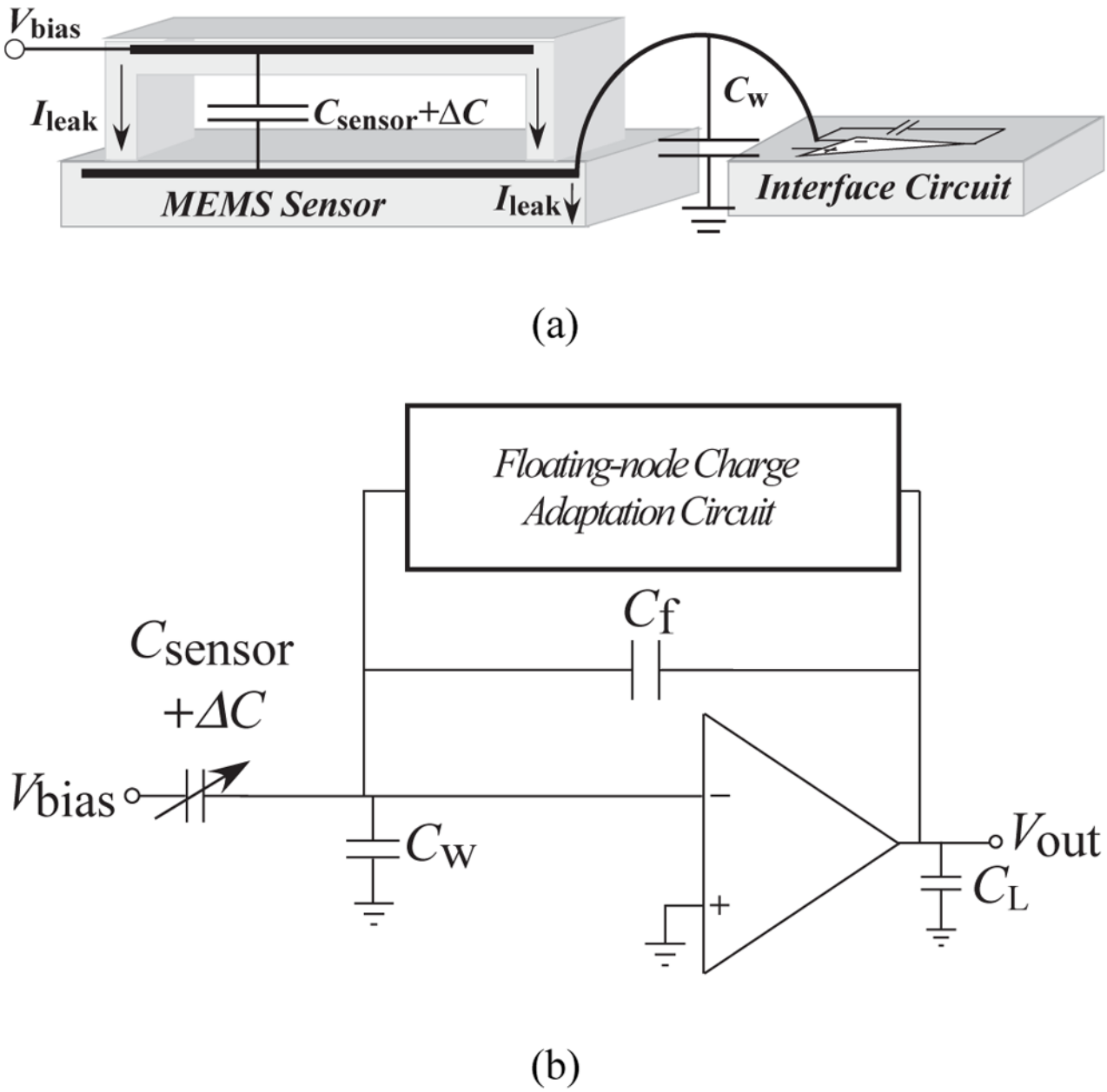

Fig. 1. Capacitive sensing diagrams

(a) In a typical two-chip hybrid approach, the small variance of the sensing capacitor, Δ***C***, the large parasitic capacitance, $\boldsymbol{C}_{\mathrm{w}}$, and the static capacitance, $\boldsymbol{C}_{\mathrm{sensor}}$, as well as the leakage currents at the interconnect make the sensing circuit design a challenge. (b) A new approach to sensing capacitive change by using a charge amplifier with a charge adaptation circuit.

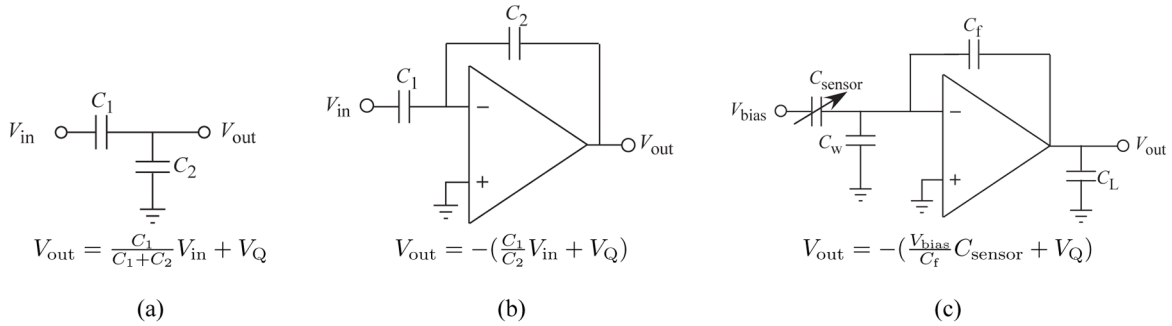

Fig. 2. Capacitive circuits

(a) A capacitive voltage divider. (b) A capacitive feedback amplifier. (c)A capacitive feedback amplifier for capacitive sensing.

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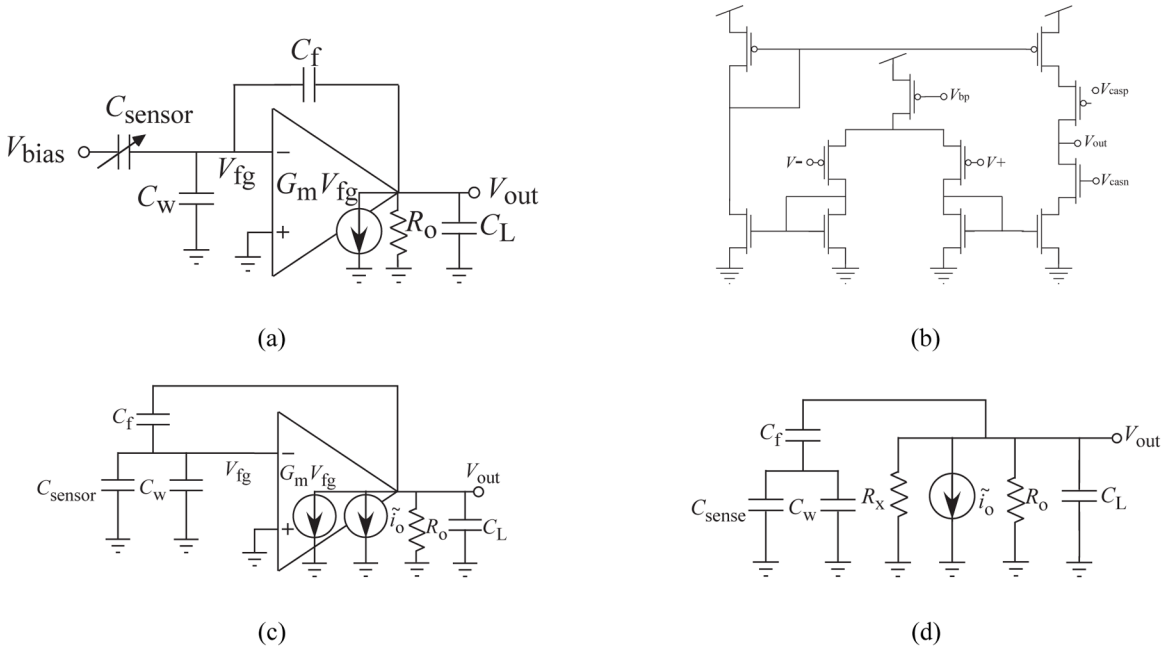

Fig. 3. Schematics of small signal models and a cascode OTA

(a) The small-signal model of the capacitive sensing circuit. (b) A single-stage cascode operational transconductance amplifier. (c) The small-signal model of (a) for noise analysis. (d) The simplified small-signal model from (b) for noise analysis.

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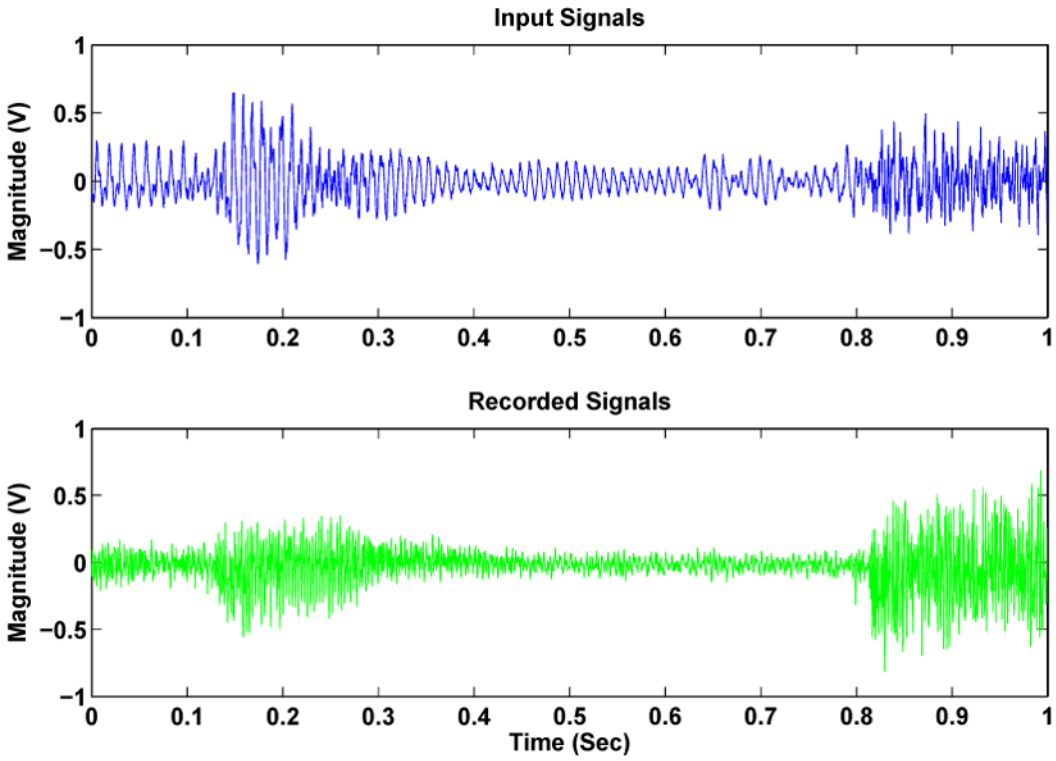

Fig. 4. Measured waveform

The input music waveform and the recorded waveform from a capacitive feedback amplifier. The distortion comes from the nonlinearity of the speaker, the background 60Hz noise, the offset of the OTA, and the limitation of the supply rails.

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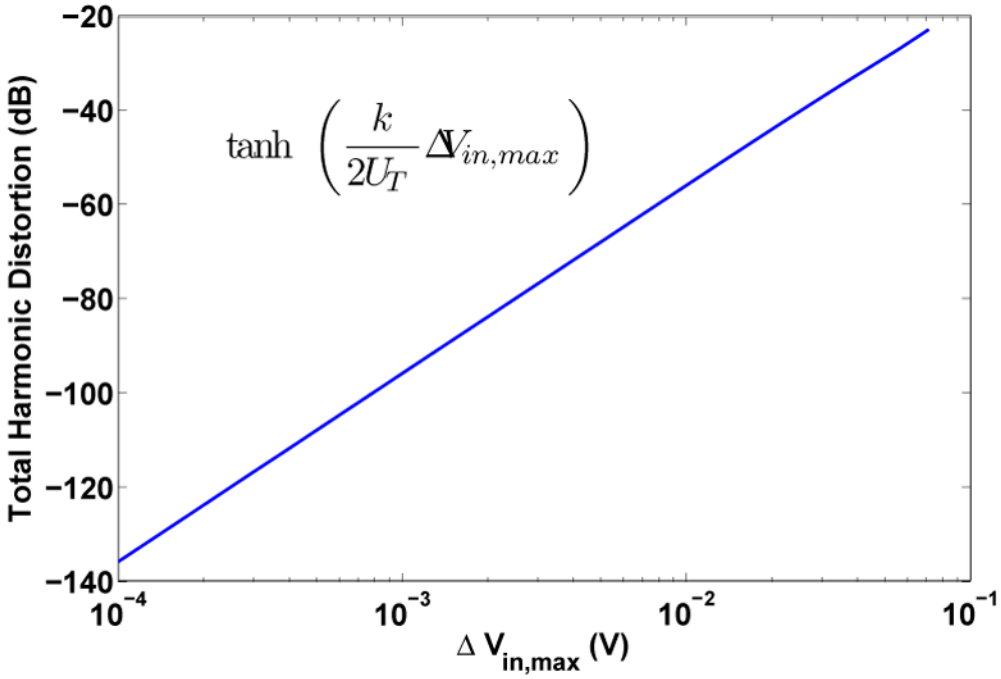

Fig. 5. Nonlinearity of an OTA

The relation between the total harmonic distortion (THD) and the maximum input linear voltage of a differential pair in the subthreshold region. The total harmonic distortion is calculated from (10) with U_T = 25 mV and κ = 0.7

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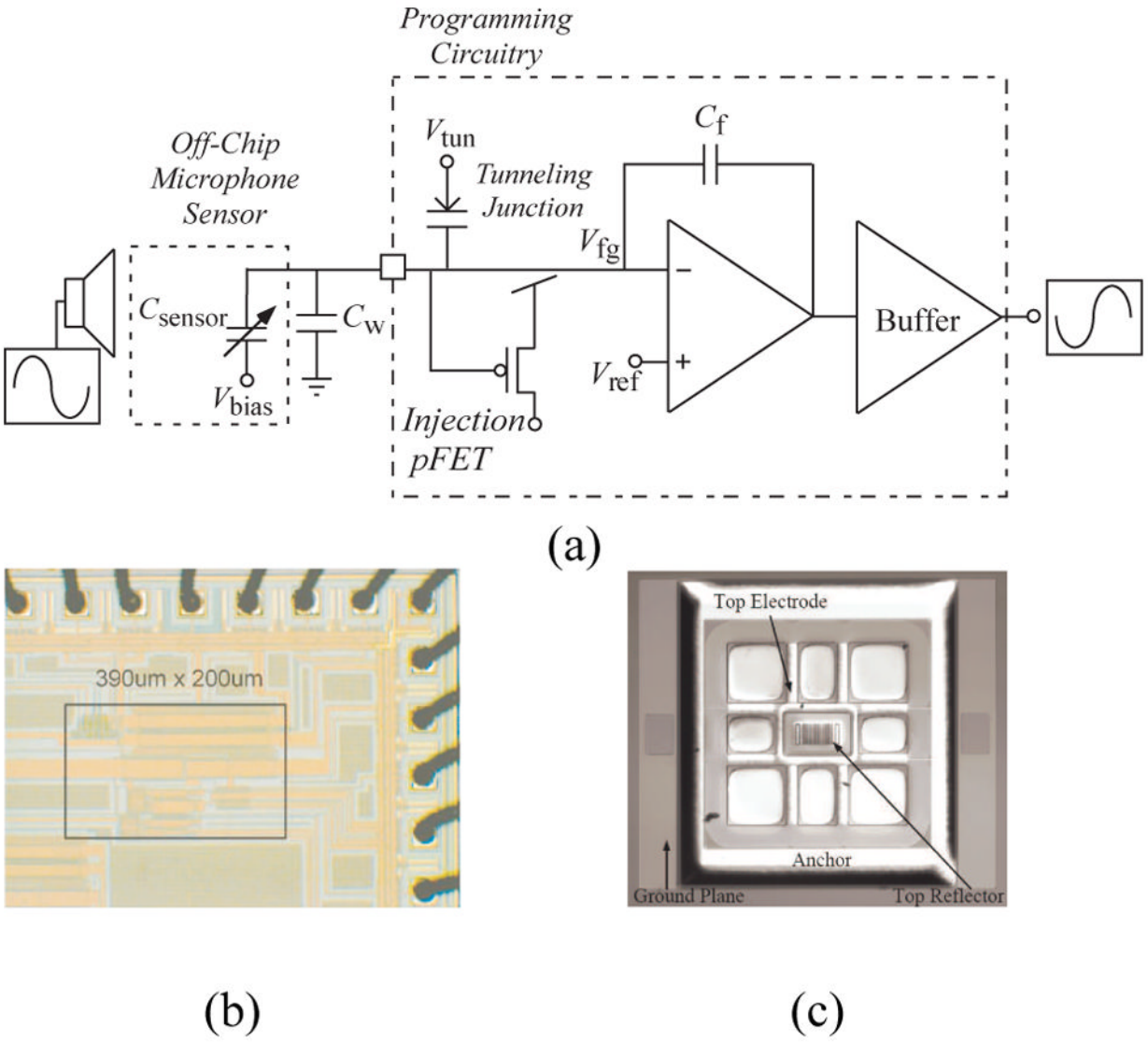

Fig. 6. The setup for audio measurements and the micrographs

(a) Setup of the capacitive sensing measurement. The charge adaptation circuitry is disabled by connecting the tunneling and the drain voltages to 3.3V. The non-inverting terminal voltage is adjusted so that the output voltage is at the mid-rail. (b) A die micrograph of a version of the capacitive feedback amplifier fabricated in a 0.5 μm double-poly CMOS process. (c) A micrograph of the MEMS sensor used in the measurement.

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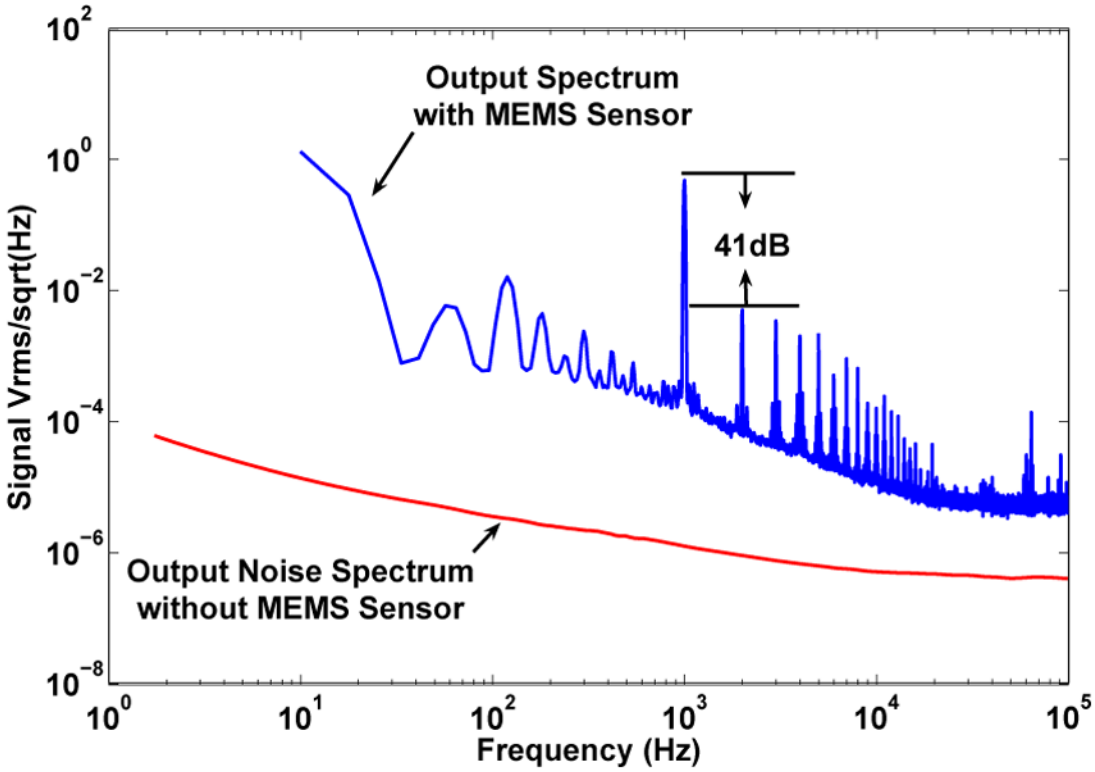

Fig. 7. The measured output signal and noise spectrums

A card type speaker is used as the 1K Hz acoustic signal source and a MEMS microphone is interfaced with the circuit. -38dB THD is observed when the output is 1*V*rms.

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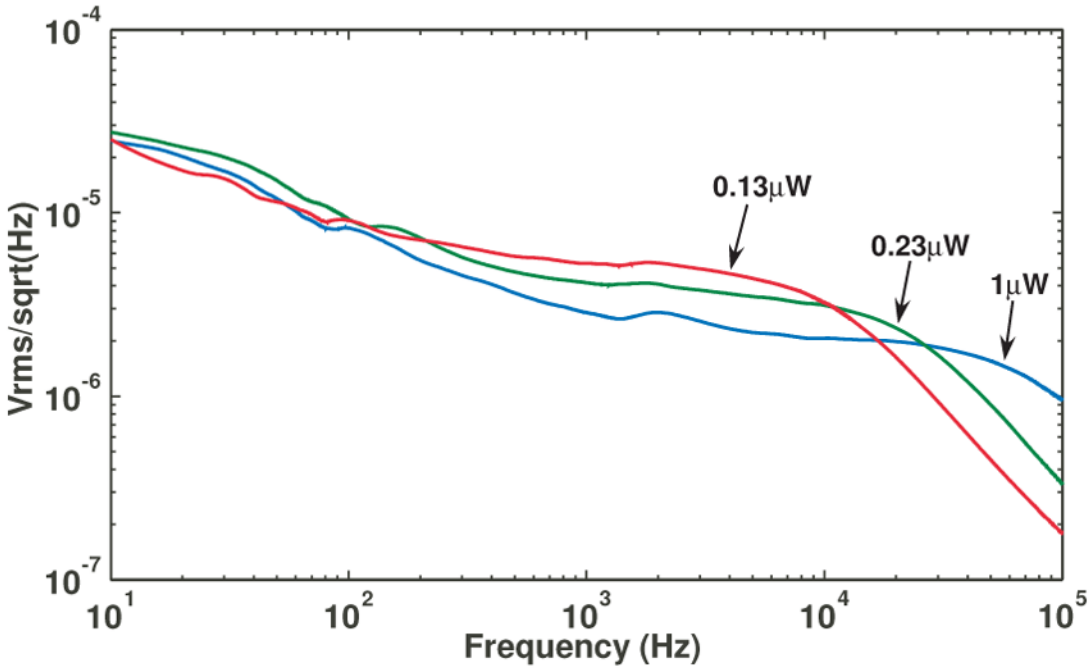

Fig. 8. Noise spectrums of a charge amplifier with a linear input capacitor

The circuit is connected to a linear 2 pF capacitor. The tail current of the OTA amplifier is tunable and the corresponding power consumptions of the three noise spectrums are 1 μW, 0.23 μW, and 0.13*uW* respectively. The bandwidth increases as the power increases but the total output noise remains constant. The noise in the audio band can be reduced by consuming more power if the circuit is followed by a low-pass filter.

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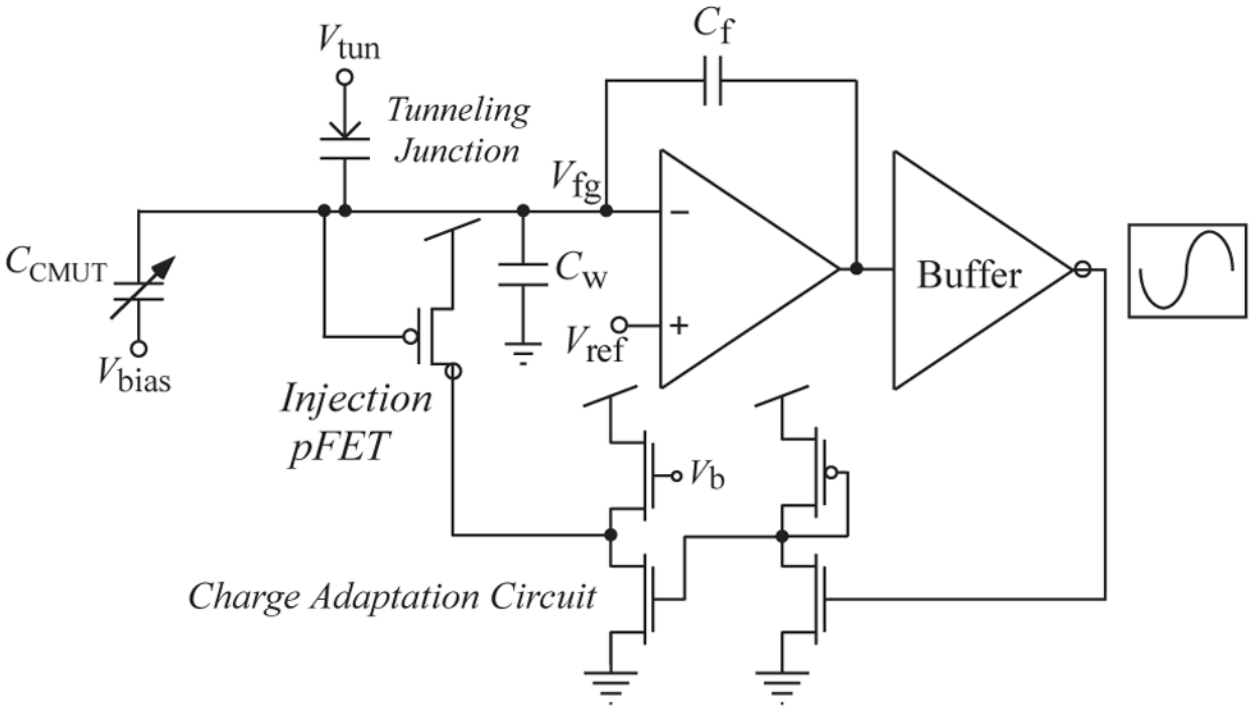

Fig. 9. Setup for the measurement with charge adaptation scheme

A an indirect injection transistor and a tunneling junction are integrated on chip. A comparator composed of discrete transistors provides the drain voltage of the injection transistor so that the injection current can balance out the tunneling and the leakage currents.

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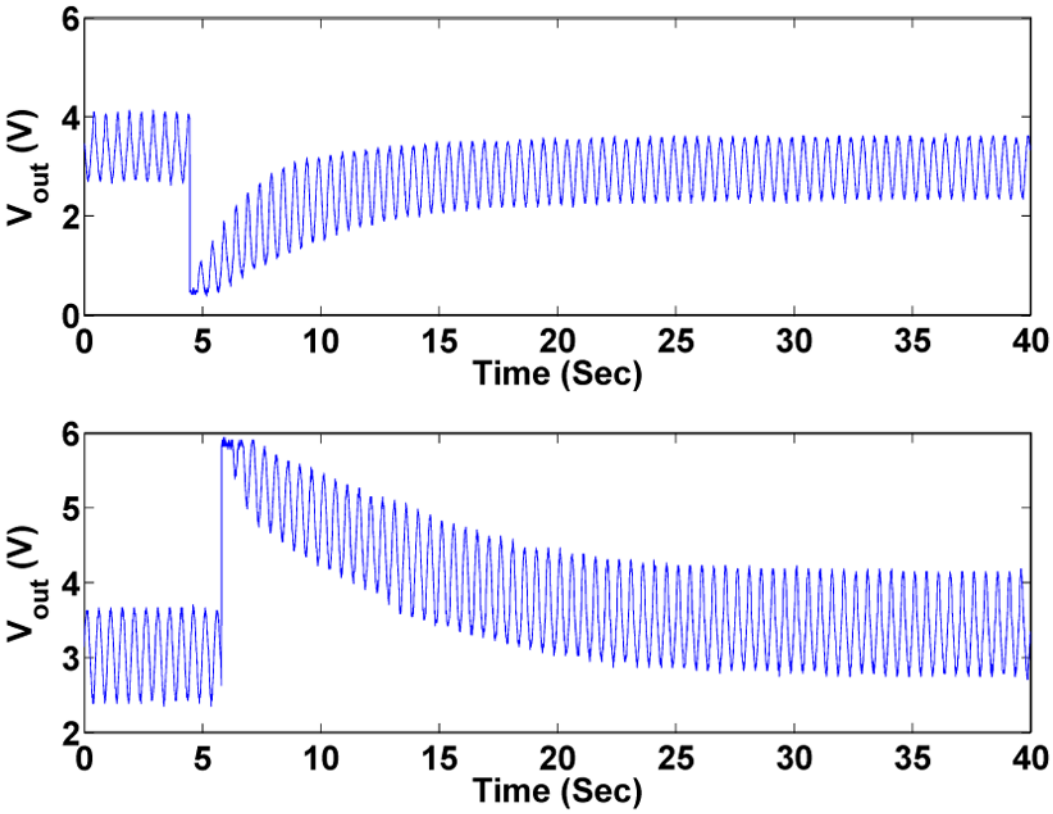

Fig. 10. Adaptation step responses

Steps from 0V to 5V and from 5V to 0V are applied to the biased terminal of the sensor. The output voltage is adapted to the mid-rail by the injection and the tunneling mechanisms.

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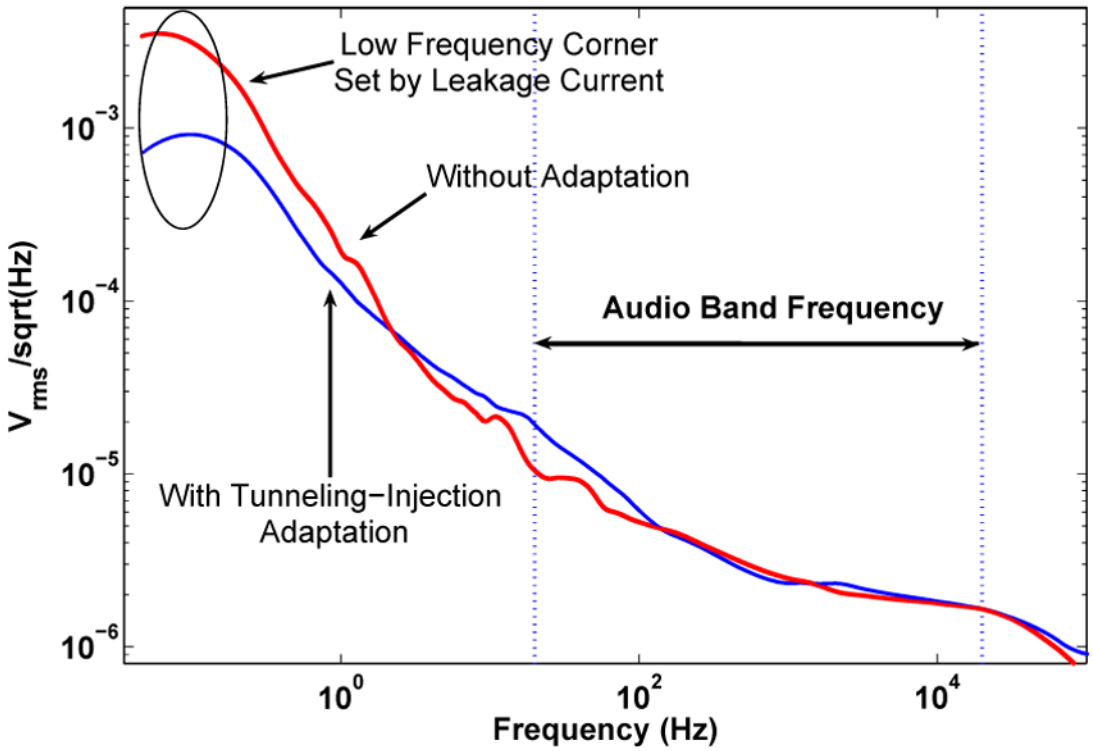

Fig. 11. Noise spectrum comparison

Using the tunneling and the injection mechanisms to autozero the output voltage does not affect the noise performance of the circuit over the frequency band of interest. Both spectrums are measured with audio MEMS sensor.

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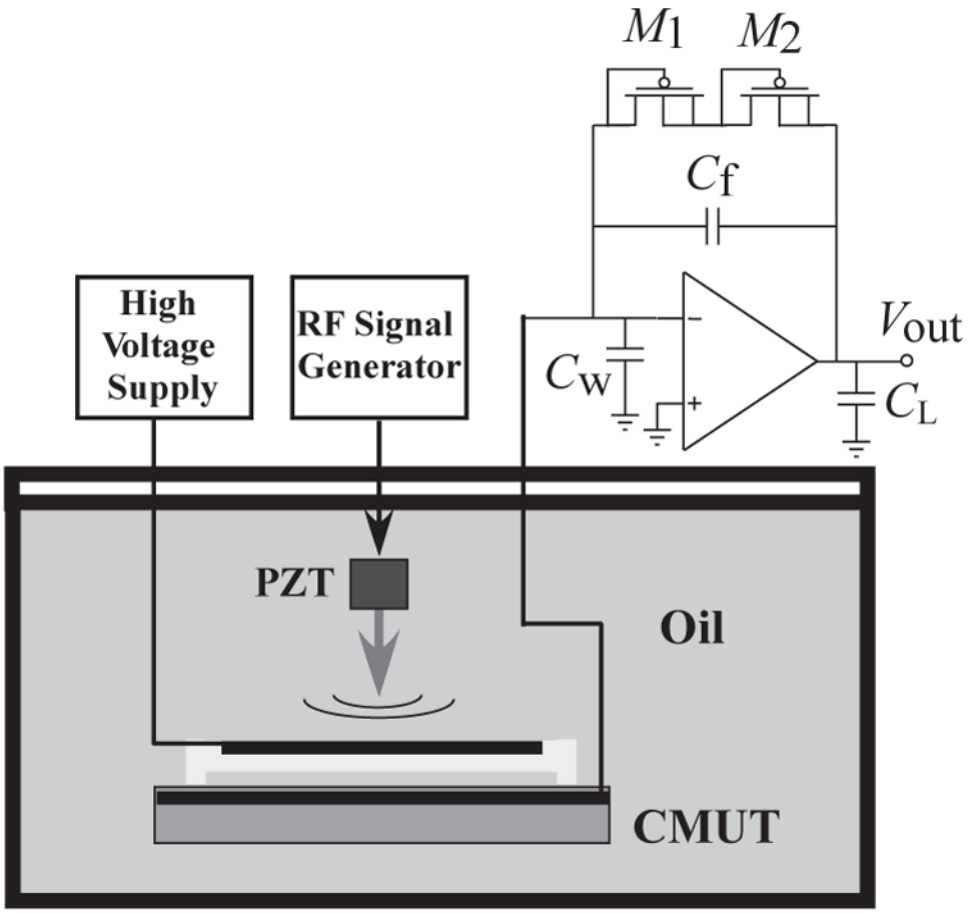

Fig. 12. Setup for the ultrasonic measurement

A capacitive sensing circuit is connected to a CMUT device. MOS-bipolar pseudo-resistor feedback scheme is used to stabilize the output DC voltage.

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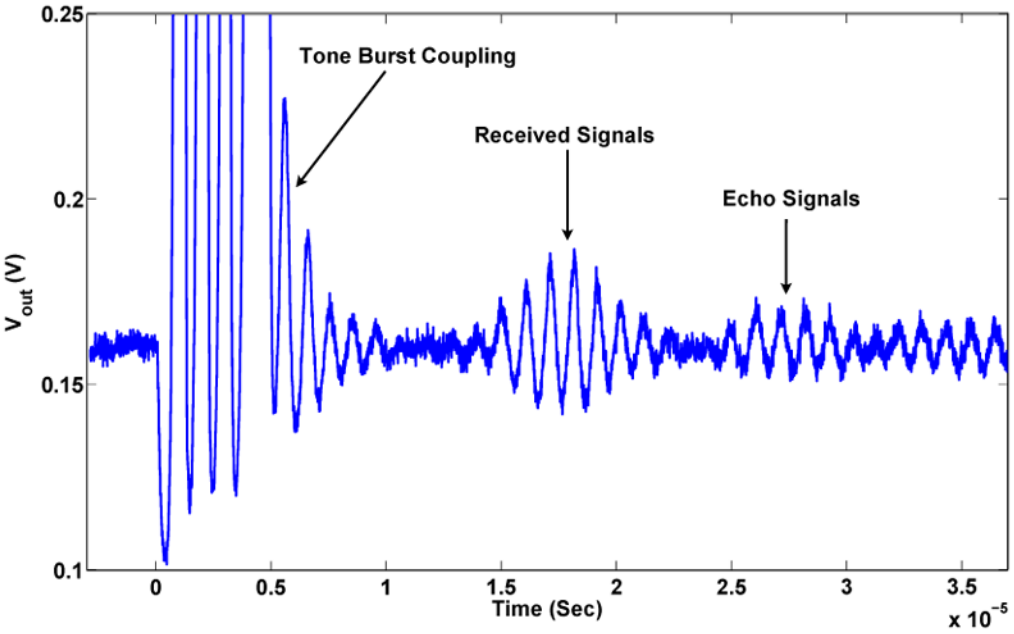

Fig. 13. Measured waveform from an ultrasonic transducer

The measured waveform from a charge amplifier that is connected to a CMUT device with a MOS-bipolar pseudo-resistor feedback scheme. The first acoustic signal arrives 15 microseconds after the piezo transducer is activated.

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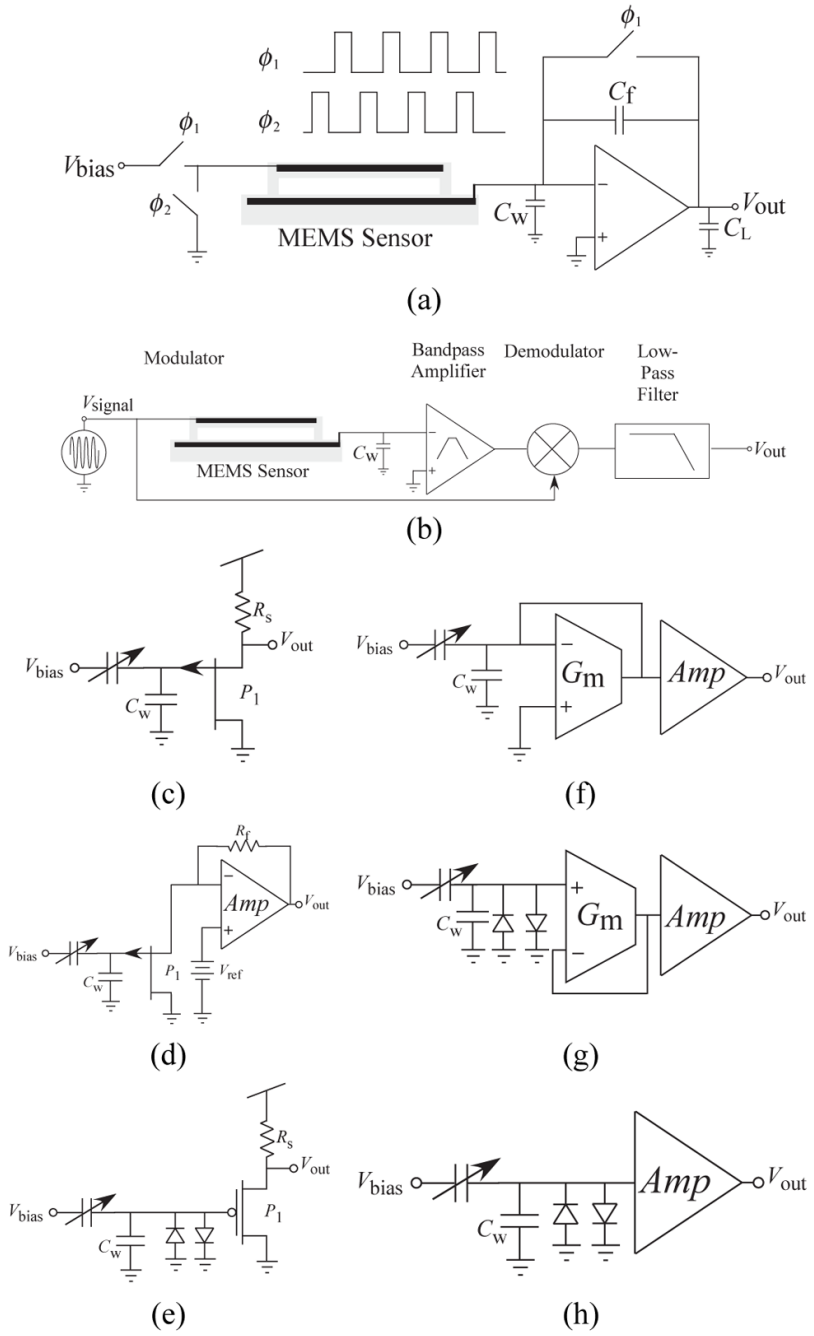

Fig. 14. Previous approaches to capacitive sensing

(a) Switched-capacitor approach. (b) Lock-in approach. (c) A self-biased JFET buffer as a microphone interface circuit. (d) The current through JFET is sensed and amplified to improve PSRR. (e)-(h) Diodes or linearized OTA are used as a large resistor and the voltage is directly amplified or buffered and then amplified.

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Table I

Audio MEMS Sensor Measurement Parameters and Results

CIRCUIT PARAMETERS	
Area	$390 \times 200\ \mu m^2$
Power Supply	3.3V
Amplifier Power Consumption	$1\ \mu W$
Open-Loop Gain	80 dB
Sensor Bias Voltage V_{bias}	3.3V
Feedback Capacitance C_f	800 fF
MEASUREMENT RESULTS AND PERFORMANCE	
Measured Leakage Current	5 fA to 1 pA
Output-referred Noise (Audio Band)	$341\ \mu Vrms$
Signal to Noise Ratio (Audio Band)	69.34 dB
Min. Detectable Capacitance (Audio Band)	83 aF
Capacitance Sensitivity @1kHz	$0.59\ aF/\sqrt{Hz}$
Min. Detectable Displacement @1kHz	$20.76 \times 10^{-4} A/\sqrt{Hz}$

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Table II

CMUT MEasurement Parameters

Amplifier Power Supply	3.3V
CMUT Bias Voltage	90*V*
CMUT Leakage Current	500 pA
CMUT Capacitance	2 pF
Piezo Transducer Frequency	1*MHz*
CMUT and Piezo Transducer Spacing	2.2*cm*

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Table III

Performance Comparison

Method	**[17] Fig. 14(b)**	**[19] Fig. 14(b)**	**[22] Fig. 14(e)**	**[20] Fig. 14(d)**	**[21] Fig. 14(h)**	**[23] Fig. 14(f)**	**This work Fig. 6**
Differential Cap.	Yes	Yes	No	No	No	No	No
Bandwidth (Hz)	2K	1 ~ 100	100 ~ 15K	100 ~ 10K	100 ~ 10K	100 ~ 10K	20 ~ 20K
Noise floor	1.12 aF	3.75 aF	27 dB SPL	4.8 μV_{rms}	25 dB SPL	30 μV_{rms}	83 aF
Output ref. noise	316 μV_{rms}	4.1 μV_{rms}	4.5 μV_{rms}	~ 100 μ_{Vrms}	5.6 μV_{rms}	300 μV_{rms}	341 μV_{rms}
$V_{out,max}$	0.13V	-	0.2V	0.51V	0.5V	0.2V	1V
THD	−60 dB	-	−20 dB	−40 dB	-	−50 dB	−38 dB
SNR (dB)	77	-	93	80	95	54	69
Power	30 mW	20 mW	150 μW	96 μW	60 μW	24 μW	1 μW